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CMP – Applications and Issues Part 2

By Christopher Henderson

Last month we discussed some of the fundamental concepts of Chemical Mechanical Polishing (CMP), as well as the application of CMP to metal interconnect. In this month's issue we'll discuss CMP for oxides.

Oxide CMP is a more complex process than metal CMP. In this situation, the slurry is a silica-based slurry using an alkaline aqueous solution like potassium hydroxide or sodium hydroxide. The water weakens the surface layer of the oxide as the hydration reaction breaks the silicon-oxygen bonds, and the silica removes the softer layer by abrasion. Borophosphosilicate glasses polish more quickly than plasma enhanced CVD or thermal oxides. For oxide CMP, the planarization is highly dependent on the hardness of the pad. When polishing oxides, there is no stopping material. This means that there is no easy way of performing endpoint detection.

As we mentioned, planarization can be the result of variable pressure. The pad applies high pressure to elevated regions and leading edges, and lower pressure to depressed and trailing regions. The removal rate at the higher elevations will be a function of the device density and the geometry. For instance, removal rates are high when there are step heights over smaller arrays, smaller gaps and narrow isolated features. However, removal rates are lower for step heights over larger or denser structures adjacent to wide unpatterned field areas like power distribution planes. Removal rates

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are also lower near scribe lines and wafer edges. We show this behavior in several diagrams on the following figure.

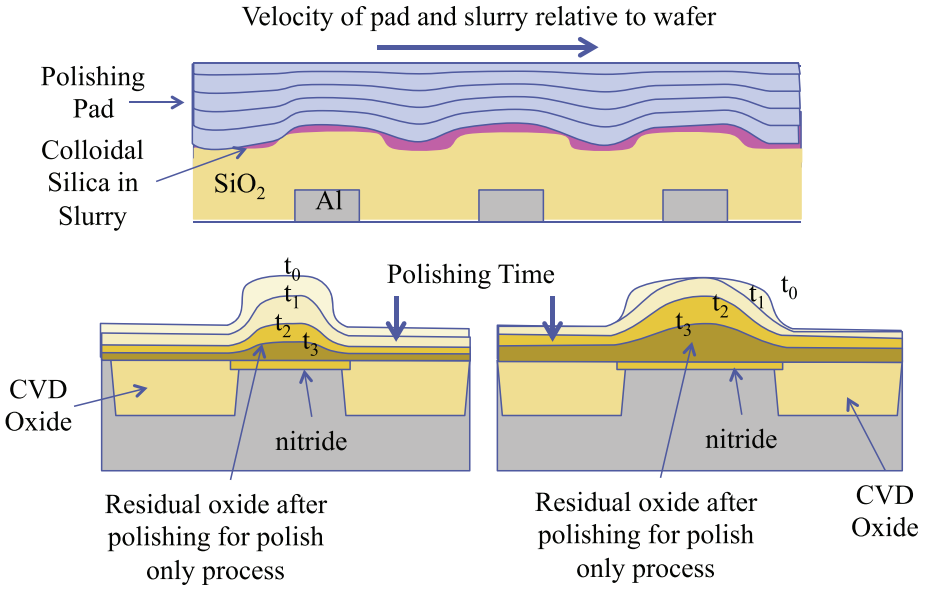


Figure 1. Several diagrams showing how oxide polishing progresses on uneven surfaces.

The top drawing is a depiction of how the leading edge of a feature of an oxide step is eroded by CMP. We show how the edge is pressed against the pad by the combined movements of the carrier and platen. The bottom drawing shows cross-sections of narrow and wide oxide steps being polished by CMP as a function of time. The leading edges are polished rapidly, and since the features continually rotate, all of the edges become the leading edge for about the same length of time. Therefore, narrow features planarize more rapidly than wider ones.

Let's move on and discus low-k dielectrics CMP. We discuss low-k dielectrics themselves nearby on the site, so please review those materials for further information. The CMP process requirements will be specific to the type of dielectric material used. In general low-k materials are quite challenging to planarize properly. They have a high removal rate and low mechanical strength, which leads to difficulties. One solution would be to cap the low-k material with a standard silicon dioxide layer and then stop the CMP process just before reaching the low-k material. This sounds good in theory, but also has its drawbacks, since it requires additional steps.

Process engineers also use CMP to level topography associated with the shallow trench isolation. In order for this to be successful however, one must precisely control the final silicon nitride thickness, since it is used as a stop for the CMP process. Shallow trench isolation CMP is the most critical CMP step for the entire process; it is also the biggest yield-limiting step. The topography left after the CMP operation will affect the overall transistor and circuit performance. Dishing in the shallow trench isolation regions leads to a thin area at the corner of the silicon island. The gate region is thin as a result, locally lowering the threshold voltage and increasing the subthreshold leakages.

Erosion is defined as the loss of the underlying oxide film in metal CMP, and is normally the result of too much over-polish. Dishing is defined as the concave thinning of a metal film, and occurs during the removal and over-polish. It happens because the polishing pad flexes, since it is not perfectly rigid. This

leads to higher polishing pressures in recessed areas and is especially true in the middle of wide exposed regions. There is a strong dependence on pattern density, which makes this problem worse for lower density areas and for large linewidths. The solutions include minimizing the over-polish time to optimize thickness uniformity, removal rate uniformity, and to optimize endpoint detection. If these solutions are not working, then the layout engineers may need to add CMP dummy features to the chips to address pattern density problems. In figure 2 we show the dishing effect in copper metallization. Since the copper is softer, it forms a concave structure in regions where the copper deposition is wide, leading to artifacts in the trenches, like we show in the bottom portion of the graphic. Some additional solutions include using stiffer polishing pads, reducing the down force or pad pressure, moving to an abrasive-free polishing process, switching to electrochemical mechanical polishing, using a non-selective slurry for the tantalum liner film and overpolishing, or moving to linear polishing tools with harder pads that can achieve the same removal rate but at reduced pad pressure.

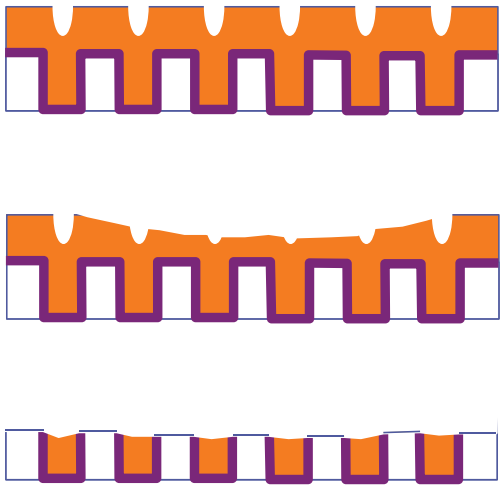


Figure 2. Origin of the dishing effect in CMP (top) polishing pad flexes into trench opening; (middle) formation or concave surface; (bottom) trench area remains “dishes” after CMP.

Let’s briefly discuss non-uniformities. There are two main issues: wafer edge effects and pattern density dependencies. These are both a function of differential pad deformation and pressure. Some possible solutions include improved carrier design and layout structures, and practices to minimize the effects of

pattern dependencies. The data in figure 3 show an example of a well-controlled process where the dishing is limited, except near the edge with a high pattern density.

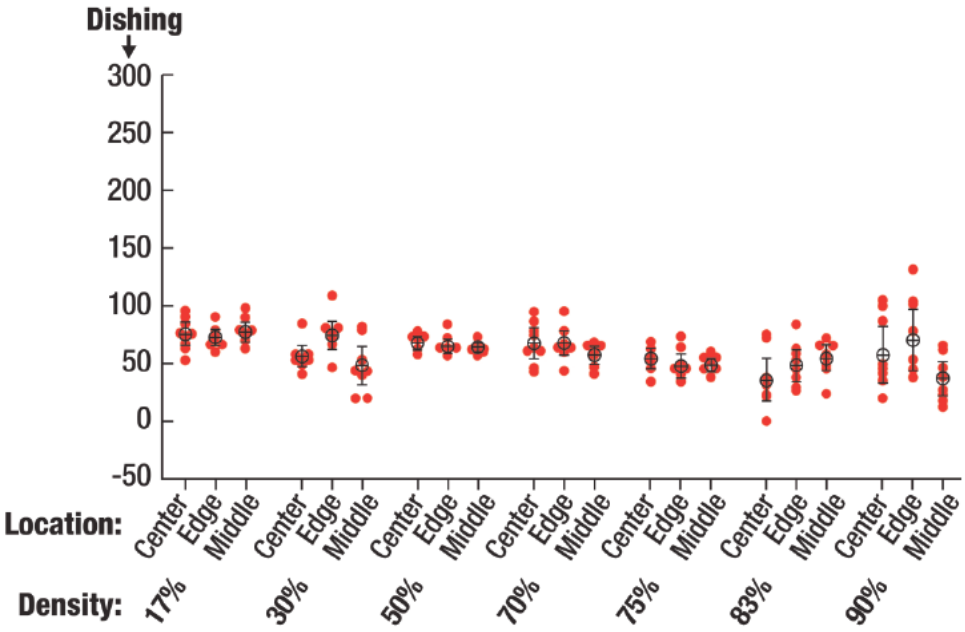


Figure 3. Data showing CMP process control for various pattern densities (courtesy Cabot Microelectronics).

Obviously, given the grinding and polishing, CMP is a very dirty process. This usually occurs in a separate area of the fab that is isolated from the main cleanroom to prevent contamination. Process engineers require further mitigation steps though. One must thoroughly clean the wafers before continuing with the processing since it can lead to cross-contamination in the fab. Metal CMP is of particular concern. Process engineers must remove slurry residues, residues of the polished films, organic residues and alkali metals introduced through the slurry. The goal is to remove all of the contaminants with no surface roughening, no oxidation or corrosion of the metal surfaces, with minimal etching. Process engineers use two key strategies to accomplish this. They keep the wafers wet to reduce adhesion, and they maintain the proper pH to ensure that the zeta potential will not attract particles to the wafer surface.

A typical cleaning cycle would include a buff polish using a soft pad, fast rotation, high-pressure ultrapure water and optional chemicals. This is followed by an initial ultrapure water rinse while wafers are still on the polishing pad. Next, engineers use an ultrapure water spray/overflow rinse immediately after they remove the wafers from the pad while they are still wet. This step typically includes megasonic clean as well. Next, they use a double-sided brush scrub immediately after the spray/overflow rinse. The ultrapure water and chemicals, like ammonium hydroxide and hydrofluoric acid are delivered through the brush itself and the process may include a brush clean to prevent "copper loading." This is followed by a ultrapure water rinse, and a dry cycle using a spin or Marangoni vapor process. Copper CMP is challenging. It does not form strong self-passivation layer, and is prone to corrosion. Process engineers need to remove the copper embedded in the top layer of the oxide without damaging the rest of the thin film.

Next month, we'll discuss process control issues for CMP.

Technical Tidbit

Removing SAC Solder Bumps

Removing Tin-Silver-Copper (SAC) Solder Bumps is a occasionally needed during the failure analysis process. SAC 305 (96.5% tin, 3.0% silver, 0.5% copper) and SAC 405 (95.5% tin, 4.0% silver, 0.5% copper) are common alloys used in lead-free manufacturing.

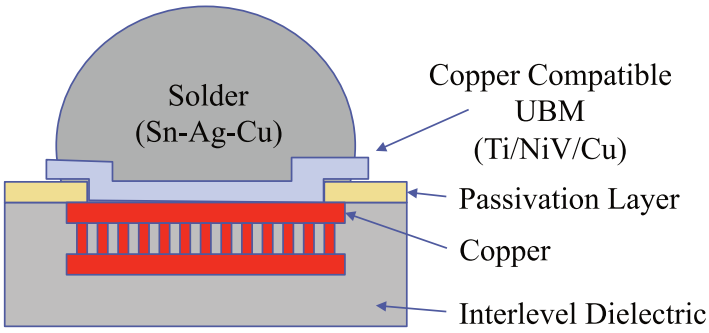


Figure 1. Diagram showing cross section of SAC solder bump and pad structure.

Tin by itself can be etched with a 5:100 ratio of Nitric Acid (HNO_3) and Methanol (CH_3OH), and silver by itself can be etched in a 5:2 ratio of Ammonium Hydroxide (NH_4OH) and Hydrogen Peroxide (H_2O_2). However, we note that tin is the primary constituent in a SAC solder, comprising 95+% of the alloy, and SAC 305 and 405 solders do not develop bulk phases with copper (see Figure 2). Therefore, it is easiest to develop an etch solution based primarily from Nitric Acid and Methanol. Some engineers will add Hydrofluoric Acid (HF) and/or Water (H_2O) in place of the Methanol to help clean the bond pad site. One should not use Hydrogen Peroxide (H_2O_2) in the etch formulation as it will attack the titanium in the Under Bump Metallization (UBM) to some degree. For more details on etching devices with lead-free solder bumps, we encourage the reader to review "Wet Etch Recipe Development for Removing Lead-Free C4 Bumps," [1] which was presented at the 2009 IPFA Conference.

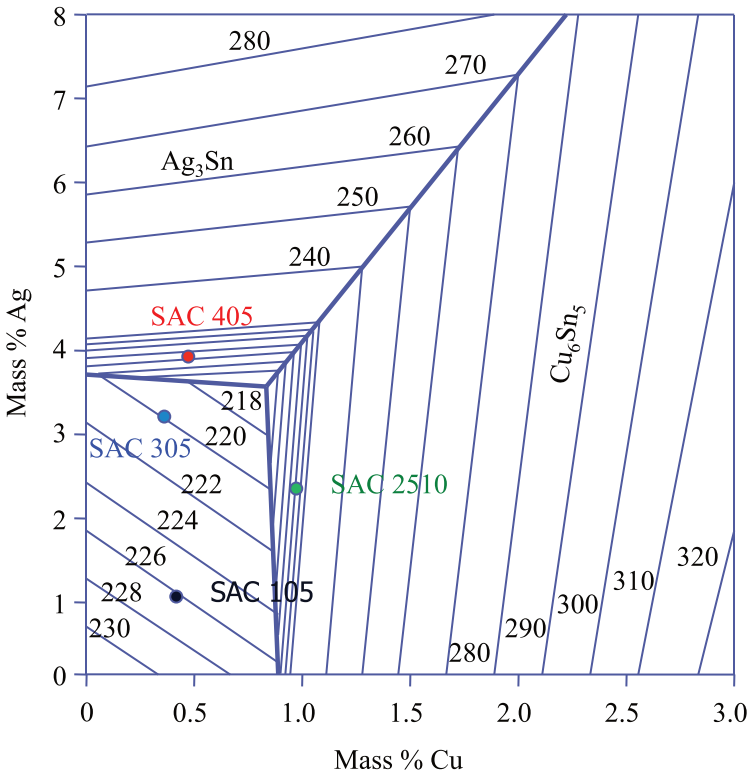


Figure 2. Ternary Phase Diagram for Tin-Silver-Copper

[1] L. Qibin, Z. Xiaole, H. Weidong, and J. Chin, "Wet Etch Recipe Development for Removing Lead-Free C4 Bumps," Proc. 16th Annual Int. Symp. on the Phys. and Fail. Anal. of Integrated Circuits (IPFA), pp. 360-362, 2009

Ask the Experts

Q: Our application has to withstand the following conditions during its lifetime for 15 years:

100,000h @ 20°C
5,000h @ 60°C
100h @100°C

We performed a storage test with this application, running for 500 hours@150°C. How many years (real life) we have simulated with this storage test refer to our real life conditions? (Ea=0,6eV; Tuse=20°C,60°C and 100°C; Tstress=150°C)

A: This simple spreadsheet shows how one might figure this out. We need to determine the acceleration of your application under the 3 different temperature regimes, compared to your stress test. These numbers appear in the column second-to-the-right. They are calculated using the Arrhenius acceleration factor formula. One can then multiply the acceleration factor by the number of hours to get the effective acceleration hours. In this instance, the total use condition environment is equivalent to 137 hours at 150°C using your activation energy of 0.6eV.

	Hours	Temp (C)	Temp (K)			Acceleration Compared to 150C	Effective Acceleration Hours
Use Condition 1	100000	20	293		AF	0.000674897602668	67.49
Use Condition 2	5000	60	333			0.011709486190678	58.55
Use Condition 3	100	100	373			0.110163111408894	11.02
Total Use Conditions							137.05
Stress Test	500	150	423				
Activation Energy	0.6						
k	8.62E-05						

Spotlight: EOS, ESD, and How to Differentiate

OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. Although EOS and ESD damage can at times look quite similar to each other, the source each and the solution can be quite different. Therefore, it is important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a two-day course that offers detailed instruction on EOS, ESD and how to distinguish between them. This course is designed for every manager, engineer, and technician concerned with EOS, ESD, analyzing field returns, determining impact, and developing mitigation techniques.

Participants learn to develop the skills to determine what constitutes a good ESD design, how to recognize devices that can reduce ESD susceptibility, and how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism.** Participants learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.
2. **Overview of the ESD Failure Mechanism.** Participants learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.
3. **ESD Circuit Design Issues.** Participants learn how designers develop circuits to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.
4. **How to Differentiate.** Participants learn how to tell the difference between EOS and ESD. They learn how to simulate damage and interpret pulse widths, amplitudes and polarity.
5. **Resolving EOS/ESD on the Manufacturing Floor.** Participants see a number of common problems and their origins.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. Participants will understand the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. The seminar will identify the major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. Participants will be able to identify basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.

5. Participants will be able to distinguish between EOS and ESD when performing a failure analysis.
6. Participants will be able to estimate a pulse width, pulse amplitude, and determine the polarity of an EOS or ESD event.
7. Participants will see examples of common problems that result in EOS and ESD in the manufacturing environment.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, written text material, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The course notes offer dozens of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

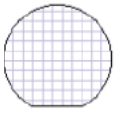
1. Introduction
   a. Terms and Definitions
   b. ESD Fundamentals
   c. EOS Fundamentals
2. Electrical Overstress Device Physics
   a. Sources of EOS
   b. EOS Models
   c. Electrothermal Physics
3. Electrostatic Discharge Device Physics
   a. ESD Models
   b. ESD Testing and Qualification
   c. ESD Failure Criteria
   d. Electrothermal Physics
   e. Electrostatic Discharge Failure Models
   f. Semiconductor Devices and ESD Models
   g. Latchup
4. EOS Issues in Manufacturing
   a. Charging Associated with Equipment
      i. Testers
      ii. Automated Handling Equipment
      iii. Soldering Irons
   b. Charge Board Events
   c. Cable Discharge Events
   d. Ground Loops/Faulty Wiring
   e. Voltage Differentials due to High Current
   f. Event Detection

Day 2

5. ESD Protection Methods
   a. Semiconductor Process Methods
   b. MOSFET Design
   c. Diode Design
   d. Off-Chip Drivers
   e. Receiver Networks
   f. Power Clamps
6. Differentiating Between EOS and ESD
   a. EOS Manifestation
   b. ESD Manifestation
   c. Circuit considerations
      i. Chip level
      ii. System level
   d. Simulating ESD
   e. Simulating EOS
7. EOS/ESD Design and Modeling Tools
   a. Electrothermal Circuit Design
   b. Electrothermal Device Design
   c. ESD CAD Design

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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AMFA2013

Advanced Materials Failure Analysis Workshop

Sunday, August 4

Indiana Convention Center
100 South Capitol
Indianapolis, IN 46225

Chris Henderson of Semitracks will chair the

2013 Advanced Materials Failure Analysis Workshop

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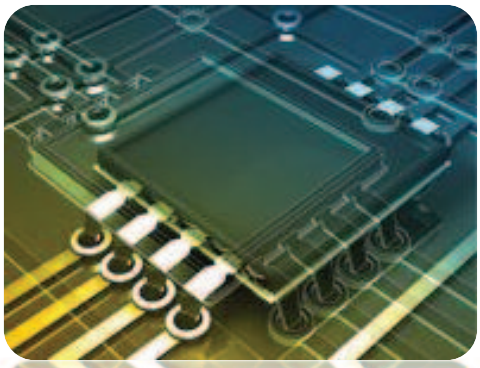

Upcoming Courses

(Click on each item for details)

EOS, ESD and How to Differentiate
September 17 – 18, 2013 (Tue – Wed)
San Jose, California, USA

Wafer Fab Processing
November 7, 2013 (Thur)
San Jose, California, USA

Advanced Thermal Management and Packaging Materials
November 19 – 20, 2013 (Tue – Wed)
Philadelphia, Pennsylvania, USA

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!
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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!