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Resistors

By Christopher Henderson

This month, we will continue our series of Feature Articles by discussing the Composition Resistor and the Film Resistor, which are part of the Fixed Resistor category.

Composition Resistors are also referred to as carbon composition resistors. The construction of a composition resistor is straightforward to understand. One uses machinery to hot press a cylinder of graphite and organic binders. One embeds leads in both ends of the graphite, the resistive material. The component is then covered in a thermoset polymer package and cured to create a solid cylinder-shaped component. These devices are not precise, and engineers typically use them in circuits where lower precision is acceptable. A composition resistor typically is only accurate to about 10% of its intended resistance value.

The image in Figure 1 shows an example of a typical composition resistor. The colored bands indicate the resistance value of the component. For more information on how to interpret the color bands, the reader should access IEC Standard 60062. There is also information on this topic at a number of websites, including Wikipedia. Most components contain four bands to list the first and second significant digits, the multiplier, and the tolerance. This component is a military component and has 5 bands; the fifth band indicates the failure rate. This particular component is a 1 MΩ resistor (red—which represents a "two" for the first significant bit; brown—

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which represents a "one" for the second significant bit; blue—which represents the "six" for the 10^6 multiplier; gold—which represents a 5% tolerance; and yellow—which represents a 0.001% failure rate).

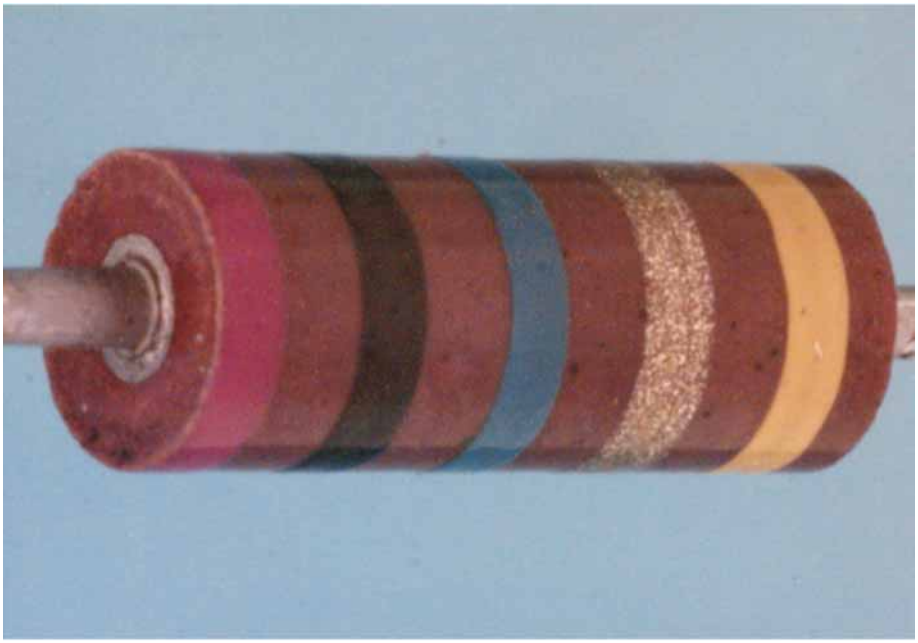


Figure 1. Overall exterior view of a typical composition resistor.

The image in Figure 2 shows a cross-sectional view of a typical composition resistor. We can see the hot-pressed carbon element, the lead-to-element interface, and the thermoset compound encasing the element and the ends of the leads.

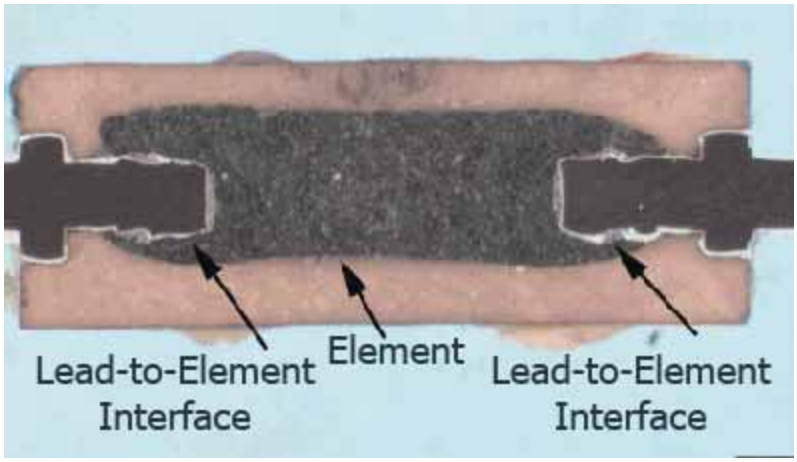


Figure 2. Cross-section view of a typical composition resistor.

Some typical failure modes for composition resistors include resistance increase due to moisture; electrical overstress damage; and mechanical damage. Moisture can lead to an increase in resistance. Moisture will penetrate through the thermoset, much like it does with a plastic encapsulated microcircuit. The moisture penetrates into the carbon element, causing swelling of the binders, leading to a change in

the volume percentage of the carbon and a higher resistance. Baking most composition resistors will return the resistance back to normal. One can improve the humidity resistance through the use of coatings on the resistor component, or a conformal coating on the board. Electrical overstress is a common failure mode, and is often accompanied by signs of charring, cracking or burning at the exterior. Finally, mechanical damage can manifest itself as damage to the body of the resistor (a cracked package), or cracking at the interface between the leads and the resistive element.

Next, we will discuss the Film Resistor. The film resistor consists of a thin film of metal, carbon, or metal oxide on a ceramic rod or tube. It uses metal end caps with wire leads that are either pressed or crimped on the ends of the rod or tube. Sometimes the end caps might be soldered to the rod or tube. The manufacturer then uses an abrasive, or a laser system to trim the metal film to give it the correct resistance value. The manufacturer then coats the tube, film and caps conformally with a polymer or epoxy. The materials are typically not hermetic, so moisture and contamination can work their way in. Some manufacturers may encase the resistor in a hermetically-sealed glass shell.

The image in Figure 3 shows an example of the construction of a thin film resistor. In this image, we removed the exterior coating. One can see the wires, end caps, rod, metal-film resistive element, and the trim kerf. In this resistor, the trim kerf creates a helical pattern. The wires are welded to the end caps in this resistor, as well.

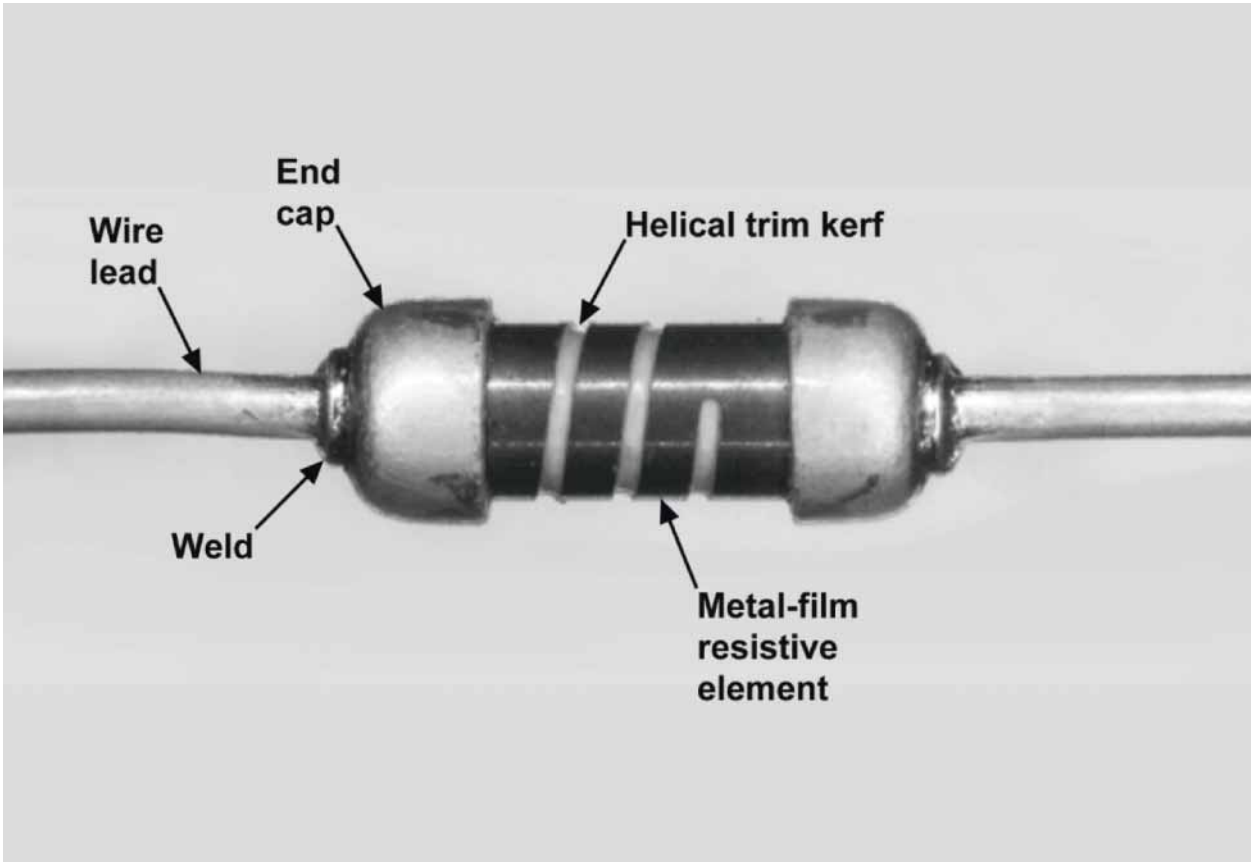
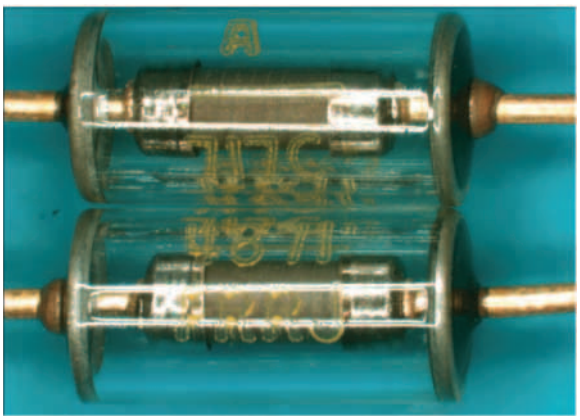
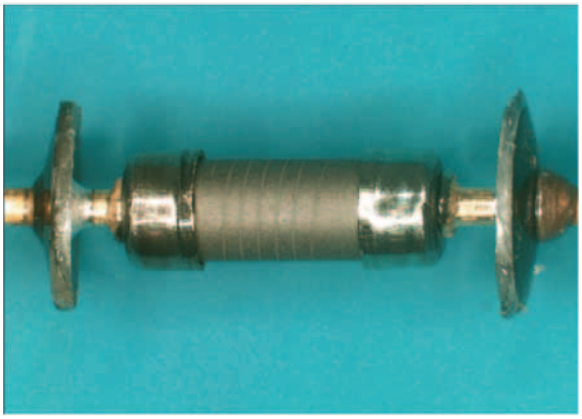


Figure 3. Construction of a Thin Film Resistor.

The images in Figures 4 (a) and (b) show examples of hermetically sealed thin film resistors. These resistors use a nickel-chromium, or nichrome alloy as the resistor element. The manufacturer seals the resistors using a glass envelope. Figure 4 (a) shows the envelopes of the two resistors intact, and Figure 4 (b) shows a resistor with the glass envelope removed. One can also see the spiral trim cut on the nichrome film.



(a)



(b)

Figures 4. (a) Overall view of a hermetic nichrome thin film resistor and (b) View of device after glass envelope was removed.

Film resistors suffer from several common failure mechanisms, including several in the mechanical damage category, such as: damage to the package; damage to the resistive film substrate; and damage to the resistive film. Other failure mechanisms include a cracked resistive film; corrosion of the resistive film, or the interface between the end cap and the film; intrusion of the coating material between the end cap and the film; and electrical overstress.

In next month's Feature Article, we will go into more detail on the Chip Resistor.

Technical Tidbit

HARA and ASILs

This month's technical tidbit covers two automotive safety concepts, Hazard Analysis and Risk Assessment, or HARA, and Automotive Safety Integrity Levels, or ASILs.

An area of increased activity in the semiconductor industry is automotive IC development. The adoption of hybrid electric vehicles, electric vehicles, and an increased emphasis on safety is driving the development efforts to be much more formal than the semiconductor industry previously did with standard commercial electronics. An important standard associated with this IC development is ISO-26262. For chip designers, a key aspect of ISO-26262 is a Hazard Analysis and Risk Assessment, or HARA. HARA evaluates the risk associated with an integrated circuit per hazard identified, based on the severity of the hazard, the exposure of the hazard (in other words, the probability of occurrence), and the controllability by the driver to mitigate the hazard. These criteria, known as S for Severity, E for Exposure, and C for Controllability, drive what are known as Automotive Safety Integrity Levels, or ASILs. ASILs are based on S, E, and C to show the degree of risk reduction needed from the design. The engineering team then sets safety goals to achieve the necessary risk reduction, which is an inherited ASIL attribute.

Severity Class	Probability Class	Controllability Class		
		C1	C2	C3
S1	E1	QM	QM	QM
	E2	QM	QM	QM
	E3	QM	QM	A
	E4	QM	A	B
S2	E1	QM	QM	QM
	E2	QM	QM	A
	E3	QM	A	B
	E4	A	B	C
S3	E1	QM	QM	A
	E2	QM	A	B
	E3	A	B	C
	E4	B	C	D

This table from the ISO-26262 standard describes the ASIL levels: A, B, C, and D, based on three levels of S, four levels of E, and three levels of C. The table lists five methods of risk reduction: QM, and ASIL A, B, C, and D.

The definitions are listed below.

QM: Quality managed risk reduction is adequate

ASIL A: Low level of risk reduction required for functional safety

ASIL B: Moderate level of risk reduction required for functional safety

ASIL C: High level of risk reduction required for functional safety

ASIL D: Highest level of risk reduction required for functional safety

These concepts are driving the development of many systems within the automobile today, including braking systems, adaptive cruise control, lane assist features, all the way up to automated driver assistance systems, like we now see in state-of-the-art automobiles. To learn more about ISO-26262 and ASILs, contact us at Semitracks, and we can recommend courses, webinars, or online training options for you.

Ask the Experts

Q: I am having trouble understanding the concept of "Force" and "Sense" for ATE measurements. Specifically, my understanding is that we use the "Force" line to apply a voltage to the DUT from the ATE, and, then the "Sense" line to get a good idea how much of the voltage applied at the ATE actually reached the DUT on the Force line. This is so that we can calibrate the tester accordingly and apply a little higher voltage at the ATE side, for example. The problem I see with both the bad and the good Kelvin connection is that the Sense line is also a trace and has some resistance, so the voltage reported back to the ATE on the Sense line is not reflective of the voltage that made it to the DUT on the Force line to begin with. Could you please explain how this would work? Could it be the Sense line is zero impedance as opposed to 50 ohms? or, do we have a set length for Sense lines?

A: You're correct that the Sense lines also have some resistance, but we would make the measurement using very low currents (like you would with a voltage measurement—which is basically what you're doing here), so therefore, the impact on the reading will be very minor. Basically, the measurement device would have extremely high impedance, so the effect of the Sense lines would be minimal.

Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

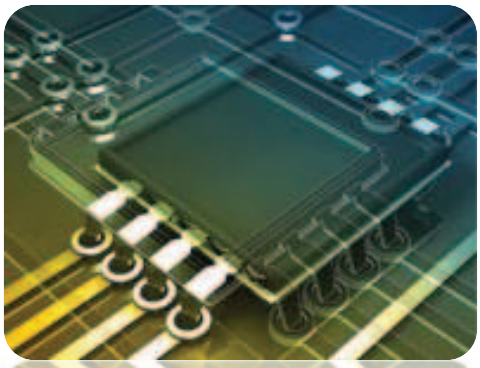
1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills
   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless

   f. Thermal Interface Materials (TIMs) and Lids
   g. Fine Pitch Warpage Reduction
   h. Stacked Die and Stacked Packages
   i. Material Selection for Board Level Temperature Cycling and Drop Reliability
4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Webinars

(Click on each item for details)

Failure and Yield Analysis

WEBINAR—4 sessions of 4 hours each
Europe: February 1 – 4, 2021 (Mon – Thur), 1:00 P.M. – 5:00 P.M. CET
US: February 1 – 4, 2021 (Mon – Thur), 9:00 A.M. – 1:00 P.M. PST

Semiconductor Reliability / Product Qualification

WEBINAR—4 sessions of 4 hours each
Europe: February 8 – 11, 2021 (Mon – Thur), 1:00 P.M. – 5:00 P.M. CET
US: February 8 – 11, 2021 (Mon – Thur), 9:00 A.M. – 1:00 P.M. PST

Wafer Fab Processing

WEBINAR—4 sessions of 4 hours each
Europe: April 6 – 9, 2021 (Tue – Fri), 1:00 P.M. – 5:00 P.M. CET
US: April 19 – 22 (Mon – Thur), 9:00 A.M. – 1:00 P.M. PST

IC Packaging Technology

WEBINAR—4 sessions of 4 hours each
Europe: April 19 – 22, 2021 (Mon – Thur), 1:00 P.M. – 5:00 P.M. CET
US: April 12 – 15, 2021 (Mon – Thur), 9:00 A.M. – 1:00 P.M. PST

Advanced CMOS/FinFET Fabrication

WEBINAR—4 sessions of 2 hours each
Europe: April 26 – 29, 2021 (Mon – Thur), 3:00 P.M. – 5:00 P.M. CET
US: April 5 – 8, 2021 (Mon – Thur), 9:00 A.M. – 11:00 A.M. PST