

InfoTracks

Semitracks Monthly Newsletter



Applications Overview Part 1

By Christopher Henderson

In this document, we begin to cover some of the applications for optoelectronics circuits.

We cover the outline for this section here. In Part 1 we will briefly discuss CCD image detectors, photomultipliers, x-ray detectors, and plasmonic devices. In Part 2 we will briefly discuss quantum dot devices, terahertz applications, and optical MEMS devices.

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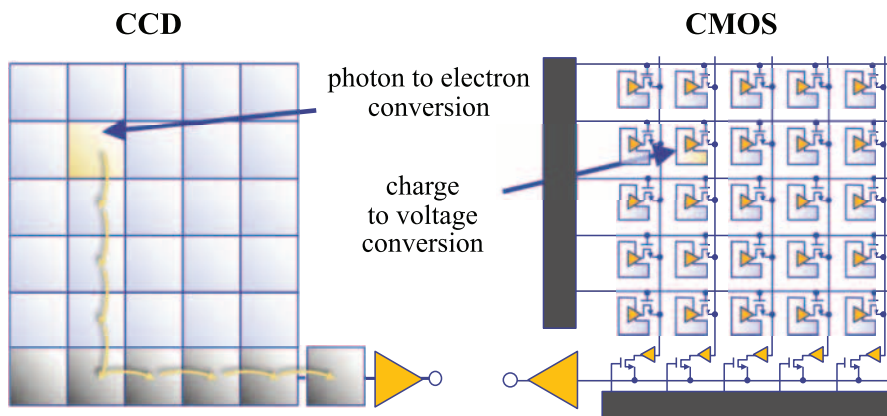


Figure 1. Illustration of image plane detectors.

We begin with image plane detectors. The most common image plane detector is the Charge Coupled Device. The Charge Coupled Device, or CCD, converts photons into electrons. The image plane



detector then uses a secondary circuit implemented in CMOS to convert the charge to voltage, like we show in the diagram in Figure 1.

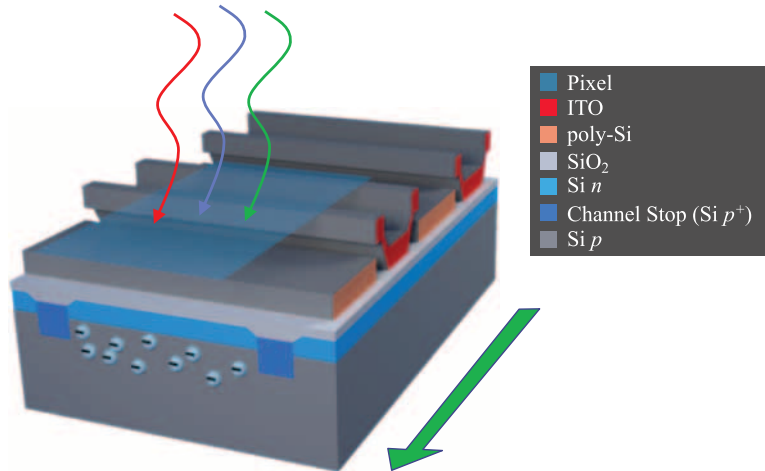


Figure 2. Image of CCD cross section.

We show a CCD cross-section image here in Figure 2. The rectangular region on top of the diagram represents the pixel area. The structure is built on a p-type silicon substrate, with channel stop p-plus implants surrounding the pixel. There is a region of n-type silicon near the surface that forms a pn junction below the surface. Above that, there is a layer of silicon dioxide, covered with polysilicon lines. In between the polysilicon lines are regions of indium tin oxide, which is a transparent conducting oxide material.

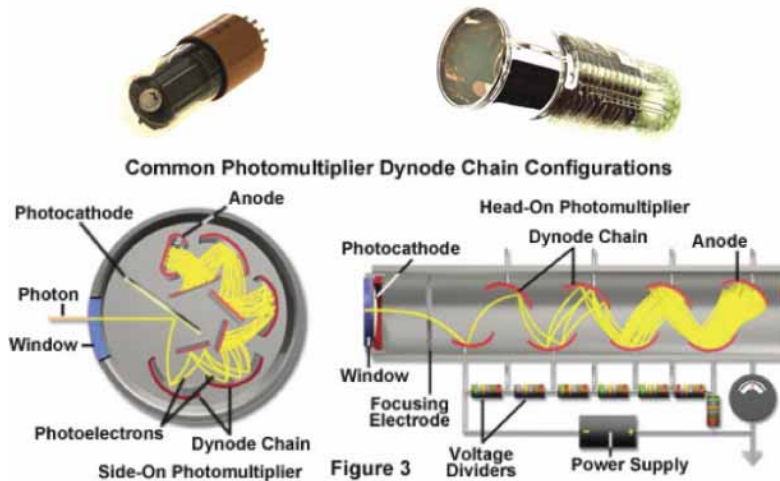


Figure 3. Cross-section images of photomultiplier tube.

Another important application is the photomultiplier tube, or PMT. We show two cross-section images of the PMT here in Figure 3. The one on the left is a cross-section view through the width of the tube, and the one on the right is a cross-section view through the length of the tube. The photocathode is at the left

end of the tube, and the anode is at the right end of the tube. The curved red plates in between represent the dynode chain that are separated by voltage dividers. The focusing electrode focuses the incoming photons toward the dynode chain, where the photomultiplication takes place. At the end of the tube, the number of photons is much greater than the incoming number.

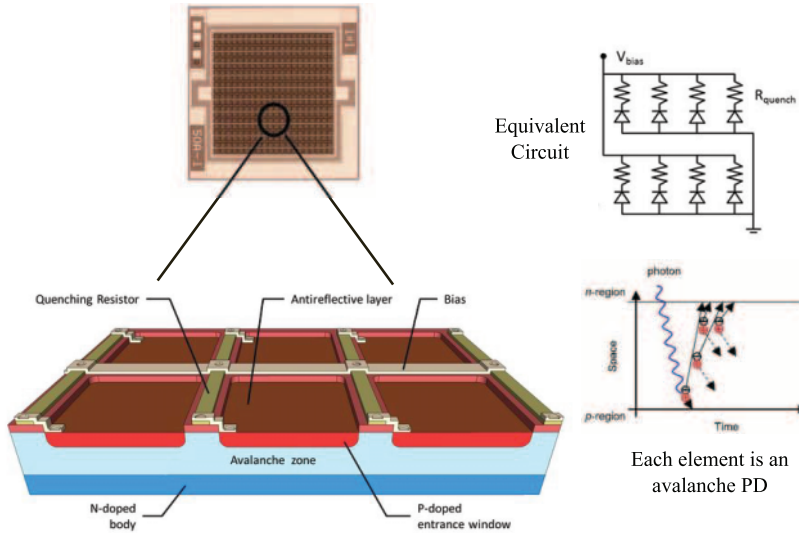


Figure 4. Diagram of Si PhotoMultiplier (SiPM).

We show a diagram of the photomultiplier element here in Figure 4. The silicon photomultiplier structure contains a n-type substrate, with p-type entrance regions above. There is an anti-reflective layer on top of the entrance windows, and a quenching resistor structure hooked to each of the cells to limit damage from avalanche breakdown. There is also a horizontal conducting layer to bias the cells. We show the equivalent circuit at the upper right, and the behavior of the structure at the lower right.

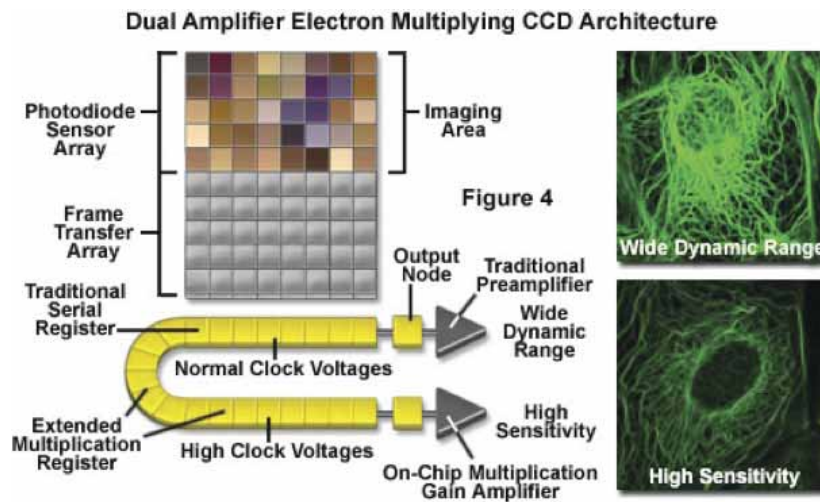


Figure 5. Illustration of electron multiplier CCD architecture.

Here in Figure 5 we show the architecture for an electron multiplier CCD. The CCD contains a photodiode sensor array, which constitutes the imaging area. Below that lies the frame transfer array, which shifts the information into either a traditional serial register, or an extended multiplication register. The serial register provides a wide dynamic range, and the multiplication register provides higher sensitivity.

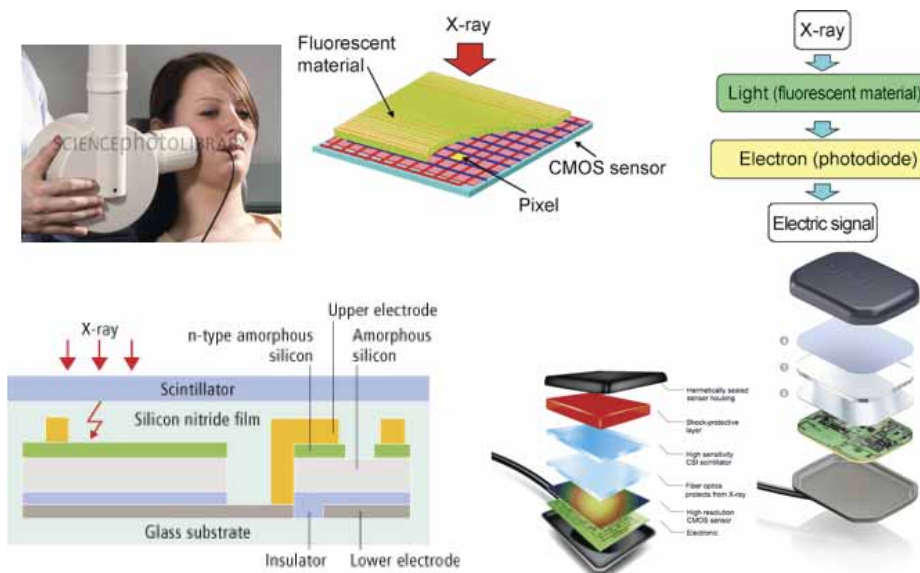


Figure 6. Illustration of x-ray detectors.

Another important application is the x-ray detector. An x-ray excites a fluorescent material, creating light that impacts a CMOS sensor array. These devices contain a layer of amorphous silicon in between a lower electrode and insulator, and an upper electrode.

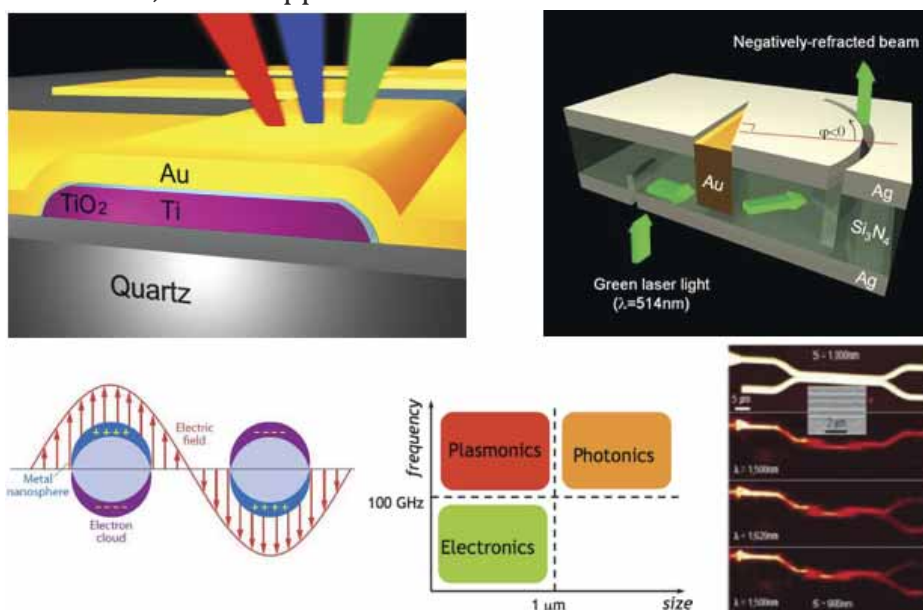


Figure 7. Illustration of plasmonics.

Next, let's move on and discuss plasmonics. Plasmonics takes advantage of the coupling of light to charges like electrons in metals, and allows breaking the diffraction limit for the localization of light into subwavelength dimensions enabling strong field enhancements. We show some example diagrams of plasmonic devices here in Figure 7.

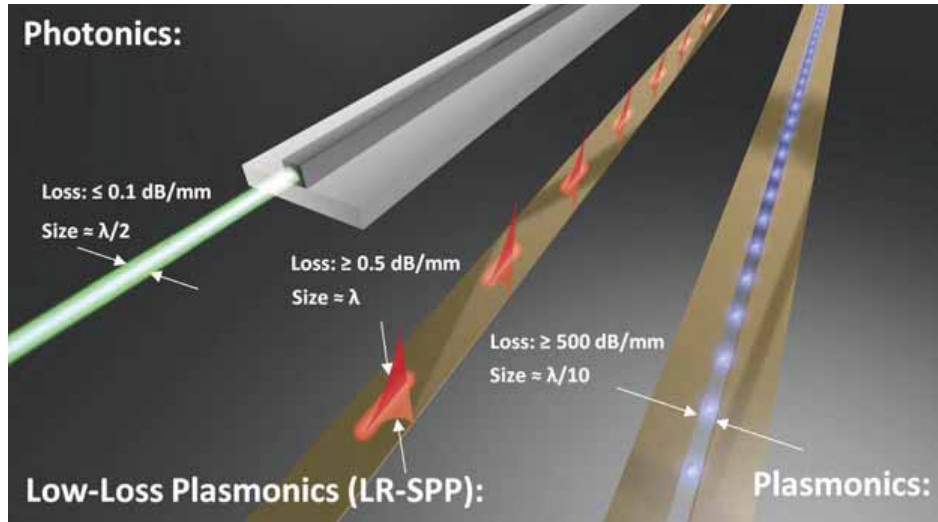


Figure 8. Comparison of plasmonics to photonics.

Figure 8 helps to illustrate some of the main differences between photonics and plasmonics. With photonics transmission the loss is quite low, on the order of less than 0.1 decibels per millimeter, but the wavelength is limited to one-half the wavelength of the light being used. In a plasmonic transmission system, the loss is considerable, on the order of 500 decibels per millimeter or higher, but the wavelengths can be much shorter, on the order of one-tenth the wavelength of the light. For low-loss plasmonics, the loss is approximately one-half a decibel per millimeter, and the wavelength is approximately the wavelength of the light.

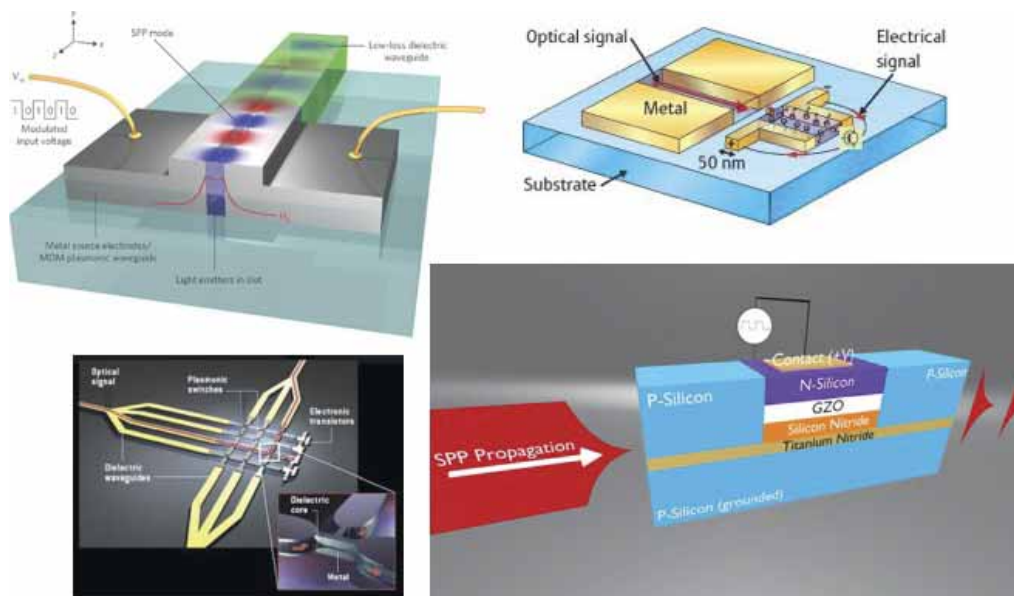


Figure 9. Examples of plasmonic devices.

Here in Figure 9 are several examples of plasmonic devices. The figure in the upper left shows a metal-dielectric-metal, or MDM, plasmonic waveguide. It enables a Strong SP Polariton, or SPP, Mode to achieve sub-wavelength localization. The figure at the upper right is a surface plasmon detector which convert optical signals in electric. In this device, the two nanopieces in an L form with a germanium layer and generate an electrical current. Other plasmonic structures can have an equivalent electronic circuit if they receive light in a determinate wavelength. This 100 nm length gold nanorod behaves like a RLC circuit. The image at the lower left is an example of a plasmonic switching array. An optical signal from the left propagates down dielectric waveguides to a metal-dielectric core structure that enables switching of the light, based on electrical signals from the transistors on the right. The figure at the lower right shows a compact plasmonic modulator, integrated with plasmonic strip waveguides. The modulator consists of a TiN strip, which carries the SPPs, a silicon nitride insulating layer, a gallium-doped zinc oxide (GZO) dynamic layer, silicon claddings, and a biasing contact. When a voltage is applied between the silicon substrate and the upper contact, the optical properties of the GZO film are changed, modulating the SPP wave. The TiN, silicon nitride, and GZO layers are all 10nm thick.

To be continued in next month's Newsletter...

Technical Tidbit

Electrostatic Chucks

This technical tidbit covers electrostatic chucks.

The electrostatic chuck (ESC) is used in a variety of semiconductor processes to hold the wafer during processing. ESCs employ a platen with integral electrodes which are biased with high voltage to establish an electrostatic holding force between the platen and wafer, thereby “chucking” the wafer. ESCs can be made from materials such as aluminum oxide, aluminum nitride and sapphire. They should have high purity, exhibit a high plasma durability, good chucking and de-chucking responses, and be useful for both low and high temperature applications.

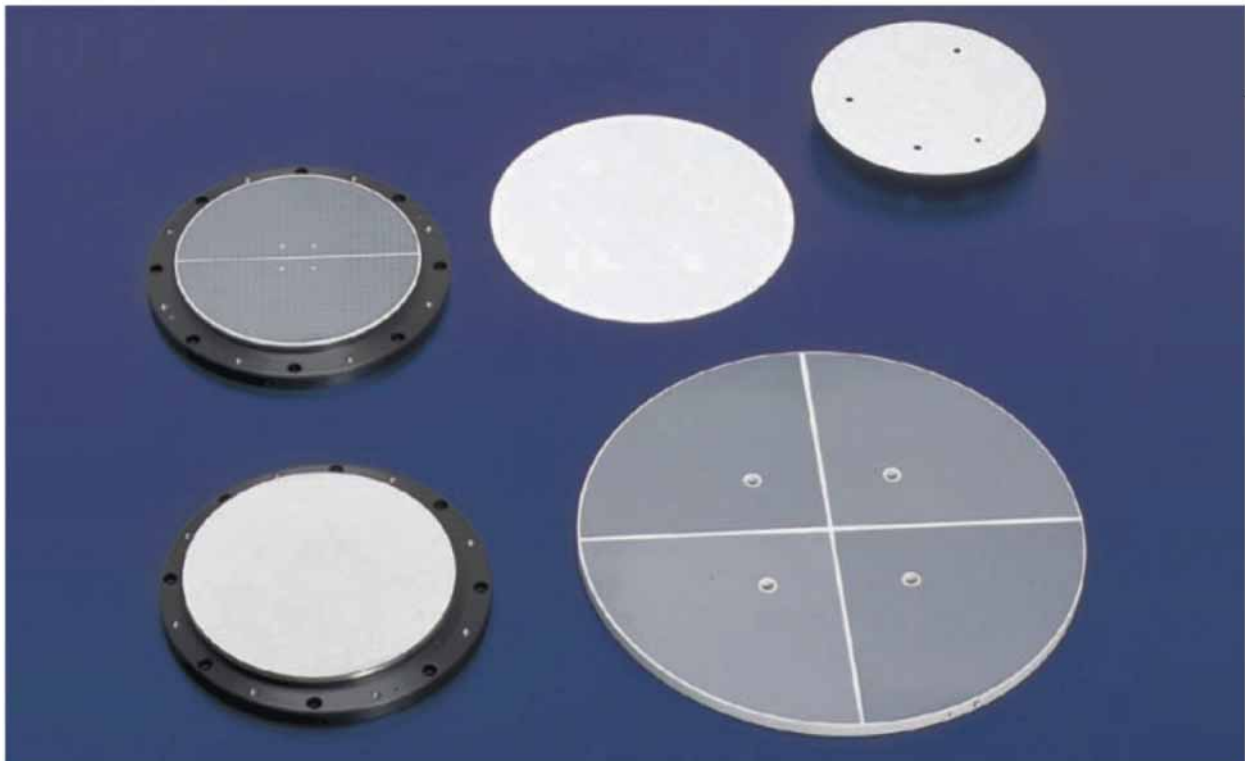


Figure 1.

The mechanical, thermal and vacuum-technical demands influence the choice of material for the chuck. Generally, a high bending stiffness D is essential. The bending stiffness is sensitive with respect to the material thickness h , the modulus of elasticity E and the Poisson's ratio like we show in the equation here.

$$D = E \cdot h^3 / 12(1 - \nu^2)$$

The thermal behavior of the assembly is determined by the CTE of the material. Special materials with low thermal expansion are necessary to achieve stability within a range of a few nanometers. Two glasses that have been demonstrated to work well are ULE by CORNING and the glass ceramic family ZERODUR by SCHOTT. Both materials have a thermal expansion in the range of $1-2 \times 10^{-8}$ per degree Kelvin and an excellent stability in high vacuum atmosphere, most notably, low out-gassing. The type of the dielectric material is essential for chucking. With a Coulomb dielectric, a nearly perfect isolation exists. The

clamping force is constant in time. The behavior of a so-called Johnsen-Rahbek dielectric is totally different because the dielectric is virtually "semiconducting." Charge enters the dielectric material and builds an electric double layer close to the substrate interface. This leads to clamping forces up to 5 to 10 times higher than with Coulomb systems. However, the clamping force is time-dependent. The substrate may adhere some hours after switching off the power.

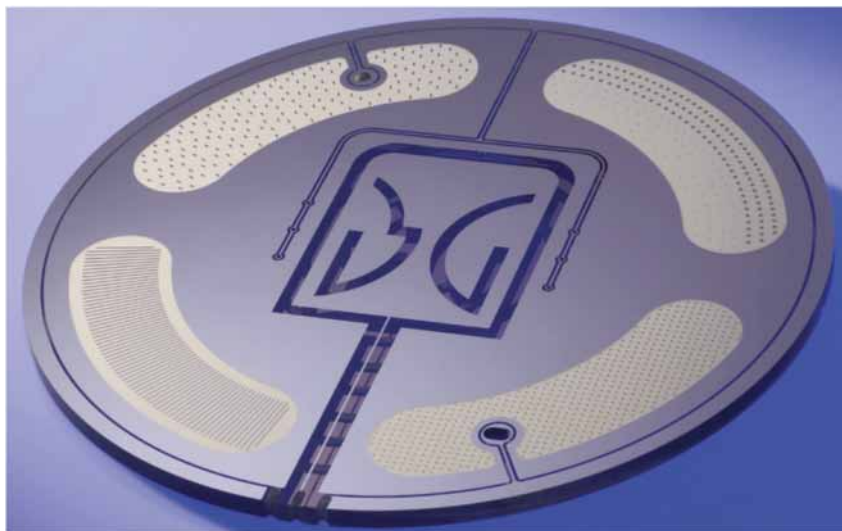


Figure 2.

A power supply system should allow for the optimization of the electrostatic force profile needed to provide effective ESC operation for each wafer/platen application. Effective electrostatic chuck operation should address issues of minimum clamping time, variation in clamping force during the wafer processing, as well as wafer charging control to minimize wafer "sticking" to the platen, and potentially other factors.



Figure 3.

For example, Trek models utilize arbitrary waveform generator (AWG) technology using easy-to-use software to allow various waveforms to be created and evaluated by the user. When the AWG is coupled to an HV amplifier, one obtains superior ESC driver performance. To illustrate the utility of this technology, a useful waveform for the application is shown in the lower right in Figure 4. The waveform has an intentional overshoot to pull the wafer in firmly and an oscillatory tail intended to minimize any residual charge that might otherwise remain on the wafer after the process is complete.

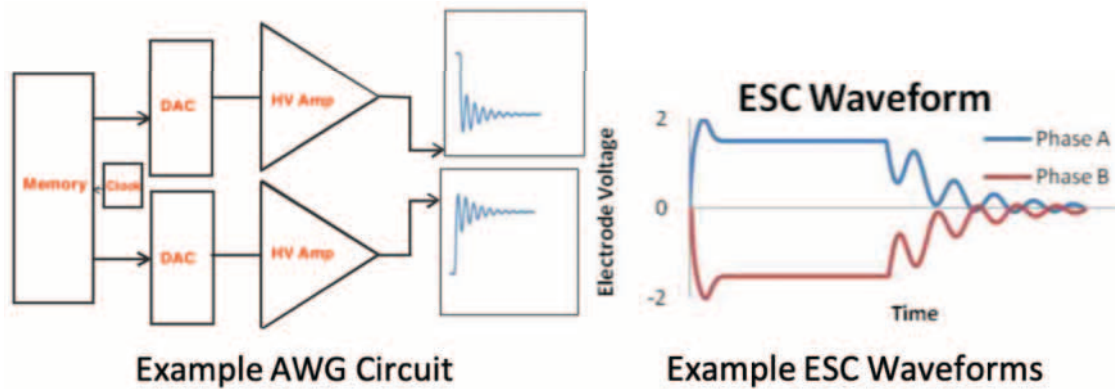


Figure 4.



Ask the Experts

Q: Why use gases other than HCl for the Cl precursor gas in the oxidation process?

A: In the past it was common practice to feed HCl gas to the oxidation furnace. Although this gas was effective for this application, its use has several drawbacks. Because of its corrosive nature, this gas deteriorates the metal distribution lines as well as the metal components in the gas management system. Such corrosion phenomena result in highly undesirable metallic contamination of the gases. Moreover the handling of the pressurized gas cylinders requires special care.

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Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

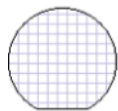
COURSE OUTLINE

1. The Package Development Process as a Package Technology:
 - a. Materials and Process Co-Design
2. Molded Package Technologies:
 - a. Die Attach
 - i. Plasma Cleans
 - b. Wire Bonding
 - i. Au vs. Cu vs. Ag
 - ii. Die Design for Wire Bonding
 - c. Lead Frames
 - d. Transfer and Liquid Molding
 - i. Flash
 - ii. Incomplete Fill
 - iii. Wire Sweep
 - iv. Green Materials
 - e. Pre- vs. Post-Mold Plating
 - f. Trim Form
 - g. Saw Singulation
 - h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
 - a. Wafer Bumping Processing
 - i. Cu and Solder Plating
 - ii. Cu Pillar Processing
 - b. Die Design for Wafer Bumping
 - c. Flip Chip Joining
 - d. Underfills

- e. Substrate Technologies
 - i. Surface Finish Trade-Offs
 - ii. Core, Build-up, and Coreless
 - f. Thermal Interface Materials (TIMs) and Lids
 - g. Fine Pitch Warpage Reduction
 - h. Stacked Die and Stacked Packages
 - i. Material Selection for Board Level Temperature Cycling and Drop Reliability
- 4. Wafer Chip Scale Packages:
 - a. Redistribution Layer Processing
 - b. Packing and Handling
 - c. Underfill vs. No-Underfill
 - 5. Fan-Out Wafer Level Packages:
 - a. Chip First vs. Chip Last Technologies
 - b. Redistribution Layer Processing
 - c. Through Mold Vias
 - 6. Through Silicon Via Technologies:
 - a. Current Examples
 - b. Fundamental TSV Process Steps
 - i. TSV Etching
 - ii. Cu Deep Via Plating
 - iii. Temporary Carrier Attach
 - iv. Wafer Thinning
 - c. Die Stacking and Reflow
 - d. Underfills
 - e. Interposer Technologies: Silicon, Glass, Organic
 - 7. Surface Mount Technologies:
 - a. PCB Types
 - b. Solder Pastes
 - c. Solder Stencils
 - d. Solder Reflow

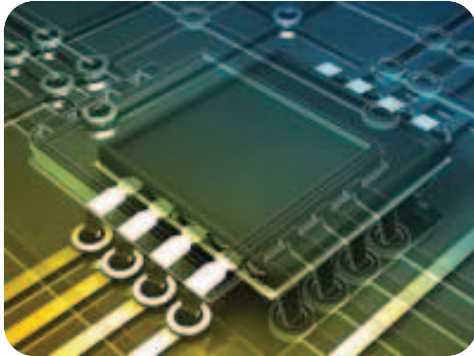
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Upcoming Courses

(Click on each item for details)

Introduction to Processing

March 2 - 3, 2020 (Mon - Tue)
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Failure and Yield Analysis

March 2 - 5, 2020 (Mon - Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication

March 4, 2020 (Wed)
Portland, Oregon, USA

IC Packaging Technology

March 5 - 6, 2020 (Thur - Fri)
Portland, Oregon, USA

Semiconductor Reliability / Product Qualification

March 9 - 12, 2020 (Mon - Thur)
Portland, Oregon, USA

Wafer Fab Processing

April 14 - 17, 2020 (Tue - Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification

April 14 - 17, 2020 (Tue - Fri)
Munich, Germany

Failure and Yield Analysis

April 20 - 23, 2020 (Mon - Thur)
Munich, Germany

IC Packaging Technology

April 27 - 28, 2020 (Mon - Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication

April 30, 2020 (Thur)
Munich, Germany