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Test Structures—Basics Part 1

By Christopher Henderson

In this document we will provide an overview of test structures as they pertain to reliability. Test structures can provide critical insight into the reliability of a semiconductor process. The advantage of using test structures is that one can evaluate a specific part of the process without having to design a complex integrated circuit. One can also provide feedback quickly, since many test structures can be realized without a full fabrication flow.

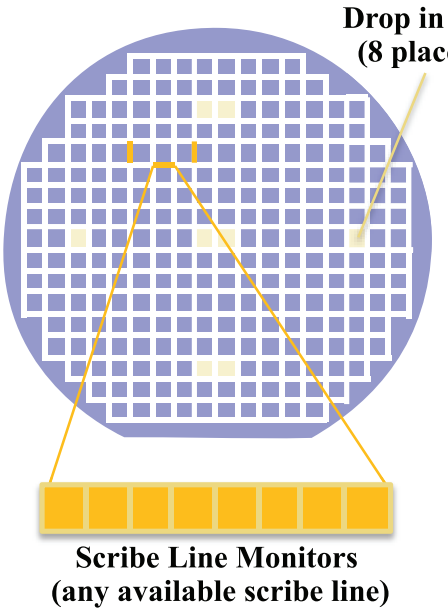

Figure 1. Location of test structures on a die.

Part 1 covers transistor level standard test structures. These are test structures that are used by process engineers to evaluate various aspects of the wafer fabrication process. When measured, stressed and then re-measured, some of these structures can provide data as to the reliability of a process.

In this Issue:

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There are several generic issues related to test structures. They relate to the design of the structures. First, where should the test structures be placed? There are two options if one intends to integrate test structures with product dice. The first option is to place the test structures in the streets, or in the area around the product die. Normally, there is an area around the die that is several hundred microns wide to accommodate the wafer dicing process. Test structures can be placed in this region and tested before the sawing operation. The benefit is that the test structures do not consume additional silicon real estate, allowing the manufacturer to maximize the amount of silicon that can be sold. However, there are some limitations to this approach. The narrow channel means that one cannot implement complex or large-area test structures. Still, in high volume production, most manufacturers prefer this approach. The second option is to dedicate a reticle field or part of a reticle field to test structures. This allows more structures and is particularly useful when developing or qualifying a technology. From a reliability standpoint, this approach also provides more flexibility to obtain the appropriate data. Second, how should one connect to the test structures? The preferred method, especially for reliability testing, is through probes or bondwires. This requires some spacing. The industry typically uses a fixed probe pad size and a common pitch and layout array for these types of structures. The most common is to use a 2 by 10 array of pads that are equidistant from one another. Third, what type of test structures should I design? In an ideal world, the set of test structures should be able to catch and characterize any and all wafer fab defects. However, in the real world, this is not the case. One cannot know all of the potential defects and problems beforehand. Therefore, the goal is to monitor for as many problems as possible. Usually, this requires a process to evaluate the effectiveness of the existing test structures, and incorporate additions and changes to the next set of structures. This requires that the manufacturer maintain corporate knowledge as to the types of defects that occur. It also requires a close interaction with the failure analysis lab. Most process engineers utilize a technology characterization vehicle or an easy-to-characterize design such as a Static Random Access Memory, or SRAM, in conjunction with test structures to obtain better coverage of potential problems.

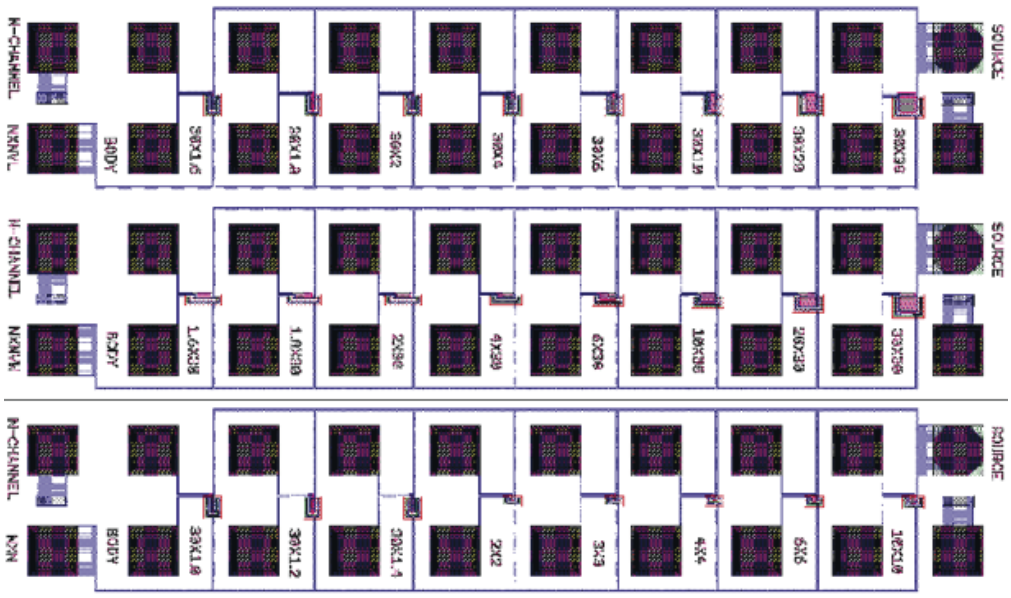


Figure 2. Test structures: N-channel transistors.

Let's begin with some basic test structures. The individual transistor can be used to characterize gate oxide leakage, negative bias temperature instability, and hot carrier effects. The transistors shown here in Figure 1 are designed as fixed width/variable length transistors, fixed length/variable width transistors, and W/L=1 transistors.

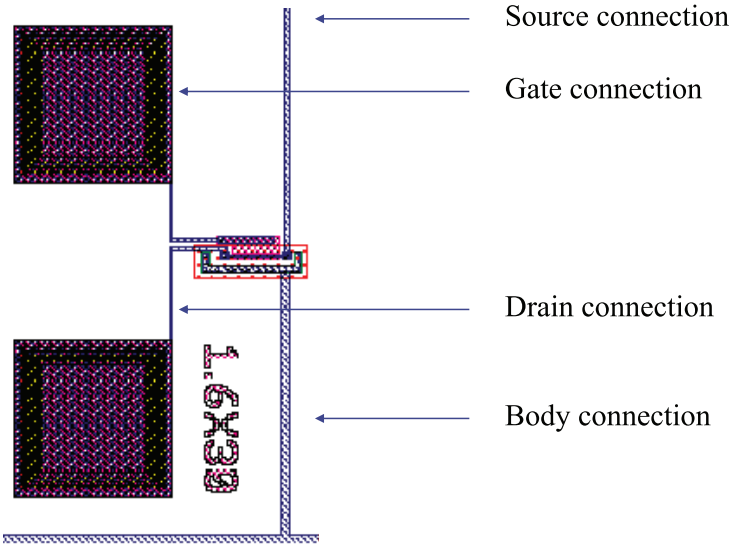


Figure 3. Close-up of N-channel transistor.

Figure 2 is a close up view of the layout of the transistor. These devices use a common body connection and a common source connection. The gates and the drains can be controlled independently.

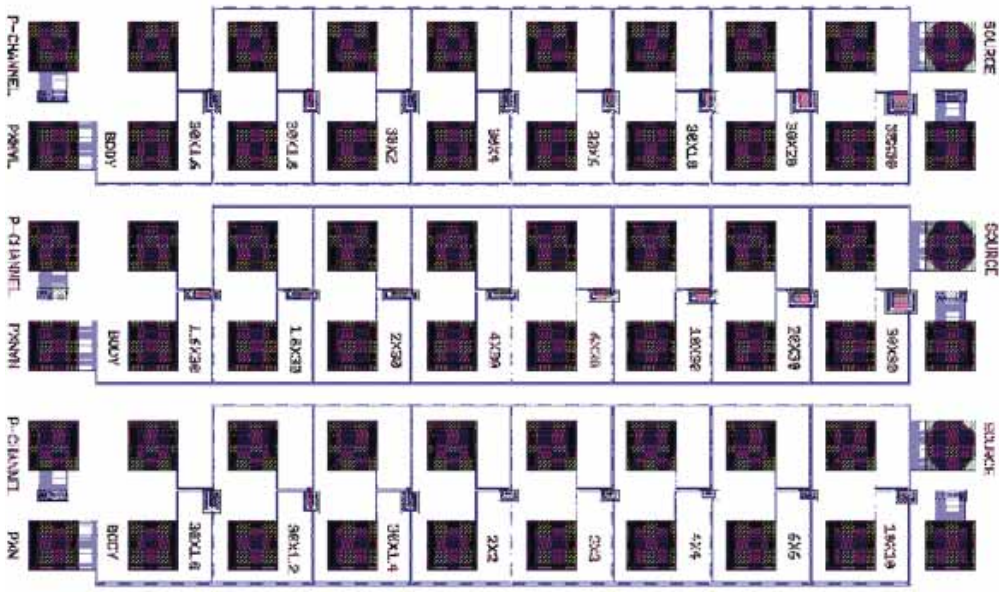
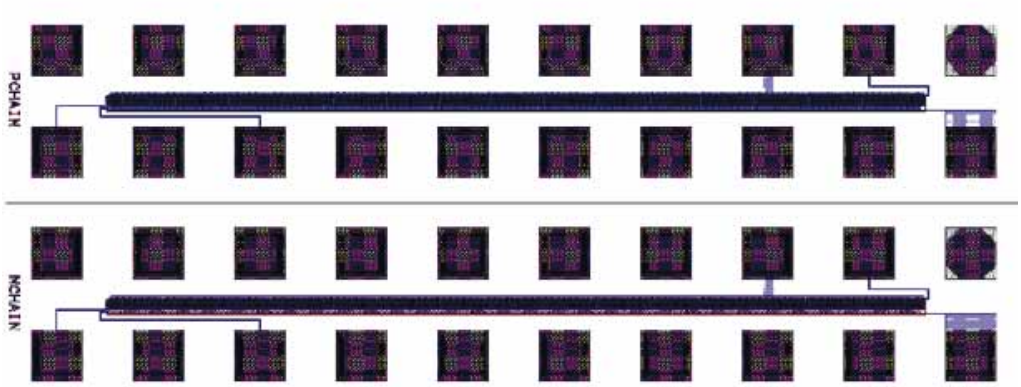


Figure 4. Test structures: P-channel transistors.

These transistors in Figure 3 have the same dimensions as those in the previous two figures, except these transistors are p-channel transistors. Both types are needed to look for processing problems that might affect one type of transistor, but not the other.



-Figure 5. Series of P-channel (top) and N-channel (bottom) transistors.

In addition to single transistors, it can be useful to look at a series of transistors. For instance, one might want to look for subtle degradation in the channel resistance. Using a series of transistors can help to magnify this effect. Figure 5 shows a line of p-channel transistors in series, and a line of n-channel transistors in series.

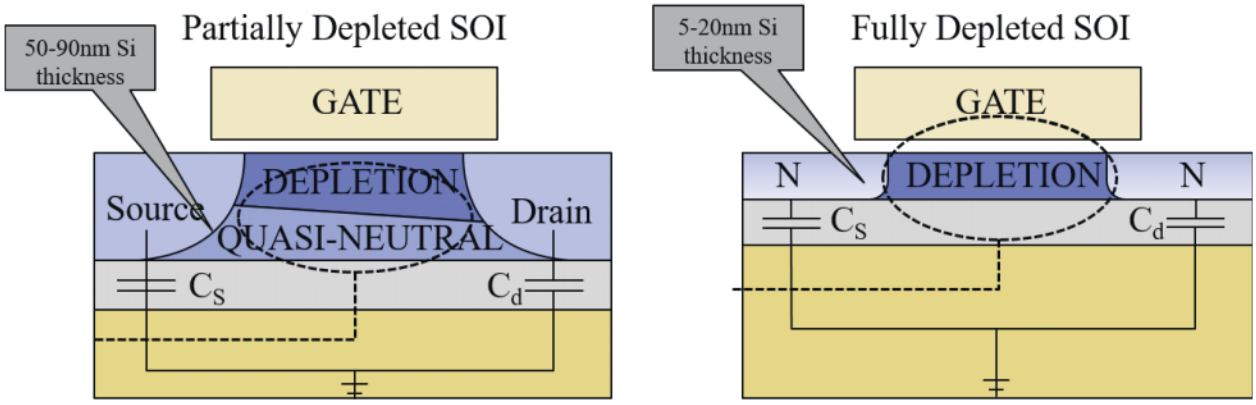
[To be continued in Semitracks' February 2019 Newsletter.]

Technical Tidbit

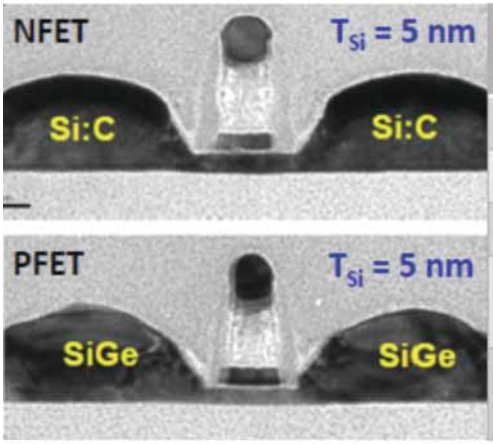
Fully-Depleted Silicon On Insulator

This month's technical tidbit covers Fully-Depleted Silicon On Insulator, or FD-SOI.

Although much of the excitement in modern integrated circuits revolves around the FinFET, there is an alternate technology which provides improved transistor performance - Silicon On Insulator, or SOI. There are two types of Silicon on Insulator technologies: partially-depleted SOI, and fully-depleted SOI. The figure on the left below shows an example of partially-depleted SOI, and the figure on the right shows an example of fully-depleted SOI. Partially-depleted SOI uses a thicker channel, so the gate cannot fully deplete the channel beneath it. Fully-depleted SOI uses a very thin channel, such that the gate can fully deplete the channel under normal operating voltages. Fully-depleted SOI, or FD-SOI, provides excellent electrostatic control of the channel, and no channel doping is necessary. One can also provide back bias to the transistor if the buried oxide layer is thin. FD-SOI also provides excellent threshold voltage control, low drain-induced barrier lowering, improved short channel effects, good subthreshold slope, and minimum junction capacitance and diode leakage. FD-SOI is also a simpler process than required for FinFET manufacturing. There are no halo implants needed to stop punch-through, and a simpler Shallow Trench Isolation (STI) process.

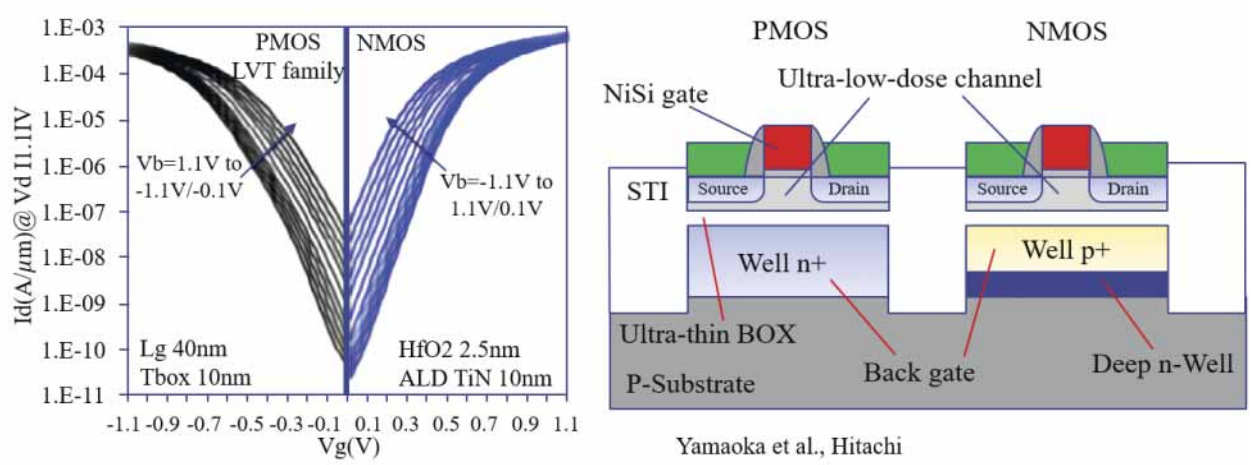


The image on the left below shows a transmission electron microscope cross-section view of n-channel and p-channel MOSFETs formed using FD-SOI. The table on the right shows comparison values between 20nm FD-SOI and 22nm bulk FinFET technologies. Notice that the parameters are quite similar. The main drawback to SOI is cost of the substrate. The wafers can be 3 to 5 times more expensive than traditional wafer substrates.



	20nm FD-SOI	22nm FinFET
L_G (nm)	22	>25
Pitch (nm)	80-100	100
I_{OFF} (nA/um)	1	1
NFET I_{ON} (uA/um)	920	960
PFET I_{ON} (uA/um)	880	850

One can also take advantage of the thin buried oxide layer to provide back bias to FD-SOI transistors. The backgate bias can modulate both the NMOS and PMOS threshold voltages at values approaching 80 mV/V, like we show below in the graph on the left. This is not an option with FinFETs; however, the FinFET does have a better subthreshold slope. The figure on the right shows how one might integrate the FD-SOI technology to control the back bias.



Yamaoka et al., Hitachi

Ask the Experts

Q: What chemical(s) might be used to prevent die attach bleed out?

A: The best way to answer to this question is to discuss the causes of die attach bleedout. The causes include:

- Excess adhesive present on the surface, possibly due to lack of automation or incorrect thickness of the layer.
- Viscosity of the compound selected, and the curing conditions. In general, faster-curing systems will work better.
- Surface contaminants can have an adverse impact, which could lead to bleed out. As such, plasma cleaning can be used to remove any contamination.

Spotlight: CMOS, BiCMOS, and Bipolar Process Integration

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's mixed-signal chips perform a wide range of applications unheard of a few years ago, including wireless applications, high speed communications, and signal processing. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. A corollary to Moore's Law is that frequencies on mixed-signal devices continue to rise. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS, BiCMOS, and Bipolar Process Integration*** is a 3-day course that offers detailed instruction on the physics behind the operation of a modern mixed-signal integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving too heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why BiCMOS devices dominate the mixed-signal industry today.
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS, Bipolar and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.

4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, emitter islands, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
2. Basic Semiconductor Concepts
   a. Diffusion/Drift
   b. PN Junction Diodes
   c. Bipolar Junction Transistor
   d. MOS Transistor
   e. Additional Concepts
      i. Avalanche Breakdown
      ii. Zener Breakdown
      iii. Tunneling
      iv. Schottky Barriers
3. General Scaling Issues
   a. Constant Field Scaling/Constant Voltage Scaling
   b. Process Integration Issues
      i. Transistors (Ion vs Ioff, Mobility Enhancement, short channel effects, etc.)
      ii. Interconnect (RC delay, power dissipation, etc.)
   c. Limitations to Scaling

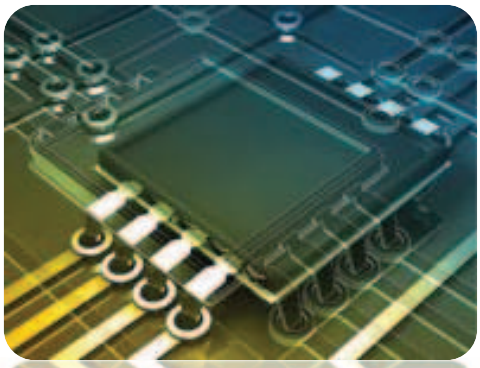
Day 2

4. Conventional CMOS
   a. Well/Substrate Engineering
   b. Device Isolation
   c. Gate Stack
   d. Contacts/Silicide
   e. Scaling Issues
   f. Basic CMOS Flow Presentation
5. Conventional BiCMOS
   a. Bipolar Transistor Fundamentals
   b. BiCMOS Process Overview
   c. Scaling and Limitations
   d. Basic BiCMOS Flow Presentation
6. Bipolar Enhancement Techniques
   a. SiGe
   b. SiGe:C
7. Power Technologies
   a. LDMOS
   b. DECMOS
   c. BCD
8. Additional Analog Circuit Elements
   a. Resistors
   b. Capacitors
   c. JFETs

Day 3

9. Interconnects
   a. Aluminum Interconnects, Issues
   b. Copper Interconnects, Issues
   c. Low-k Dielectrics
10. CMOS/Bipolar/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In

11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors
12. Conclusion/Wrap Up



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

CMOS, BiCMOS and Bipolar Process Integration
February 18 – 20, 2019 (Mon – Wed)
Singapore

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA