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InfoTracks

Semitracks Monthly Newsletter

Fault Diagnosis Algorithms Part 2

By Christopher Henderson

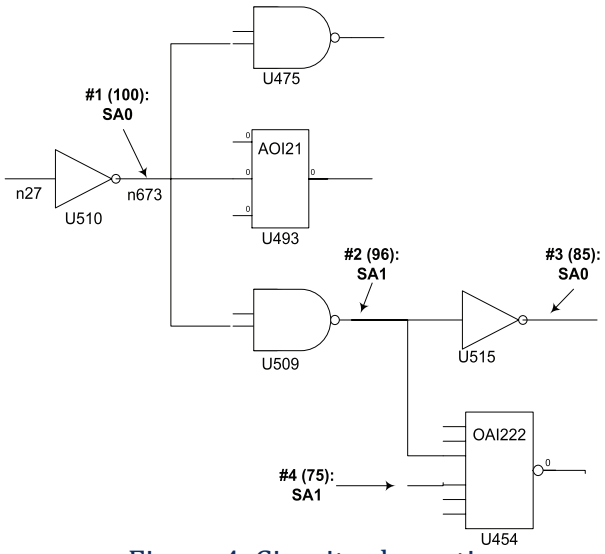

Figure 4. Circuit schematic.

This is an example of a circuit schematic. The gates are identified using their unique symbols, which makes it easier for the designer to understand data flow and logical behavior. In order to view a circuit schematic one must use the design software to generate the view, or use an interchange file format such as the Electronic Data Interchange Format (EDIF) to pass the appropriate information to a viewer.

Schematic navigation can be performed manually by examining printed schematics, or from the design software. In the design

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software, additional functions are available that allow the user to go forward and backward through the circuitry. This can be quite useful for following a fault propagation path. It doesn't give an indication of relative distances on the IC though. There might be a relatively large distance between two gates because of routing and compaction issues, but the gates appear close together on the schematic.

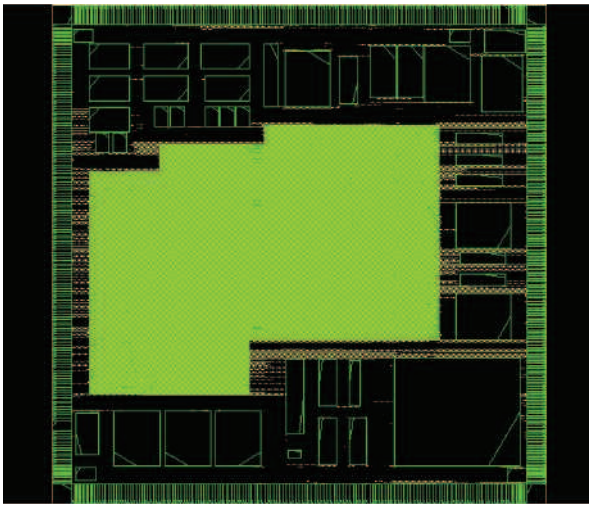


Figure 5. Circuit artwork.

This is a screen shot showing the circuit artwork on an IC. Because today's ICs are complex, it can take a long time for the computer to draw the polygons on the screen. The GDSII files that contain the polygon information can occupy gigabytes of space. In order to improve drawing speed, it usually makes sense to turn off all but just a few layers in the software. Another method is to just display the bounding boxes for the cells, like we show here. Since this is a physical representation, the circuits at the location of a defect can be identified.

Layout navigation is performed using routing or floorplanning software tools in the design software suite. There are also stand-alone artwork viewers that can be used for this purpose. With the appropriate linkage between the design and the layout, one can input a cell name or wire name and the software will highlight the object for the user. This can be useful for determining the location of a feature on the IC. It is also useful for evaluating the physical properties of faults. When a group of faults is clustered in a small area, this means that it is usually easier to find the defect. When the faults are spread around the IC widely, this usually means that it will be difficult to isolate the defect.

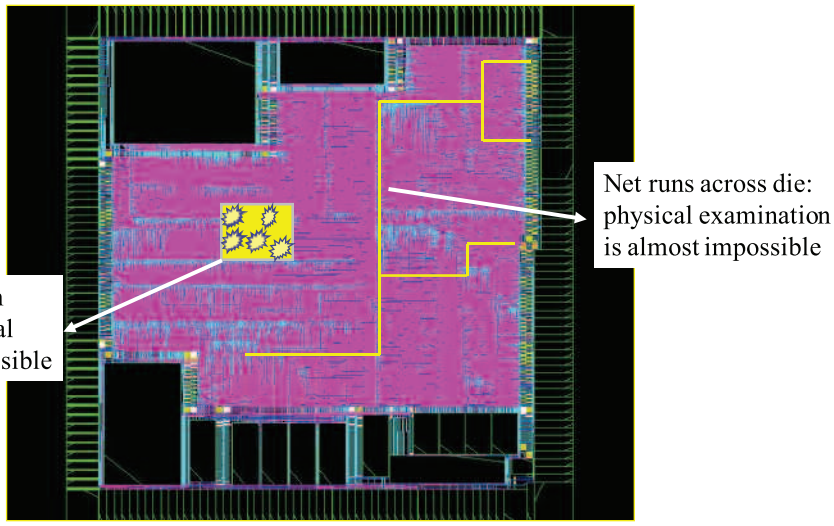


Figure 6. Fault proximity.

Fault proximity is important for quickly localizing defects on ICs. If the faults discovered through the diagnosis process are close to one another physically as shown here in Figure 6, then it becomes much easier to deprocess the IC and examine the area for defects. When the fault or faults discovered through the diagnosis process are associated with nodes that run across large areas of the die, then physical examination is almost impossible. There is simply too much area to examine on the IC in this case.

Fault diagnostic output needs to be evaluated to make sure it is worth bypassing other fault localization techniques and moving straight to the physical characterization step. A diagnosis needs to have one or a small number of high scoring candidates in order to be a good diagnosis. If there are low scoring candidates that can indicate that multiple defects are present, that there is an unmodeled or complex behavior, or that the algorithm is inappropriate for the defect type. If the candidates are low-scoring, then it makes sense to try a different algorithm or to look for more failures, either on the die or on other dice with related or similar failures.

The good news is that many diagnostic runs will implicate a single stuck-at fault. This is a good sign, but equivalent faults can make the actual localization more difficult. Many types of defects can mimic a stuck-at fault without being a short to VDD or VSS. An open circuit is a good example of this. Also, a fault at a particular node can give the same results as a fault on an adjacent node or a nearby node. Be sure to consider this possibility when trying to isolate the problem.

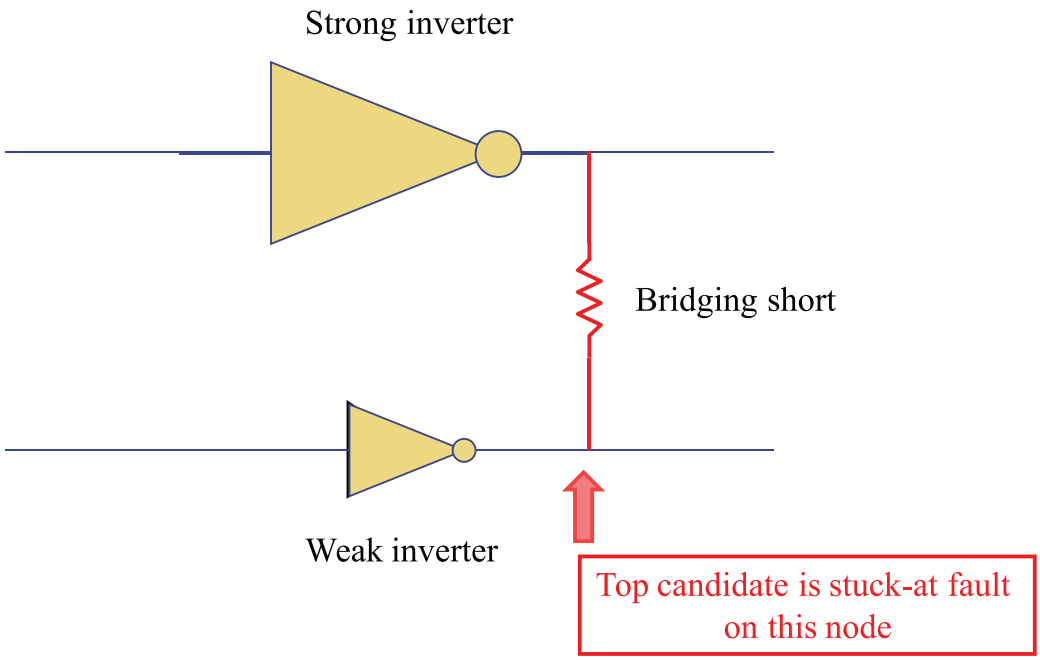


Figure 7. Dominance bridging fault.

When running diagnostic algorithms, one must also be aware of dominance when it comes to bridging faults. A gate with larger transistors will dominate the behavior of a gate with smaller transistors when the two are shorted together. That means that the stuck-at fault will most likely show up on the net associated with the weak inverter because the stronger inverter will overpower the weak one.

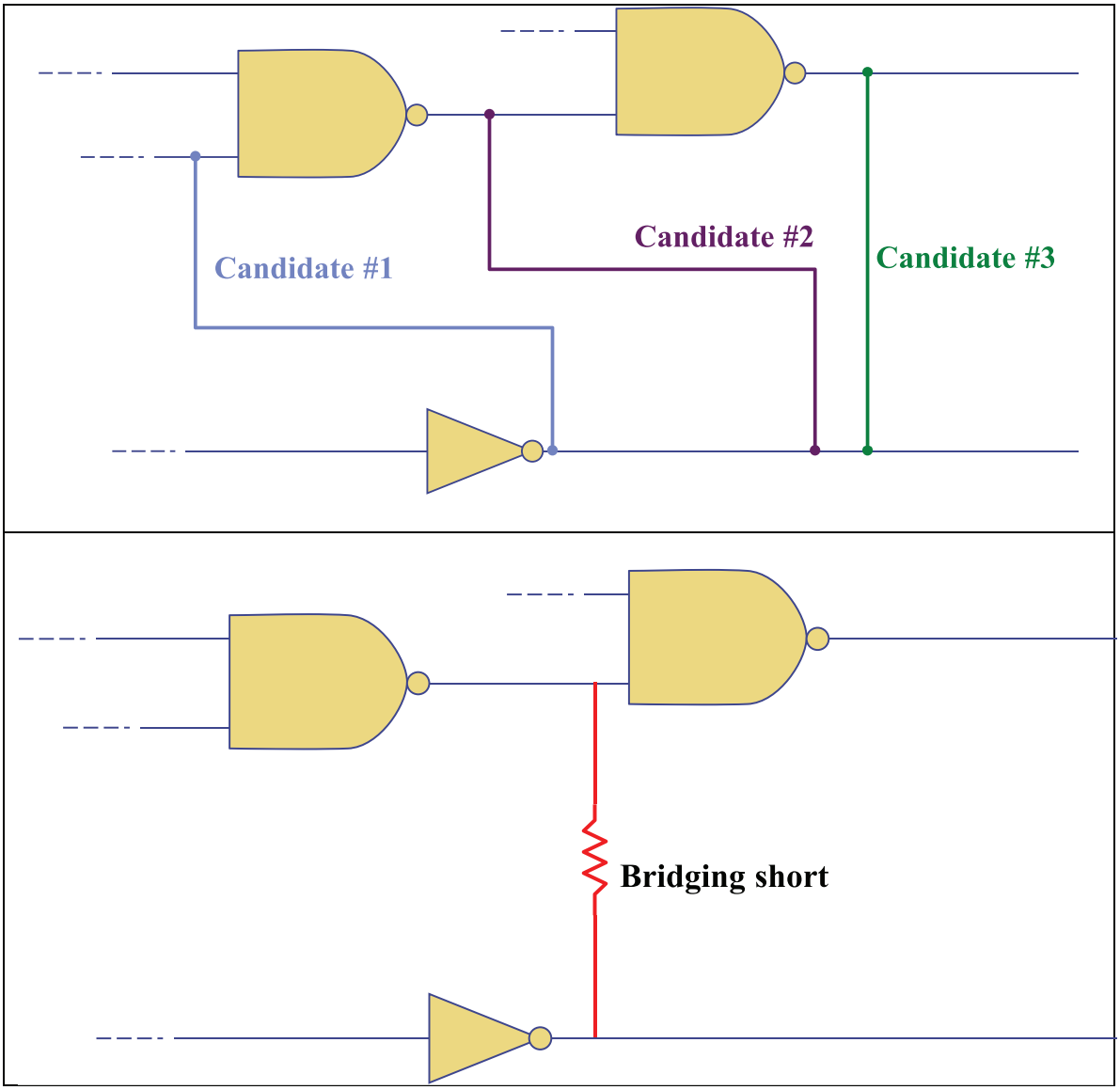


Figure 8. Candidate #2 is best.

Here is an example where we need to be concerned with equivalent faults. Let's assume we have three candidate bridging faults (Figure 8, top). In this case, all three faults are equivalent to one another as far as what will be detected on the output. In general, it is best to pick the middle fault, as it has the highest probability of corresponding to the actual bridging short (Figure 8, bottom).

Resources
Figures 4, 5 and 6
After Lavo

Technical Tidbit

ANOVA Part II

In last month's Technical Tidbit, we introduced ANOVA. To review it, please go to last month's newsletter on our website. This month, we'll continue with our discussion and cover two-factor ANOVA. In last month's ANOVA data, we assumed a single factor, or that our batches were identical. Now let's assume that the batches are actually wafers from different suppliers we intend to use. In order to account for this additional variable, we perform a two-factor ANOVA without replication. We do it without replication since there is just one value we're examining, the yield. This table shows the results. Again, notice that our F ratios are less than the F-crit values, so the implication is that the manufacturing methods are statistically the same. Also, notice that the p-value for the rows is much greater than 0.05. It is important though, not to read too much into this.

1. The p-value is not the probability that the null hypothesis is true, or the probability that the alternative hypothesis is false.
2. The p-value is not the probability that the observed effects were produced by random chance alone.
3. The 0.05 significance level is merely a convention.
4. The p-value does not indicate the size or importance of the observed effect.
5. In the absence of other evidence, the information provided by a p-value is limited.

Anova: Two-Factor Without Replication

SUMMARY	*Count*	*Sum*	*Average*	*Variance*
Batch 1	4	381.2	95.3	6.54
Batch 2	4	365.8	91.45	20.75
Batch 3	4	368	92	6.12666667
Batch 4	4	371.4	92.85	7.41666667
Batch 5	4	365.3	91.325	10.8558333
A	5	454	90.8	7.83
B	5	463.3	92.66	11.493
C	5	477.4	95.48	3.622
D	5	457	91.4	10.26

ANOVA

Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Rows	42.638	4	10.6595	1.41839835	0.28670237	3.25916673
Columns	64.8855	3	21.6285	2.87798008	0.08015854	3.49029482
Error	90.182	12	7.51516667			
Total	197.7055	19				

We refer to an experimental design with two sets of factors as a two-way design. For example, let's say we have a chemical vapor deposition design of experiments we wish to perform. We use different gas combinations and temperatures for the DOE. We then would like to evaluate the significance of the factors using the F distribution. This type of analysis can help us evaluate the effects of changing the variables, and interactions that might occur between the variables.

A factor is an independent variable. A k factor ANOVA addresses k factors. In Two Factor ANOVA without Replication there is only one sample item for each combination of factor A levels and factor B levels. In Two Factor ANOVA with Replication there is more than one sample item for each combination of factor A levels and factor B levels. Here is some example data for a CMP process with 4 slurries and 3 different chemicals. This is an example of ANOVA Two Factor with Replication, since there is more than one sample item per combination factor. The table shows variations in the polishing rate in percent.

Treatments	A	B	C	D
1	1.31	1.82	1.43	1.45
	1.45	2.10	1.45	1.71
	1.46	1.88	1.63	1.66
	1.43	1.72	1.76	1.62
2	1.36	1.92	1.44	1.56
	1.29	1.61	1.35	2.02
	1.40	1.49	1.31	1.71
	1.23	2.24	1.40	1.38
3	1.22	1.30	1.23	1.30
	1.21	1.37	1.25	1.36
	1.18	1.38	1.24	1.31
	1.23	1.29	1.22	1.33

This table shows the two-factor ANOVA results for the sums, averages and variances.

Anova: Two-Factor With Replication					
SUMMARY	A	B	C	D	Total
1					
Count	4	4	4	4	16
Sum	5.65	7.52	6.27	6.44	25.88
Average	1.4125	1.88	1.5675	1.61	1.6175
Variance	0.004825	0.02586667	0.02455833	0.01273333	0.04386
2					
Count	4	4	4	4	16
Sum	5.28	7.26	5.5	6.67	24.71
Average	1.32	1.815	1.375	1.6675	1.544375
Variance	0.00566667	0.1131	0.00323333	0.073425	0.08373292
3					
Count	4	4	4	4	16
Sum	4.84	5.34	4.94	5.3	20.42
Average	1.21	1.335	1.235	1.325	1.27625
Variance	0.00046667	0.00216667	0.00016667	0.0007	0.00387833
Total					
Count	12	12	12	12	
Sum	15.77	20.12	16.71	18.41	
Average	1.31416667	1.67666667	1.3925	1.53416667	
Variance	0.01046288	0.10293333	0.02789318	0.04815379	

This portion of the table shows the Sum of Squares (SS), the Degrees of Freedom (df), the Mean Squares (MS), and the F-ratio for the rows, columns, and the interaction or error, as Microsoft Excel lists it. The chemicals show an F-ratio of 23.22 for an F-distribution with 2 degrees of freedom, and the slurries show an F-ratio of 13.81 for an F-distribution with 3 degrees of freedom, and an F-ratio of 1.87 for the interaction with 6 degrees of freedom. In this case, the F-ratio is much higher than F-crit, indicating that there is a statistical difference between the methods and treatments. This implies that these manufacturing processes are not the same.

Anova: Two-Factor With Replication						
ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Sample	1.0330125	2	0.51650625	23.2217366	3.3314E-07	3.25944631
Columns	0.92120625	3	0.30706875	13.8055824	3.7773E-06	2.86626555
Interaction	0.2501375	6	0.04168958	1.87433264	0.11225061	2.36375096
Within	0.800725	36	0.02224236			
Total	3.00508125	47				

Ask the Experts

Q: Why is Aluminum not typically used as a dopant atom??

A: The main reason process engineers don't use aluminum in standard CMOS processing is that the solid solubility of aluminum in silicon is quite low (1x10^18 atoms/cc). This makes it difficult to do heavy doping. However, there is some use of aluminum as a dopant atom in certain photovoltaic cells, where low leakage levels (and therefore light doping levels) are used.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.
6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.

7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing
5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation

12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage

18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

IRPS

International Reliability Physics Symposium

2018 IEEE International Reliability Physics Symposium

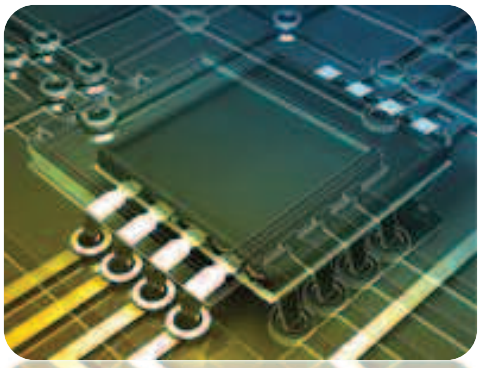
IEEE

March 11-15, 2018
Hyatt Regency San Francisco Airport
1333 Bayshore Highway
Burlingame, CA, USA 94010

Registration is available at www.irps.org

Chris Henderson, Semitracks President

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com anytime before the symposium!



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
March 19 – 22, 2018 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany

CMOS, BiCMOS and Bipolar Process Integration
September 10 – 12, 2018 (Mon – Tue)
San Jose, California, USA