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Low Pressure CVD

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Low Pressure CVD

In this section we'll discuss a variant of chemical vapor deposition known as Low Pressure Chemical Vapor Deposition, or LPCVD. This technique is commonly used for materials like polysilicon and silicon nitride deposition.

There are two basic types of chemical vapor deposition: low pressure CVD and atmospheric pressure CVD. In a low pressure CVD reaction such as plasma-enhanced CVD, the surface reaction is reaction rate limited. In order to grow the appropriate thickness, the temperature and time must be closely controlled. We discuss PECVD in a section close by. In an atmospheric pressure CVD reaction, the reaction rate is mass transfer limited. In this situation the flow of the gas must be uniform. This means that wafers cannot be placed too close to each other; otherwise they will interrupt the flow of the reaction gas.

Low pressure CVD has two distinct advantages over traditional chemical vapor deposition. LPCVD can occur at lower temperatures than traditional CVD. This allows one to use CVD to deposit layers after lower melting temperature materials have already been deposited, like aluminum. Furthermore, one can lower the temperature further by adding energy to a CVD process. Plasma enhancement is a common method to do this.

Low Pressure CVD has several disadvantages. Cleanliness is a major problem. Particles can be generated as a result of gas phase

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reactions instead of surface reactions. Other disadvantages include rough surfaces, surface cleaning issues, the need for accurate temperature control, gas entrapment, and toxic, hazardous gases. There is also a general lack of understand of CVD processes. Standard oxidation reactions have been studied for decades, while CVD processes have only been studied for the past dozen years. Many processes are even newer. Finally, there is a lack of proper gas phase species for most metals.

Let's move on and discuss the uses for LPCVD. The first one is silicon nitride. A quality silicon nitride layer is amorphous, dense, chemically and thermally stable, has a relatively high dielectric constant, and a low coefficient of thermal expansion. This film normally exhibits a high tensile stress, but it can be highly compressive in certain situations. The front-end-of-the-line process applications include creating a mask for selective oxidation of silicon like a LOCOS field oxide, creating a hard mask for the shallow trench isolation trench etch, creating an STI trench liner, and depositing ONO capacitor dielectrics in DRAMs. The back-end-of-the-line applications typically use PECVD, since one can use lower temperatures. We discuss that topic in a section close by. Basically, the deposition process involves reacting dichlorosilane and ammonia to produce a solid silicon nitride layer, and hydrochloric acid and hydrogen as exhaust gases. This occurs at temperatures between 700 and 800°C. In a hot-wall LPCVD reactor, one must compensate for depletion effects. The process is affected by many variables, each of which must be controlled for a favorable outcome.

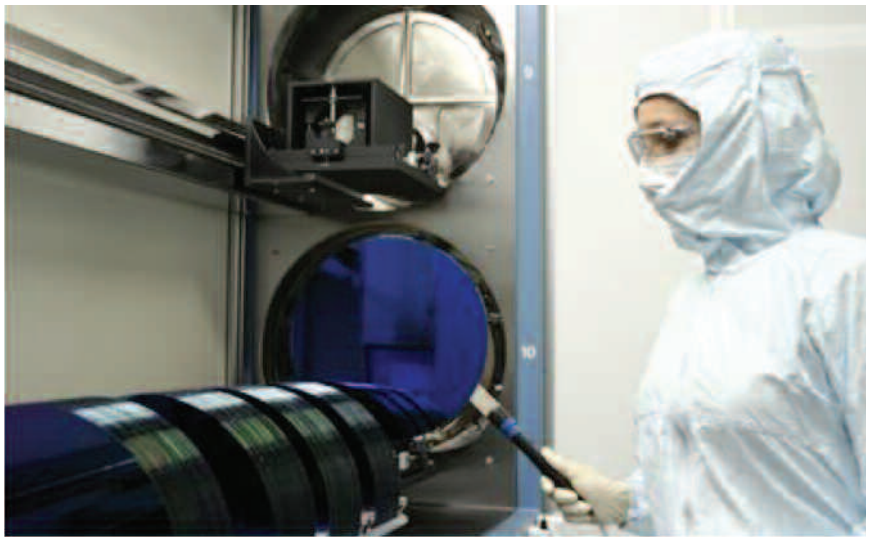
Polysilicon is another important application for LPCVD. The applications include heavily doped polysilicon for MOS transistor gates, capacitor electrodes, local interconnect in MOS circuits, and bipolar transistor emitters. They also include lightly doped polysilicon for high value resistors used for cross-coupled feedback in SRAMs, and STI trench refill. Process engineers can deposit these films conformally over steep topography. The polysilicon film is composed of small grains of single crystal silicon separated by grain boundaries. The properties of each grain are quite similar to those of single crystal silicon. However, the behavior along the grain boundaries is quite different, with enhanced diffusion properties, dopant segregation, and trapping of charge carriers.

Polysilicon exhibits a much higher resistivity than single crystal silicon for the same doping level. This occurs because the dopants segregate along grain boundaries, leaving fewer dopant atoms within the grains. Also, defects in grain boundaries decrease carrier mobility and the grain boundaries are full of dangling bonds—some of which can trap free carriers. The deposition process involves pyrolysis, or thermal decomposition, of silane. This yields solid silicon on the surface, and hydrogen as an exhaust gas. Process engineers typically use a batch process in a hot-wall LPCVD furnace with these approximate values. Process engineers might dilute the silane with a hydrogen carrier gas, which suppresses the gas phase decomposition of silane because it is one of the reaction products. Also, gas phase decomposition is undesirable because the resultant silicon particles will rain down on the growing film, causing roughening. Therefore, the engineers use a modified set of deposition conditions used to deposit amorphous silicon, which yields a slower reaction.

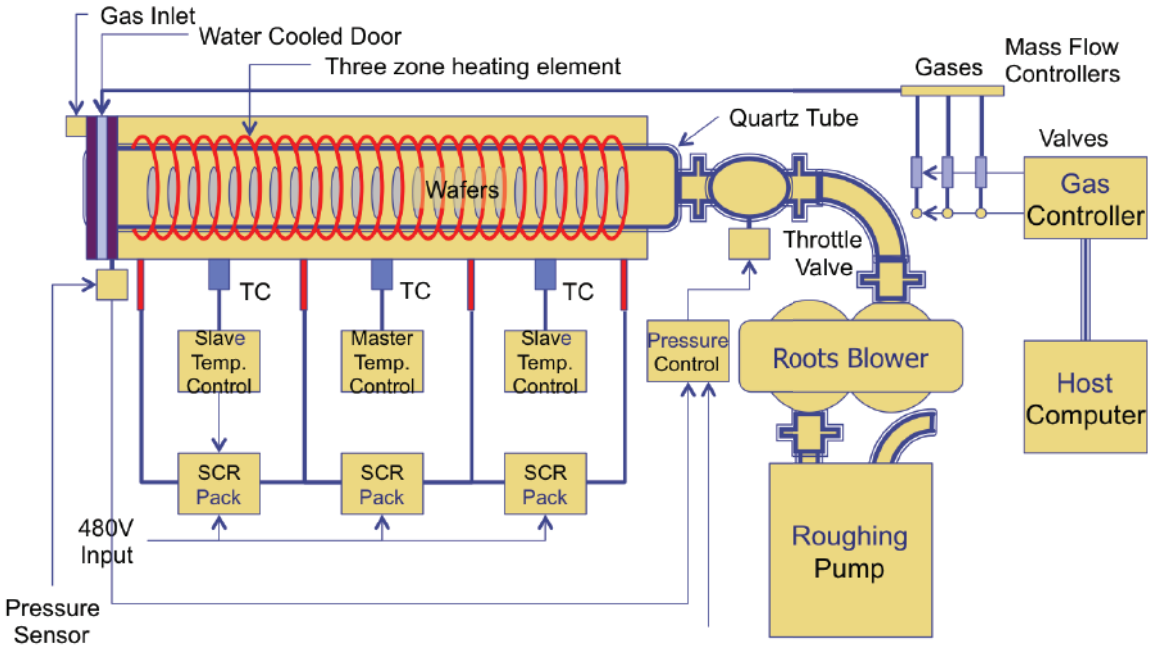
In most applications, process engineers dope the polysilicon to lower its resistance. There are three methods to do this: furnace doping, ion implantation, and in-situ doping. In furnace doping engineers pre-deposit from a liquid, solid or gas, as this is an easy method for very heavy doping. The major downside to this approach is lack of process control. Ion implantation is the preferred method since one can select the energy to put the range at the center of the film and do the anneal with rapid thermal processing. In-situ doping is another option where one dopes during the deposition by adding doping gases like diborane or phosphine to the reactant gases. In a batch reactor this severely complicates the process control, but it is less of an issue in a single wafer reactor. One cannot do dual-doped polysilicon with this approach though, where one doped the polysilicon over the n-channel transistor differently than over the p-channel transistor.

Let's move on and discuss LPCVD equipment. The hot-wall horizontal tube reactor is a common system for this process. It is used primarily for silicon nitride and polysilicon, the two materials we just discussed. It is very similar to an atmospheric oxidation furnace tube. These systems contain a long tube made from high purity silica, and a radiant heating system made from high resistance ceramic coils surrounding the tube. The gases are metered into the tube at one end, and exhausted at the other end. Process engineers mount the wafers in a fused silica boat, about 5 to 6 millimeters apart from one another. One typically loads between 100 and 200 wafers into the system at a time, which is possible because the environment is a surface reaction rate-limited process that doesn't required equal mass transport to all areas of all the wafers.

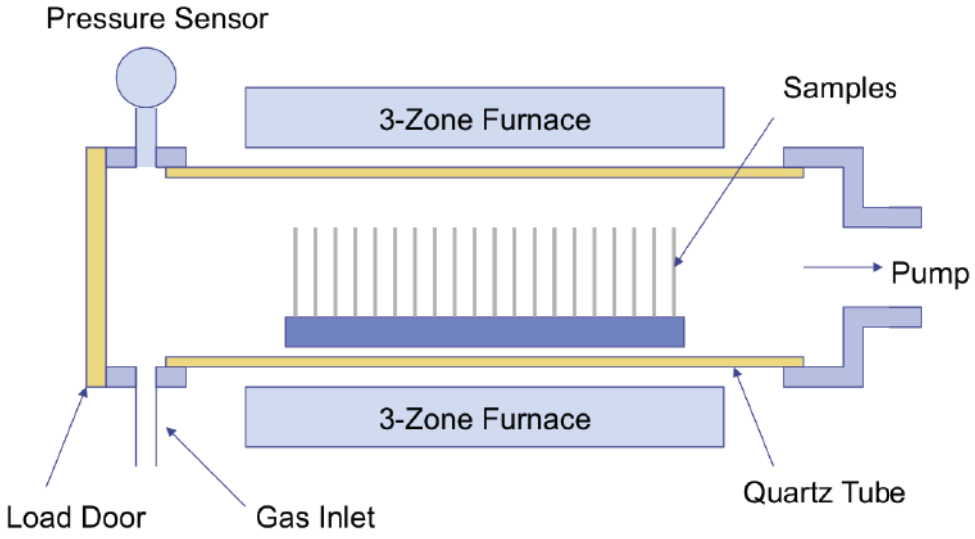
A typical LPCVD system uses vacuum pumps and a pressure control system to maintain a constant pressure. They operate between 600 and 850°C, and pressures between one-quarter and two torr. The advantages to LPCVD include a relatively simple design, excellent economy, high throughput and good uniformity. The disadvantages of these systems include susceptibility to particle contamination, which necessitates frequent cleans, and the need to compensate for gas depletion effects.



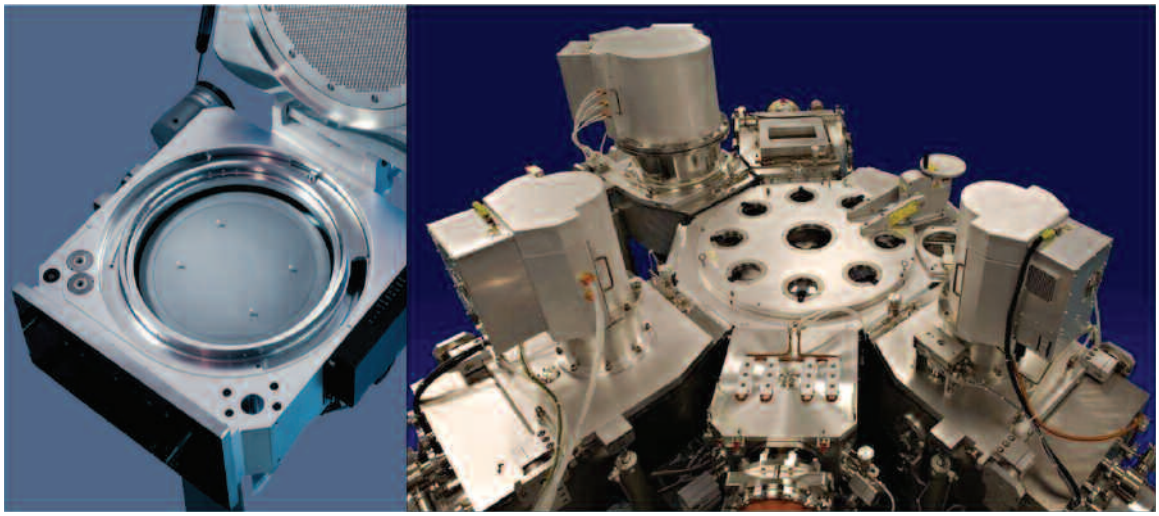
This figure shows a basic schematic for an LPCVD tool, along with the vacuum system. Again, these systems can hold many wafers in the quartz tube, allowing for high throughput in the process. Since the tube is rather long, most systems will contain zones that can be individually controlled to ensure better uniformity.



The next figure shows an example of a CVD quartz tube that processes wafers in batch form in more detail. A low pressure CVD reactor consists of a quartz tube connected to a pump. The gas inlet is used to introduce the reactant gases as well as gases used to purge the system, such as nitrogen. The wafers are loaded through the door on the left. In a low pressure system, the wafers can be placed closer, as is shown here. A furnace encompasses the quartz tube. This heats the chamber, driving the reaction rate faster.



Today, process engineers also use cluster tools for low pressure CVD steps. *Many manufacturers replaced their hot wall batch reactors for cluster tools in 300 millimeter and some 200 millimeter processes. *This technology is similar to Rapid Thermal Processing and Plasma Enhanced Chemical Vapor Deposition systems. These systems employ a cold wall reactor, which minimizes film deposition on the chamber walls. Another important aspect of these systems is that they perform single-wafer processing. This eliminates the need to operate in surface reaction rate-limited regime, eliminates cross-batch process variability, does not suffer from gas depletion effects, and facilitates in-situ doping. The deposition conditions are different from batch reactors; a prime example would be polysilicon. They use higher operating pressures, which produce deposition rates that are a factor of ten higher than batch reactors. Furthermore, multiple chambers allows clustering. For example, one can process the entire gate stack in the tool, beginning with the gate pre-clean, followed by the gate oxidation-nitridation, followed by the in-situ doped polysilicon deposition.



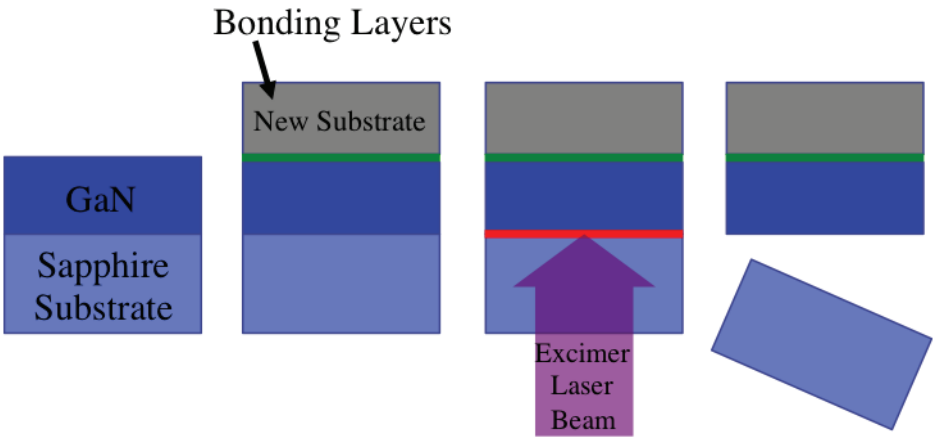
These images show examples of the process chamber and the entire cluster tool for LPCVD. Although these tools are more complex and suffer from slower throughput, the benefits of performing multiple operations together and doing them more uniformly outweigh the disadvantages in most situations.

In conclusion, we discussed low pressure chemical vapor deposition. This technique is used primarily for silicon nitride and polysilicon deposition. We discussed the two types of reactors. There are batch, or hot wall, reactors, that allow 100 to 200 wafer to be processed simultaneously, and there are single wafer—or cold wall—reactors, that can be integrated into cluster tools for operations like gate stack processing. These single wafer systems also provide better control for uniformity and doping, which is essential in most advanced processes.

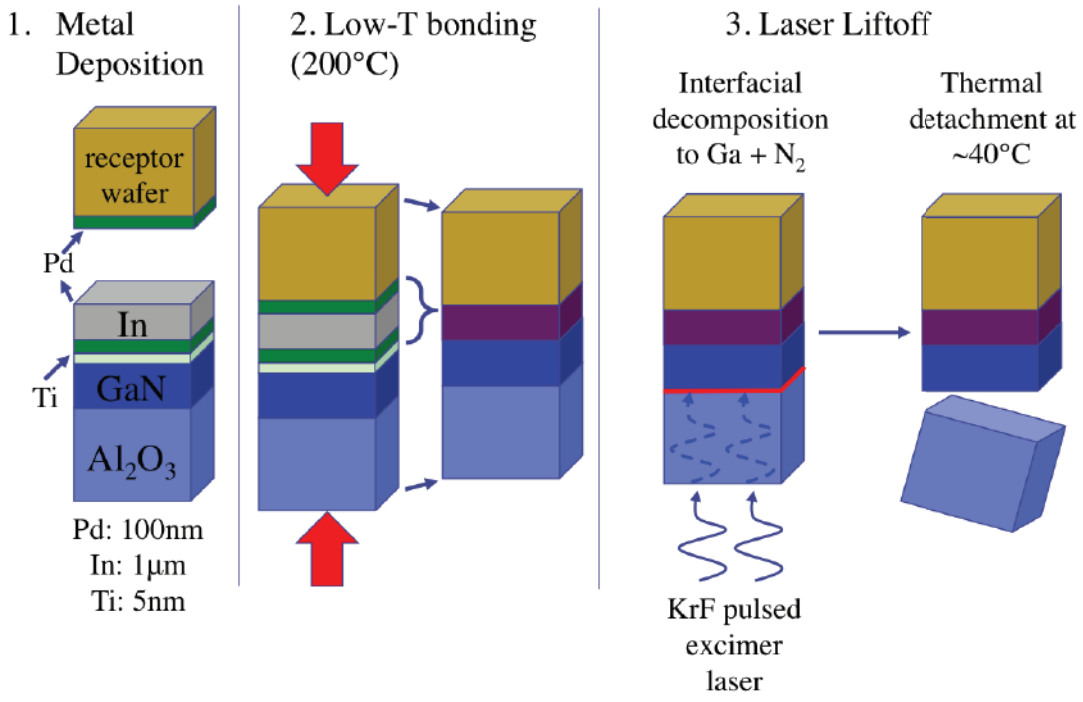
Technical Tidbit

Laser Liftoff Method

An important step for some types of Light Emitting Diodes (LEDs) is the substrate removal step. This is necessary for many types of vertical LED structures. There are two main techniques for performing this step: mechanical substrate removal and the laser lift-off technique. This approach fractures a horizontal interface, specifically the interface between the seimconductor and sapphire or silicon-carbide. This allows one to generate vertical and thin gallium nitride structures. Osram uses this approach for some of their products. IPG Photonics makes dedicated laser lift-off tools. Their manual tool can do 20 to 40 wafers per hour and their automated tool can do up to 60 wafers per hour. Their tools are relatively expensive though, ranging in price from $500,000 to $1,000,000.



Let's look a little further into how the laser lift-off method works. First, one deposits metal on the receptor and semiconductor wafers. The typical metal is palladium on the receptor wafer, and titanium-palladium-indium on the semiconductor wafer. Second, one bonds the wafers together at low temperatures. This creates a palladium-indium alloy. Third, one focuses laser light through the semiconductor wafer on the sapphire/gallium nitride interface. The laser energy initiates a fracture, causing the gallium nitride layer to separate from the sapphire substrate, but remain attached to the receptor wafer due to the palladium-indium bond. This technique is growing in popularity, as it reduces the consumption of materials like sapphire substrates.



Ask the Experts

Q: I am just getting started in Semiconductor Reliability. What are the best conferences to attend that focus on this topic?

A: Depending on your location, there are several that I would recommend:

- If you are in the United States, then I would recommend the International Reliability Physics Symposium (IRPS). It will be held in Pasadena, California, April 17 – 21, 2016. http://www.irps.org
- Another good conference on Wafer Level Reliability is the Integrated Reliability Workshop (IRW). It will be held in the Lake Tahoe area, October 9 – 13, 2016. http://www.iirw.org
- If you live in Europe, I would recommend the European Symposium on Reliability of Electron Devices Failure Physics and Analysis (ESREF). It will be held in Halle, Germany, September 19 – 22, 2016. http://conference.vde.com/esref-2016/Pages/default.aspx
- And finally, if you live in Asia, I would recommend the International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA). It will be held in Singapore, July 18 – 21, 2016. http://www.ieee-ipfa.org/2016

Global Semiconductor & Electronics Forum

March 9th-11th 2016
Shanghai Marriot Hotel City Centre
Shanghai, China

Semitracks will be attending the Global Semiconductor Forum in Shanghai, China. If you would like to talk with us regarding education and training programs, please send us an email at info@semitracks.com

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Registration is available at www.arena-international.com/gsef

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Semitracks will also be offering an **Introduction to Processing Course** just prior to the GSF meeting, on March 7-8. This course will give attendees an overview of the wafer fabrication and package assembly processes. It is a great way to get up-to-speed quickly on semiconductor manufacturing. For more information, please go to: **http://http://www.semi-tracks.com/courses/processing/introduction-to-processing.php**

Spotlight: Process Integration Short Course

Our CMOS, BiCMOS and Bipolar Process Integration Course is scheduled for March 21 and 22 in Albuquerque, New Mexico. We don't offer this course publicly very often, so now is your opportunity to attend it. For further information, please visit the website (Click here)

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS and BiCMOS Process Integration*** is a five-day course that offers detailed instruction on the physics behind the operation of a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and interconnect performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into four segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why CMOS (Complimentary Metal Oxide Semiconductor) devices dominate the industry today
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.

3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, strained silicon, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

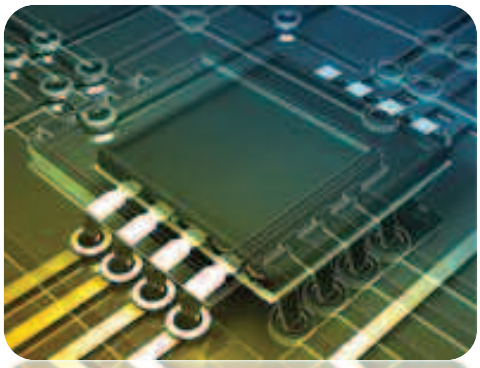
INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction
2. Conventional CMOS
   a. Key Components and Parameters
   b. Process Overview and Integration Issues
   c. Scaling and Limitations
3. Mobility Enhancement Techniques
   a. Strained Silicon
   b. Crystal Orientation
4. Gate Stacks, High-k Dielectrics
   a. Gate Conductor Materials and Properties
   b. High-k Materials and Properties
   c. Gate Stack Integration
5. Options for Source-Drain, Extensions
   a. Elevated Source/Drain
   b. Co-Implantation of Inactive Species
   c. Schottky-Barrier Source-Drain
6. Three-Dimensional Structures
   a. FinFETs, Multi-Gates
7. Interconnects
   a. Aluminum Interconnects, Issues
   b. Copper Interconnects, Issues
   c. Low-k Dielectrics

8. Conventional BiCMOS
   a. Bipolar Transistor Fundamentals
   b. BiCMOS Process Overview
   c. Scaling and Limitations
9. Bipolar Enhancement Techniques
   a. SiGe
   b. SiGe:C
10. CMOS/BiCMOS Reliability Considerations
   a. Electrostatic Discharge
   b. Electromigration and Stress Migration
   c. Soft Errors, Plasma Damage
   d. Dielectric Reliability
   e. Bias Temperature Instabilities
   f. Hot Carrier Reliability
   g. Burn-In
11. Yield Considerations
   a. Yield Detractors
   b. Models
   c. Monitors



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
January 18 – 21, 2016 (Mon – Thur)
San Jose, California, USA

Packaging Failure and Yield Analysis
February 22 – 24, 2016 (Mon – Wed)
Manila, Phillippines

Introduction to Processing
March 7 – 8, 2016 (Mon – Tue)
Shanghai, China

CMOS, BICMOS and Bipolar Process Integration
March 21 – 22, 2016 (Mon – Tue)
Albuquerque, New Mexico, USA

Wafer Fab Processing
March 29 – April 1, 2016 (Tue – Fri)
San Jose, California, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany

Advanced Thermal Management and Packaging Materials
June 7 – 8, 2016 (Tue – Wed)
Albuquerque, New Mexico, USA