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Thermal Processing—Part VI, Ancillary Tools

By Christopher Henderson

This month, let's move on to briefly discuss the ancillary tools for thermal processing. There are two common tools for measuring oxide thickness: the reflectometer and the spectroscopic ellipsometer. The reflectometer uses optical interference. It determines the interference between the light reflected at the air-silicon dioxide interface and the light reflected at the silicon dioxide-silicon interface. This technique only works on oxides thicker than 10 nanometers. The spectroscopic ellipsometer uses a laser to look at changes in polarization that occur when the light reflects off of the silicon or silicon dioxide surface. The polarization change depends on the spectrum, so the spectrum can provide more accurate data. This technique works on dielectrics down to 5 angstroms, and can be applied to a wider range of materials than just silicon dioxide, making it a good choice for low-K and high-K dielectrics. Finally, the transmission electron microscope can be used for offline verification of very thin oxides. Since it requires destructive sample preparation, it must be performed outside of the normal process flow.

The industry uses still other tools to assess oxide film quality. Process engineers make these measurements both inline and off-line. For dielectric strength, process engineers measure time to breakdown, charge to breakdown, and other MOS measurements. For mobile ion charge, engineers use capacitance-voltage plotting. They do this with and without bias and at different temperatures. They

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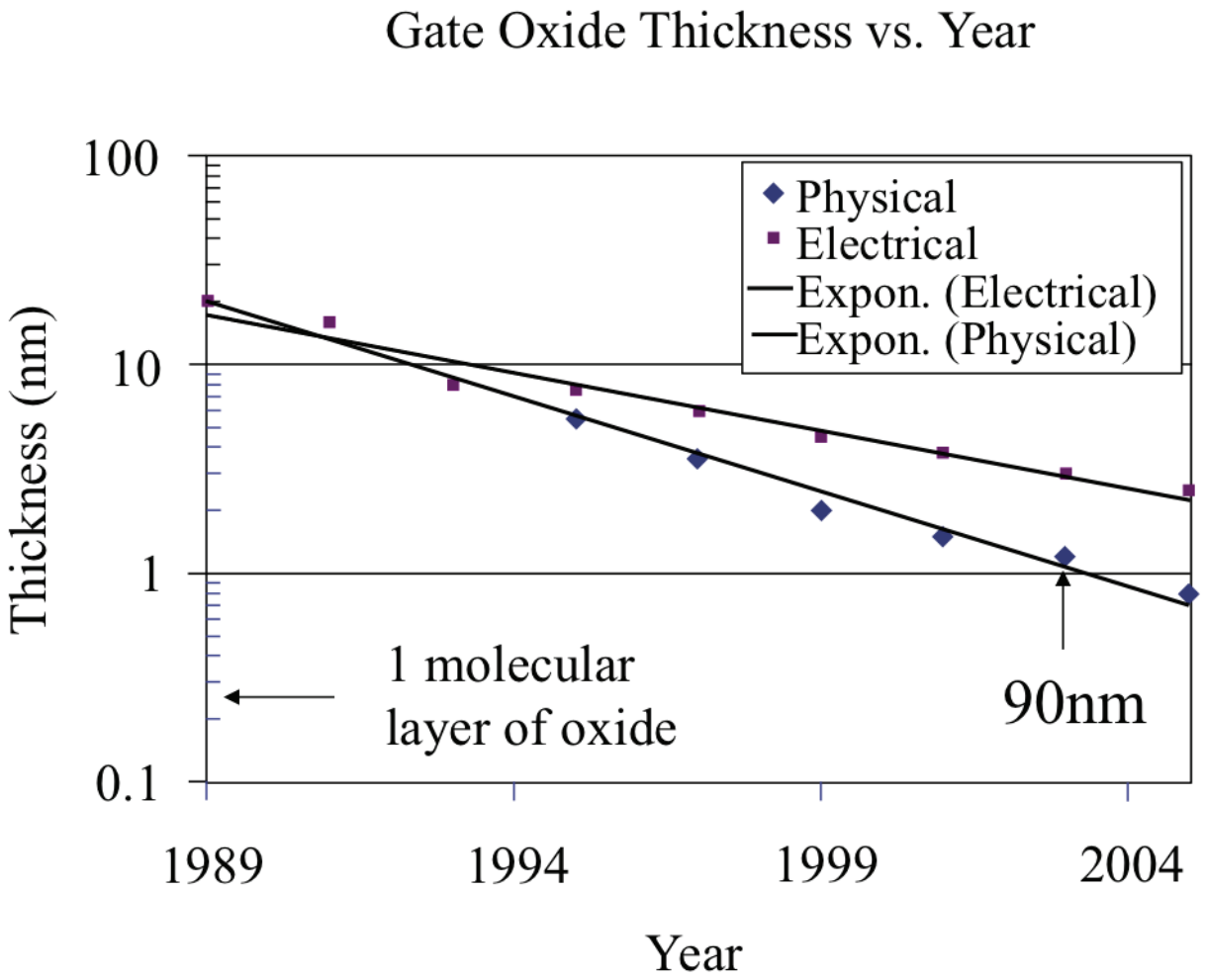
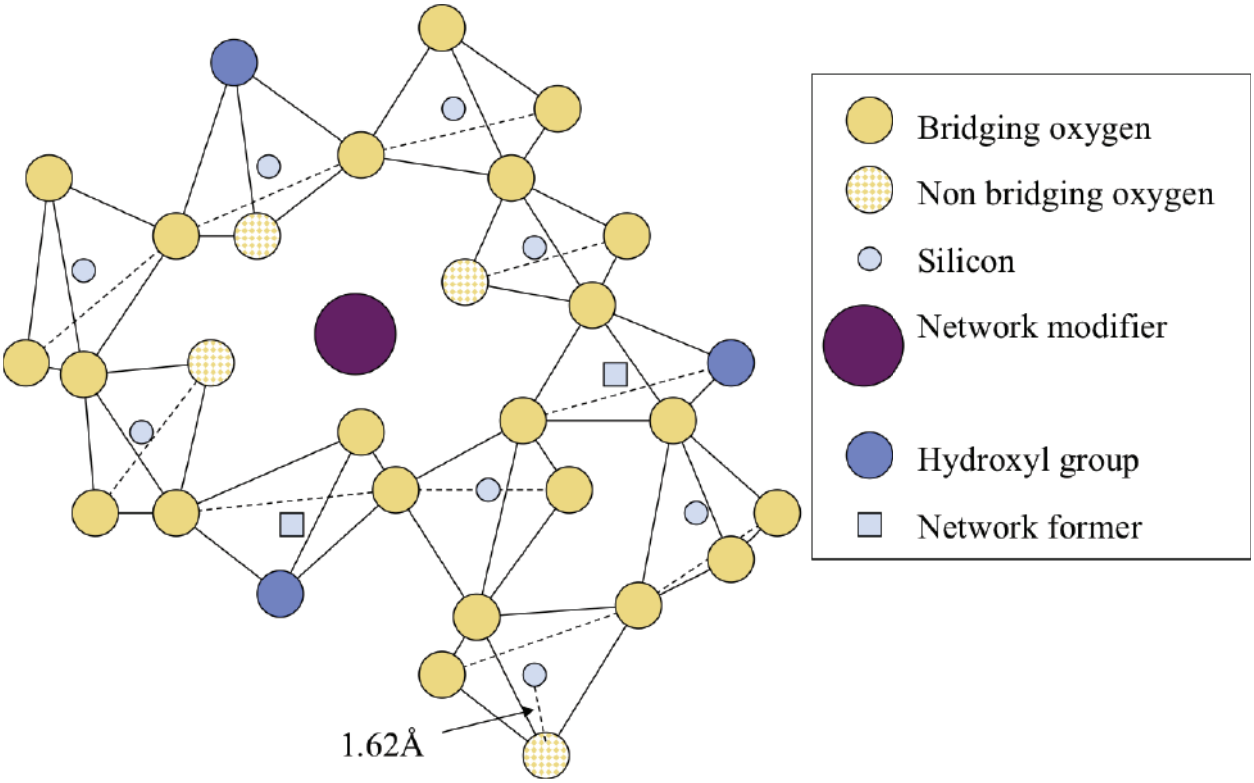
measure the shift in the flatband voltage of an MOS transistor under stressed conditions and compare it to an unstressed sample to look for differences. For fixed and trapped charges, again process engineers use the capacitance voltage plot and other MOS transistor measurements. Finally, for particulate contamination, they use wafer inspection systems to look at both patterned and unpatterned wafers.

With all thermal processing, temperature control is the most critical factor. Process engineers must include examination of ramp rates, monitor for temperature overshoot, account for stabilization times, and other variables. As feature sizes become smaller and smaller, this is a more important activity.

Let's move on now and discuss the oxidation process. The oxidation process is used for several key steps in the manufacture of a semiconductor device. Probably the most important step is the gate dielectric. The gate dielectric is the foundation of the MOS transistor. In order to create state-of-the-art, functional integrated circuits one must be able to grow a high quality gate dielectric. Oxidation is also used to form the isolation between transistors. The LOCOS (pronounced low-cos) process, or Local Oxidation of Silicon, relies on oxidation to form the silicon dioxide isolation layer. Oxidation is also used in the shallow trench isolation process to create the oxide layers on the sidewalls of the trench. Oxidation is used to mask for ion implantation. It is also used to grow a feature called a pad oxide that provides stress relief between the silicon and silicon nitride layers. Oxidation is also used to create tunnel oxides, capacitor dielectrics, and sacrificial oxide layers.



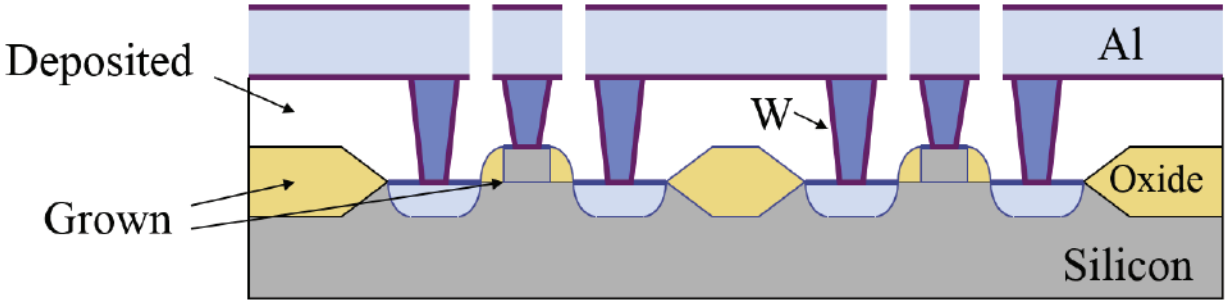
As Moore's Law continues, the thickness of the gate oxide has continued to decrease. This data shows the gate oxide thickness as a function of technology. In 1989, at the 1.2μm feature size, the gate oxide thickness was approximately 20 nanometers. By 2003, at the 90nm feature size, the gate oxide thickness was approximately 1.2nm or 12Å. We are rapidly approaching the situation where the gate oxide thickness is on the order of just a few layers of atoms. Although silicon dioxide has been an excellent gate dielectric, it will need to be replaced in the next few years. This is an area of extensive research currently.



The glass or amorphous state of silicon dioxide is called fused silica. This state is not thermally stable below about 1700°C. This means that it will slowly convert into a crystalline form. The good news is that this process is so slow below 1000°C that for all intents and purposes, it does not occur. The structure of fused silica glass is moderately complex, as evidenced by the image shown here. Basically, the structure is composed of units of one silicon atom and four oxygen atoms loosely bound together by the oxygen atoms. There are bridging and non-bridging oxygen atoms in the structure. The distance between the silicon atom and the oxygen atoms is 1.62Å (angstroms), while the distance between oxygen atoms is 2.27Å. The network formers are the doping species like phosphorus and boron. Network modifiers are the mobile ionic species like sodium, potassium, and lead. Because this structure is quite loose, various deposition conditions can lead to various properties.

The process of silicon dioxide formation is straightforward. One exposes the silicon surface to an oxidizing environment at high temperatures. The environment might consist of oxygen, or steam might be used to accelerate the growth process. High temperatures also help to accelerate the process, allowing moderately thick films of up to 1μm to be grown in a time frame of several hours or less. The results are

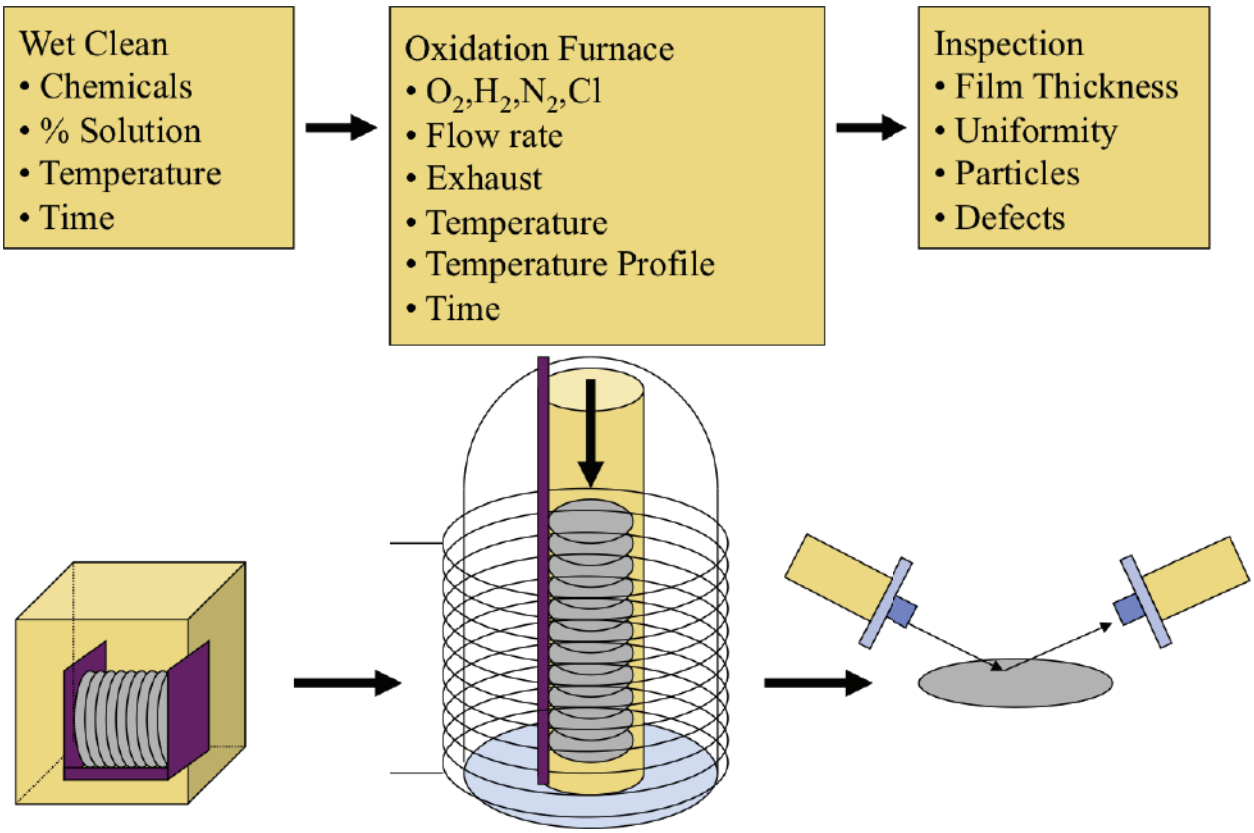
reproducible, and the oxide film can be quite uniform. When we discuss thermal oxidation, we are talking about grown oxides as opposed to deposit oxides. Grown oxides are in direct contact with the silicon surface, while deposited oxides are used at higher levels in the process, like interlevel dielectrics.



As the silicon dioxide is formed, silicon bonds are broken at the surface of the silicon. Oxygen atoms insert themselves between the silicon atoms. The resulting silicon-oxygen bonds take up more room than the silicon-silicon bonds. This causes an expansion in the material. Silicon dioxide occupies 227% of the original space occupied by the silicon.

Item	Value
Melting Point (°C)	~ 1600
Density (g/cm^3)	2.2 (6.6 x 10^{22} atoms/cm^3)
Refractive Index	1.46
Dielectric Constant	3.9
Band Gap (eV)	9
Si/SiO_2 Barrier (eV)	3.1 for electrons, 4.6 for holes
Dielectric Strength (V/cm)	10^7 (10 V for 100 Å oxide)
Stress (on Si) (Mpa)	< 400
Thermal expansion coefficient ($°C^{-1}$)	5 x 10^{-7}
Thermal conductivity (W/cm-K)	0.014
DC resistivity (W-cm)	10^{14} - 10^{16}
Etch rate in buffered HF (Å/min)	1000
Note: Buffered HF 34.6% (wt.) NH_4F, 6.8% (wt.) HF, 58.6% H2O	

Here are some of the more common properties of silicon dioxide. As we mentioned earlier, its structure is amorphous and dependent on the oxidation conditions. It has a very high melting point and low density. The bandgap of silicon dioxide is rather high, making it a formidable barrier to electrons as well as holes. The resistivity of an oxide layer is quite high, ranging from 10 to the 14 up to 10 to the 18 ohms per centimeter. Thermally grown oxide can be removed using a buffered hydrofluoric acid etch. A standard etch, listed at the bottom of the table, will remove approximately 1000Å per minute.



This diagram shows an overview of the thermal oxidation process. Before oxidation begins, the wafers are cleaned using a prescribed procedure. Next, the wafers are placed in the oxidation furnace. Gases such as oxygen, hydrogen, nitrogen, and chlorine might be introduced to achieve different growth rates, stoichiometries (pronounced stoy-key-om-e-trees), and properties. Other parameters such as flow rate, exhaust rate, temperature, the temperature profile and time can be used to obtain a particular thickness or quality to the oxide. After the oxidation is complete, the oxide layer is inspected for film thickness, uniformity, particles or other types of defects.

Here is a breakdown of the pre-oxidation steps. First, wafers undergo a series of wet cleaning processes. The first of these cleans is the Piranha etch. This is an aggressive etch that removes organic contamination and particles. The next clean is the standard clean one or SC-1. This etch removes

particles. This is followed by an SC-2 clean, which removes inorganic contaminants. This is followed by a quick etch in hydrofluoric acid to remove the native oxide that grows during normal storage conditions. The wafers are then loaded immediately into the furnace for the oxidation process. The growth of the oxide occurs right at the silicon/silicon dioxide interface. Initially, the rate of the reaction is limited by the rate of the surface reaction. As the oxide layer grows, the reaction becomes limited by the diffusion of the oxygen to the silicon surface.

The typical process sequence is listed here. First, the wafers are cleaned to start with a pristine surface. Next, the cleaned wafers are loaded into a quartz boat. The oxidation furnace is set to idle and purged with dry nitrogen. Dry nitrogen is used to prevent oxidation during idle furnace and the temperature ramp processes. The idle temperature is approximately 850°C. Next, the wafers are pushed into the furnace. The temperature is ramped up at a rate of 10°C per minute to the oxidation temperature and stabilized. Once the temperature has stabilized, the nitrogen gas is replaced with oxygen, steam, or an oxygen/hydrochloric acid mixture. The oxidation process runs for the specified period of time. Once it is complete, the furnace is purged with nitrogen to quench the oxidation process. The furnace is cooled to room temperature, and the wafer boats are pulled out of the furnace.

In summary, we covered thermal processing equipment and process issues. There are two major categories of thermal processing equipment: oxidation and diffusion furnaces, and rapid thermal annealing systems. In many instances, oxidation and diffusion can be handled by the same furnaces. There are also numerous ancillary tools for oxide characterization, including reflectometers and ellipsometers for oxide thickness, and CV plotters for charge characterization. We discussed oxide formation and its properties, explaining the atomic structure of silicon dioxide as well as its common physical and electrical properties. Finally, we discussed the basic process sequence for an oxidation step.

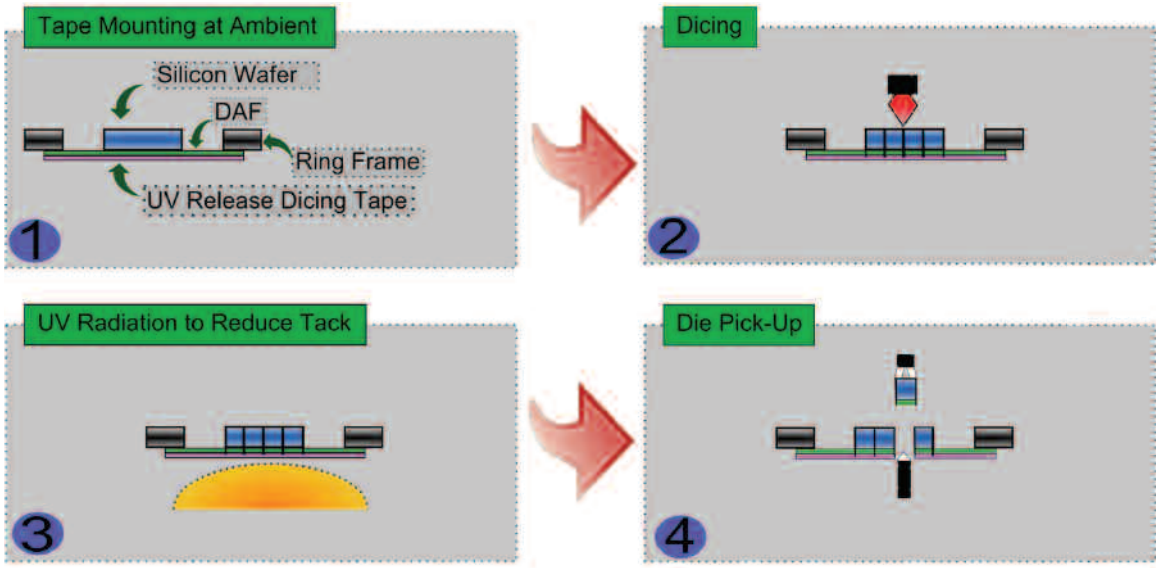
Technical Tidbit

Die Attach Film

A die attach film, or DAF, can be an alternative to using epoxy tubes. Die attach film is a product that combines dicing tape and die attach into one single sheet. This is a high volume manufacturing process, and die attach films can be used where one does or does not need an electrically conductive path between the die substrate and the leadframe. Die attach film can also provide a more uniform bond line, create a uniform fillet, and avoid die tilt problems. Die attach film typically comes in rolls like we picture here, where the DAF is the same size as the wafer. Accordingly, these rolls can be for 150, 200, or 300 millimeter wafers.

A die attach film can provide a method to facilitate sawing and mounting of small dice. One of the big challenges with small dice and die attach paste is making sure the device is level during the mount process on the leadframe. These die attach films are designed to work with a variety of die sizes (from 0.2mm to 10mm on a side), with thin dice (down to 50um), with wafer metallization schemes (including no metallization, TiNiAg, and Au) and leadframe metallization (Cu, Ag, Au, NiPdAu). Die attach films are thin, so there is less risk of the die shifting during the mount and cure operations. Die attach films are shelf-stable, so they can be shipped and stored under normal temperature conditions. Die attach films eliminate the formation of a die attach fillet. Elimination of the die attach fillet saves room in the package design, which can lead to lower Au wire costs (less wire used for bonding), lower mold compound costs (smaller package), and lower leadframe costs (smaller leadframe). This can also be useful when placing die close together in a small package. One drawback to a die attach film is that it can lead to higher stress conditions in some package material systems.

The process for using a die attach film is similar to standard wafer dicing tape. First, one spreads out the die attach film over the ring frame and then cuts the die attach film to fit the ring frame. One then mounts the silicon wafer to the die attach film. Next, one proceeds with the dicing operation. After the dicing operation, one applies ultraviolet radiation to the backside of the film to reduce the tack of the film. Finally, one can then use a pick and place tool to lift the die (and the die attach film under the die) from the tape and place it on the leadframe for mounting and curing.



Ask the Experts

Q: Where do we use melamine in the IC packaging process??

A: Melamine is a material used for the cleaning of mold stain deposited during the molding of epoxy molding compound for encapsulation of leadframe products like capacitors, resistors or semiconductor IC chips. This allows thermosets and thermoplastics to easily come out of the mold after molding.

Spotlight: Product Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can also involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types can create difficulties. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. Customers expect fast, smooth qualification, but incorrect assumptions, use conditions, testing, calculations, and qualification procedures can severely impact this process. Your company needs competent engineers and scientists to help solve these problems. ***Product Qualification*** is a two-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor technology and product qualification. This course is designed for every manager, engineer, and technician concerned with qualification in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues and how to resolve them.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and relationship to qualification.
2. **Failure Mechanisms.** Participants learn how product qualification and failure mechanisms relate to one another. We provide an overview of these mechanisms. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, EOS, ESD, latchup, drop tests, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to qualify today's components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled in qualification.
4. The seminar will discuss the major qualification processes, including JEDEC JESD47, AEC Q-100, MIL-STD, and other related documents.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement additional tests that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

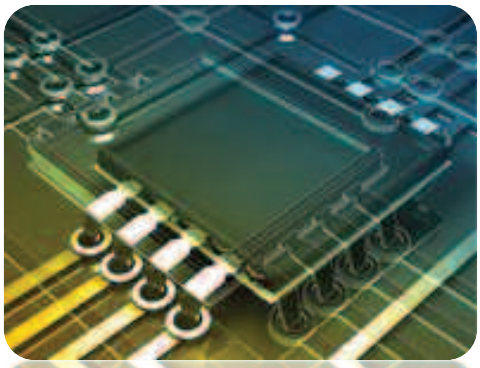
By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures
3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding
4. Overview of Package Level Mechanisms
   a. Ionic Contamination
   b. Moisture/Corrosion
   c. Thermo-Mechanical Stress
   d. Interfacial Fatigue
   e. Thermal Degradation/Oxidation
   f. Solder Joint Reliability
5. Overview of Board Level Reliability
   a. Solder Joint Reliability
   b. EOS/ESD/LatchUp
   c. Single Event Effects

Day Two (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
7. Developing Screens, Stress Tests, and Life Tests
   a. Burn-In
   b. Life Testing
   c. HAST
   d. JEDEC-based Tests
   e. Exercises
8. Developing a Qualification Program
   a. Process
   b. Standards-Based Qualification
   c. Knowledge-Based Qualification
   d. MIL-STD Qualification
   e. JEDEC Documents (JESD47H, JESD94, JEP148)
   f. AEC-Q100 Qualification
   g. When do I deviate? How do I handle additional requirements?
   h. Exercises



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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Product Qualification
January 26 – 27, 2015 (Mon – Tue)
San Jose, California, USA

Wafer Fab Processing
January 26 – 29, 2015 (Mon – Thur)
San Jose, California, USA

EOS, ESD and How to Differentiate
January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA

Failure and Yield Analysis
April 27 – 30, 2015 (Mon – Thur)
Munich, Germany

Semiconductor Reliability
May 4 – 6, 2015 (Mon – Wed)
Munich, Germany

EOS, ESD and How to Differentiate
May 7 – 8, 2015 (Thur – Fri)
Munich, Germany