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Alternate Channel Materials for High Mobility CMOS

By Christopher Henderson

This year's International Electron Device Meeting (IEDM) discussed a wide range of approaches for creating CMOS transistors with better performance. One axis of performance that is important is higher speed for faster switching. Higher speed invariably means higher mobility, so researchers have been investigating techniques to make this happen.

Silicon has a moderate mobility, but there are methods to improve it marginally. This can be done using strain. Companies like Intel and TSMC offer technologies and devices that use strained silicon. To get a larger improvement, one needs to consider alternate materials.

This table shows the major materials and candidates that can be or are used in CMOS devices. Silicon is the existing material for most devices. The electron and hole mobility for silicon are reasonable, but they're not the highest numbers that are potentially available. Germanium has a much higher electron mobility and a lower electron mass. More importantly, germanium has the highest hole mobility of any of the major semiconductor materials at 1900 cm^2/V-sec. It also has the lowest mass for heavy holes, which is the main type of carrier in a p-channel transistor. Some companies, like IBM, mix Si and Ge together in the transistor channel to improve mobility. GaAs, InP, InAs, and InSb all have even higher mobilities. InAs and InSb have the highest mobilities, but the bandgaps for these materials are quite low. GaAs and InP have a larger bandgap, which makes them more useful in low power applications.

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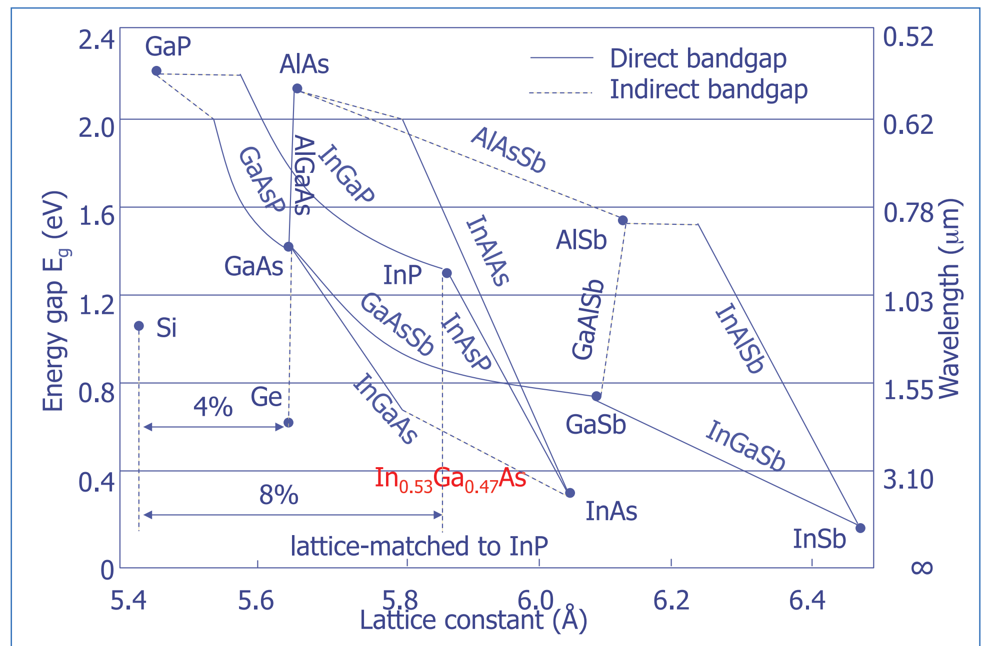
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

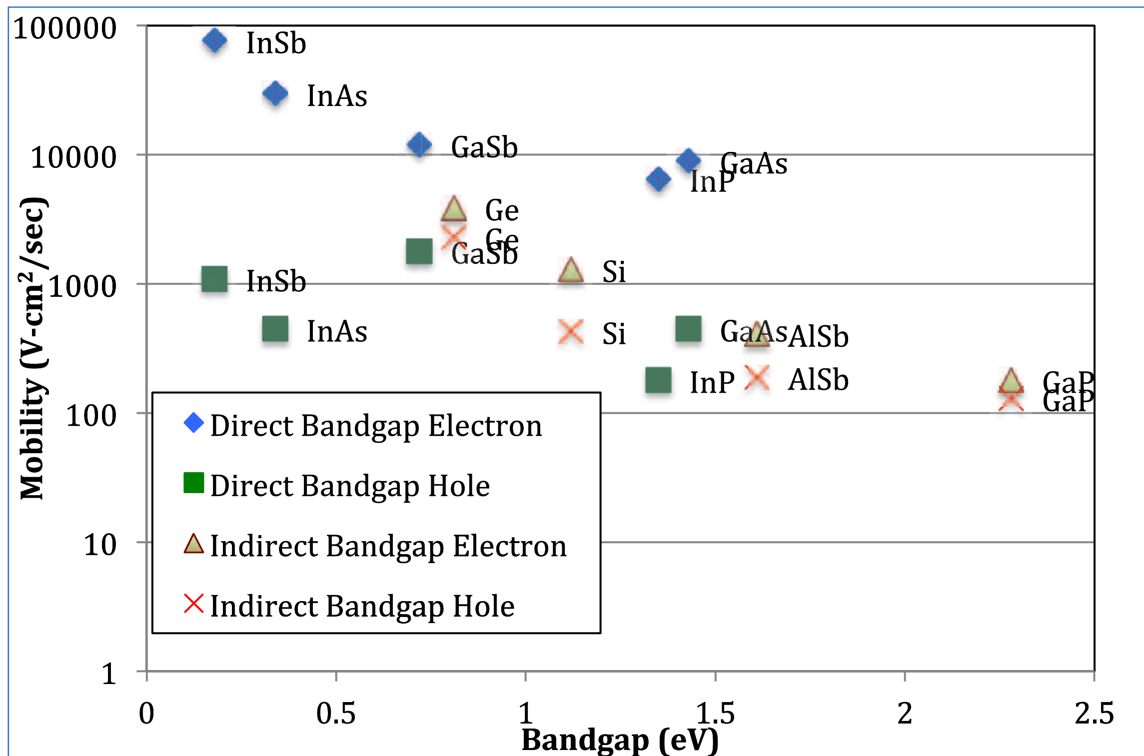
Material	Si	Ge	GaAs	InP	InAs	InSb
Electron Mobility (cm^2/V-sec)	1600	3900	9200	5400	40000	77000
Eff. Electron Mass (/m_o)	m_t: 0.19 m_l: 0.916	m_t: 0.082 m_t: 1.467	0.067	0.08	0.026	0.0135
Hole Mobility (cm^2/V-sec)	430	1900	400	200	500	850
Eff. Electron Mass (/m_o)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	m_{HH}: 0.45 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.12	m_{HH}: 0.57 m_{LH}: 0.35	m_{HH}: 0.44 m_{LH}: 0.016
Bandgap (eV)	1.12	0.66	1.42	1.34	0.36	0.14
Permittivity	11.8	16	12	12.6	14.8	17

In order to create a channel with a different material, one must take into account the lattice mismatch. This chart shows the energy gap of several compound semiconductors as a function of their lattice constants. We also include germanium and silicon on the list. In general, germanium and the three-five materials have larger lattice constants than silicon. A high mismatch is worse for process integration as it is hard to control the strain induced by the differences in the lattice constants. Notice that germanium is about four percent larger than silicon. InGaAs is approximately eight percent larger, when deposited as a 53 percent indium, 47 percent gallium ratio.



Materials with a lower band gap tend to have lower electron effective mass (high electron mobility) and higher permittivity. Since a narrow bandgap leads to high leakage current, it is necessary to choose appropriate materials from the viewpoint of both effective mass and bandgap. This means that materials like germanium and gallium arsenide are best positioned as alternate channel materials. However, this is only part of the story. Another factor for which one must account is the Schottky barrier height. The Fermi level position tends to be strongly correlated with the minimum in the

interface trap density. The Schottky barrier height is also correlated to the interface trap density minimum. Therefore, one would prefer a material with a lower Schottky barrier height against electrons for an n-channel device, and a lower Schottky barrier height against holes for a p-channel device. Germanium is a suitable candidate for the p-channel device, but gallium arsenide is not as suitable. Better materials from a Schottky barrier standpoint would be indium arsenide, indium phosphide, or indium gallium arsenide.



In conclusion, there are a number of possibilities, but each possibility has advantages and disadvantages. Germanium is an excellent choice for p-channel transistors, as it has the highest hole mobility, minimal lattice mismatch, and a low Schottky barrier height against holes. GaAs is a mature technology, has a large bandgap (which means low leakage), and has a relatively low lattice mismatch, but it has a high Schottky barrier height to both electrons and holes. InP and InGaAs are both suitable for n-channel transistors as they have low Schottky barrier heights to electrons, but their lattice constants are quite different than silicon. InAs might also be suitable, but its bandgap is quite narrow, leading to higher leakages. GaSb might be suitable for p-channel transistors, but it has not been studied sufficiently yet. It also has a large lattice mismatch to silicon. InSb is yet another candidate that could be used in both p- and n-channel transistors, but the bandgap is very narrow and the lattice mismatch to silicon is quite large. At this time, germanium is the leading candidate to replace silicon in the p-channel transistor, and InAs or InGaAs are probably the leading candidates for the n-channel transistor, but new results could change the outcome. If the research continues to be positive, we should expect to see these materials used in transistors within the next 4-8 years.

Current Collapse

By Christopher Henderson

Gallium nitride (GaN) is gaining traction as a material for high power semiconductor devices. Several manufacturers are now selling GaN devices for applications that require high power and high voltage, like military radar systems, blue LEDs for Blu-Ray players, and power inverters in satellites. As with all semiconductor devices, GaN suffers from various failure mechanisms. We can group failure mechanisms into two general areas: parasitic effects and degradation mechanisms. Parasitic effects include current collapse, excess leakage current, the Kink effect, and hot electron degradation. Common degradation mechanisms include gate leakage current, trap formation, gate metal diffusion and ohmic metal degradation. In this article, we'll cover current collapse in more detail.

Current collapse manifests itself as a lag or delay in current through a transistor as the gate is switched on and off. The lag is primarily associated with the rise in current as the gate-to-source voltage goes high, rather than the fall in current as the gate goes low. This shows up as a slump, shown in Figure 1 on the upper right. The correct waveform is shown on the lower right.

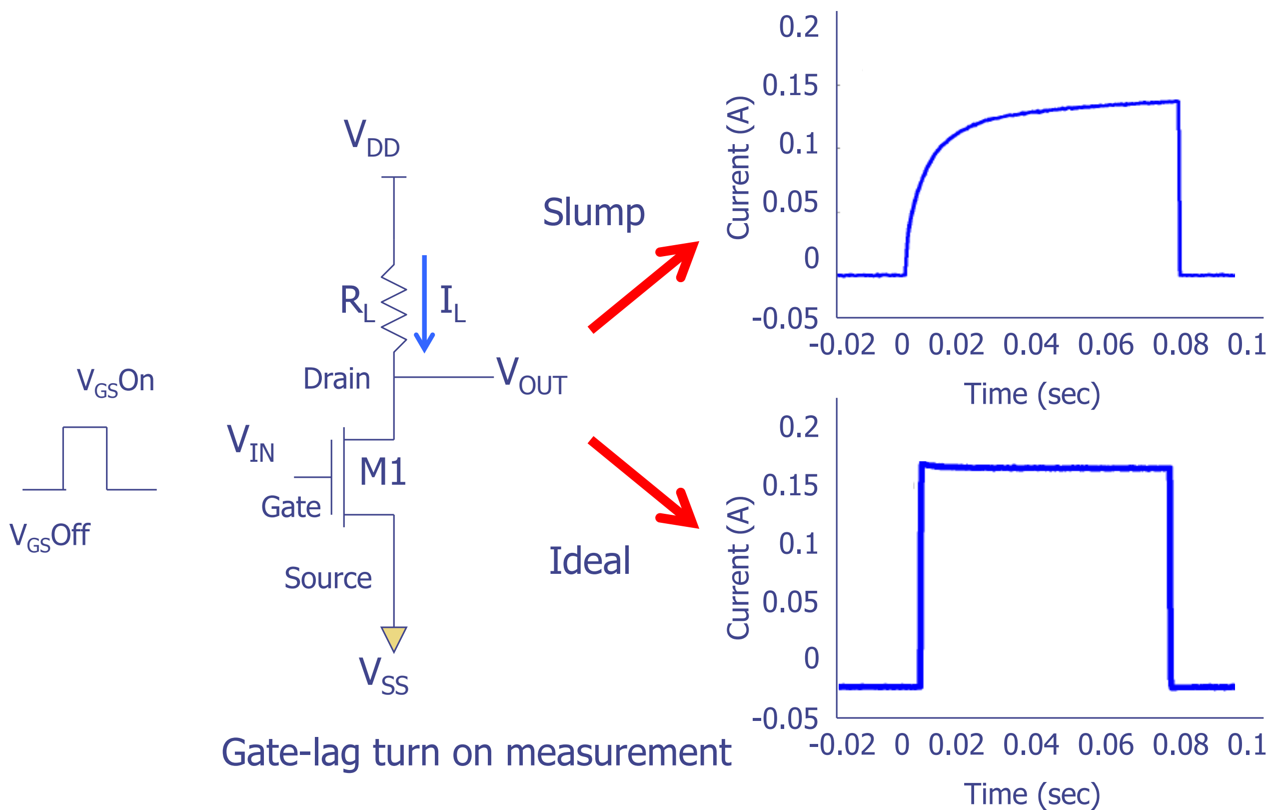


Figure 1

Figure 2 shows experimental data that characterizes the current collapse effect. The degree of collapse is associated with the applied voltage to the gate. The higher the applied gate voltage, the greater the current collapse. The current goes down as a result of a change in threshold voltage and the decrease in transconductance. Current collapse is in general due to surface traps. One of the major differences between silicon and compound semiconductor-based transistors is the lack of a native oxide or dielectric in a compound semiconductor MOSFET. Since one cannot easily oxidize or nitridize the surface of a compound semiconductor, one must instead deposit a dielectric. In general, deposited dielectrics do not form a strong bond to the semiconductor material. This means that there are numerous dangling bonds that can lead to interface traps. A second interface can be problematic as well. Traps in the epitaxial region can induce a collapse through a threshold voltage shift. In order to create a high electron mobility transistor (HEMT), engineers grow aluminum gallium nitride (AlGaN) layers on the GaN to produce a quantum well, or channel that facilitates electron flow in the device. Like the deposited dielectric, this deposited semiconductor layer can have numerous dangling bonds due to processing and lattice mismatch effects. These dangling bonds can create traps which affect the threshold voltage, which in turn affects the current through the device.

To correct these problems, process engineers work to minimize trapping effects by ensuring optimal bonding conditions between the epitaxial layer and the substrate, and the semiconductor material and

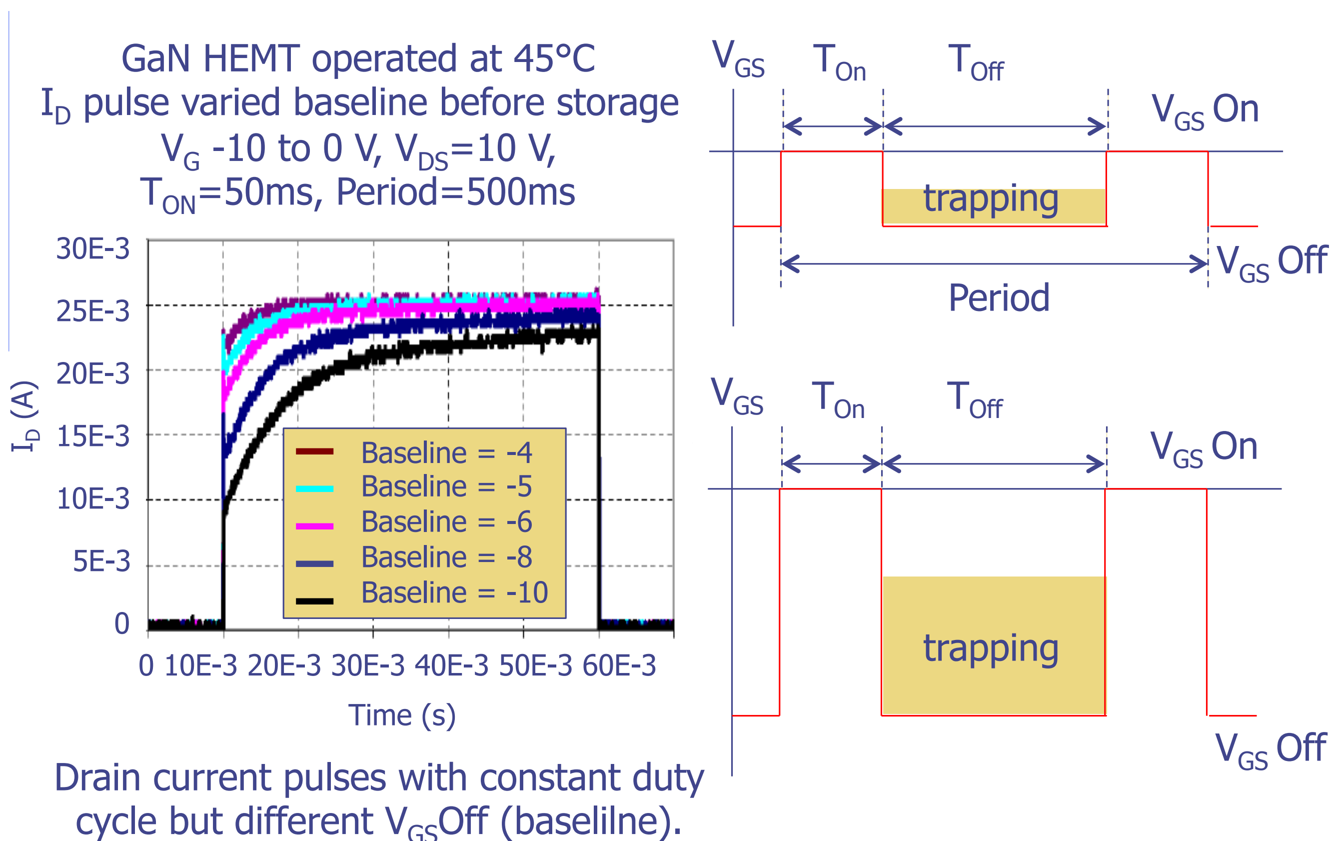


Figure 2

the dielectric. Process engineers experiment with temperature, pressure, growth rates, and other variables associated with Chemical Vapor Deposition to minimize the problem. This can help to minimize this parasitic effect. Another way to minimize the effect is to use a silicon nitride passivation layer. Silicon nitride has the advantage of containing nitrogen like the GaN and AlGaN layers, which leads to fewer dangling bonds.

Ask the Experts

Q: Currently, I have an issue with a BJT IC that failed after reliability. The failures recovered after we subjected them to baking. We did put these devices back into the chamber in the hope of simulating the failure again. But no failures were detected. You can say that baking has irreversible effect on these devices.
Do you think this is a case of surface charge? How can I confirm further if surface charge is the cause here.
Hope you can spare some time to help me with this issue.
Thanks a lot for your help.

A: It could still be a charge-related problem, but the charge may not have occurred in a way that a burn-in could activate. For example, an overstress event that avalanches the collector-base or emitter-base junction can sometimes place charge on a junction. If the bias is correct during the test, or if the overstress event occurred at the end of the reliability test during the electrical testing, then the charge might be present during the test. If you then did a bake, you would re-distribute the charge and make the leakage go away. If you put the devices back in the chamber, but there was no overstress event, there would not be any failures.

Examining the I-V curves and a schematic of the bias in the reliability test would also be a useful thing to do. It might give you some insight into where the overstress might have originated and how it might have been detected at electrical test.

Spotlight on our Courses: Wafer Fab Processing

This month we are highlighting our upcoming Wafer Fab Processing Course in San Jose in March. Our Wafer Fab Processing Expert, Jim Fraser, provides keen insight into current issues as well as explaining concepts to personnel who might be new to the field. You can register for this course on our web site (http://www.semitracks.com/index.php/en/courses/public-courses/processing/wafer-fab-processing).

Overview

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. *Wafer Fab Processing* is a four-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

Outline

Module 1: Basics & Fundamentals; Semiconductor Devices and ICs

Acronyms
Common Terminology
Brief History
Semiconductor Materials
Electrical Conductivity
Semiconductor Devices
Classification of ICs & IC Processes
Integrated Circuit Types
The Global Market for Semiconductors
Other Microelectronics Sectors

Module 2: Crystallinity, Crystal Defects, Crystal Growth

Crystallinity
Crystal Defects
Crystal Growth
Controlling Crystal Defects

Module 3: Basic CMOS Process Flow

Basic CMOS Process Flow
- Device Isolation
- Well Formation
- Gate Formation
- Source/Drain Formation
- Contact Formation
- Metal-1 Interconnect
- Metal-2 Interconnect
- Passivation and Bond Pads
- Parametric Testing

Process Evolution
Shallow Trench Isolation (STI)

Module 4: Ion Implantation 1 (The Science)

Doping Basics
Ion Implantation Basics
Dopant Profiles
Crystal Damage & Annealing

Module 5: Ion Implantation 2 (Equipment, Process Issues)
Equipment
Process Challenges
Process Monitoring & Characterization
New Techniques

Module 6: Thermal Processing
Overview of Thermal Processing
Process Applications of SiO2
Thermal Oxidation
Thermal Oxidation Reaction Kinetics
Oxide Quality
Atomistic Models of Thermal Diffusion
Thermal Diffusion Kinetics
Thermal Annealing
Thermal Processing Hardware
Process Control

Module 7: Contamination Monitoring and Control
Contamination Forms & Effects
Contamination Sources & Control
Contamination Characterization & Measurement

Module 8: Wafer Cleaning
Wafer Cleaning Strategies
Chemical Cleaning
Mechanical Cleaning

Module 9: Vacuum, Thin Film, & Plasma Basics
Vacuum Basics
Thin Film Basics
Plasma Basics

Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
CVD Basics
LPCVD Films
LPCVD Equipment
Epi Basics
Epi Process Applications
Epi Deposition Process
Epi Deposition Equipment

Module 11: PVD
PVD (Physical Vapor Deposition) Basics
Sputter Deposition Process
Sputter Deposition Equipment
Al-Based Films
Step Coverage and Contact/Via Hole Filling
Metal Film Evaluation

Module 12: Lithography 1 (Photoresist Processing)
Basic Lithography Process
Photoresist Materials
Photoresist Process Flow
Photoresist Processing Systems

Module 13: Lithography 2 (Image Formation)
Basic Optics
Imaging
Equipment Overview
Actinic Illumination
Exposure Tools

Module 14: Lithography 3 (Registration, Photomasks, RETs)
Registration
Photomasks
Resolution Enhancement Techniques
The Evolution of Optical Lithography

Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
Etch Basics
Etch Terminology
Wet Etch Overview
Wet Etch Chemistries
Types of Dry Etch Processes
Physics & Chemistry of Plasma Etching

Module 16: Etch 2 (Dry Etch Applications and Equipment)
Dry Etch Applications
- SiO2
- Polysilicon
- Al & Al Alloys
- Photoresist Strip
- Silicon Nitride

Dry Etch Equipment
- Batch Etchers
- Single Wafer Etchers
- Endpoint Detection
- Wafer Chucks

Module 17: CVD 2 (PECVD)
CVD Basics
PECVD Equipment
CVD Films
Step Coverage

Module 18: CMP
Planarization Basics
CMP Basics
CMP Processes
Process Challenges
Equipment
Process Control

Module 19: Copper Interconnect, Low-k Dielectrics
Limitations of “Conventional” Interconnect
Copper Interconnect
Cu Electroplating
Damascene Structures
Low-k IMDs
Cleaning Cu and low-k IMDs

Module 20: Leading Edge Technologies & Techniques
Process Evolution
Atomic Layer Deposition (ALD)
High-k Gate and Capacitor Dielectrics
Ni Silicide Contacts
Metal Gates
Silicon on Insulator (SOI) Technology
Strained Silicon
Hard Mask Trim Etch
New Doping Techniques
New Annealing Techniques
Other New Techniques
Summary of Industry Trends

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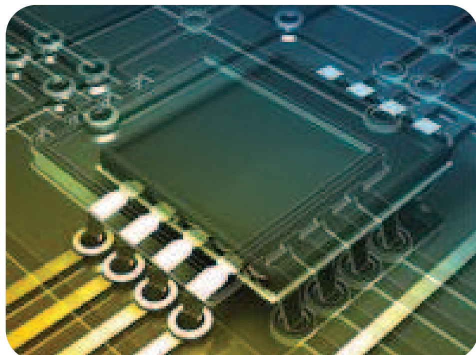

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
March 12 – 14, 2012 (Mon. – Wed.)
San Jose, CA, USA

Wafer Fab Processing
March 12 – 15, 2012 (Mon. – Thurs.)
San Jose, CA, USA

Failure and Yield Analysis
April 9 – 11, 2012 (Tues. – Fri.)
Singapore

EOS, ESD and How to Differentiate
April 12 – 13, 2012 (Thurs. – Fri.)
Malaysia

ESD Design and Technology
April 22 – 24, 2012 (Sun. – Tues.)
Tel Aviv, Israel

Failure and Yield Analysis
April 22 – 25, 2012 (Sun. – Wed.)
Tel Aviv, Israel

Failure and Yield Analysis
May 7 – 10, 2012 (Mon. – Thurs.)
Munich, Germany

Copper Wire Bonding
May 7 – 8, 2012 (Mon. – Tues.)
Munich, Germany

Semiconductor Reliability
May 14 – 16, 2012 (Mon. – Wed.)
Munich, Germany