Issue 19 January 2011

InfoTracks

Semitracks Monthly Newsletter

Upcoming Failure Analysis Course

Millions of dollars wasted… Lost competitive advantage… Idle manufacturing lines and customer frustrations…

These are the all-too-common consequences of semiconductor failures.

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Future Memories – Part 1: Phase Change Memory

By Christopher Henderson

This article is the first in a series of articles on new memory technology. As we quick approach the limits of scaling in traditional DRAM and Flash memories, new memory technologies will be needed if we wish to continue creating smaller, more feature-rich electronics. In this first segment, we will discuss Phase Change Memory. In future issues we will also cover resistive RAM, several quantum magnetic devices, carbon nanotubes, and molecular memories.

One of the big problems with scaling today's flash and DRAM memories further is the limit on charge storage. Cell sizes are approaching the point where the amount of charge stored in a single DRAM or Flash memory cell is down into the thousands of electrons. At this level, leakage, process variation, variation in the application, retention times, and a host of other variables become problematic. These problems will likely limit future scaling below 20nm. There are several technologies that have the potential to permit scaling beyond this point. We will discuss one of the leading ones, Phase Change Memory, in this issue.

Phase Change Memory is one of the most developed replacement technologies. There are actually production devices on the market from companies like Micron (formerly Numonyx), and Macronix. Phase-change memory is a type of non-volatile computer memory. It is also known as PCM, PRAM, PCRAM, Ovonic Unified Memory, and C-RAM. Phase change memory uses the unique behavior of a chalcogenide glass. With the application of heat produced by the passage on an electric current, this material can be "switched" between two states, crystalline and amorphous. Table 1 shows some of the properties associated with the chacogenide structure. Recent versions can achieve two

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(continued)

additional distinct states, effectively doubling its storage capacity. Phase change RAM is one of a number of new memory technologies competing in the non-volatile role with the almost universal Flash memory. Examples of such phase change materials are GeSbTe and AgInSbTe. Micron in particular uses $Ge_2Sb_2Te_5$ for its phase change memory devices.

Figure 1 shows the cross section cutaway of a phase change memory cell. In this technology developed by IBM and Macronix, the cell uses a common source line for the transistors associated with the two cells. The word line forms the gate connection for the transistor, and the drain connects to the chalcogenide material. The bit line runs perpendicular above the cell, and is used to program the cell by changing the state of the chalogenide material from polycrystalline to amorphous, or vice versa. The smaller the chalogenide bridge is, the less current required to program the cell.

Phase change memory requires high programming current densities, which is a distinct drawback. To program the cell, current densities of greater than 10^7 A/cm² (compared to 10^5-10^6 A/cm² for a typical flash memory cell) are required. This has led to active regions which are much smaller than the driving transistor area. The discrepancy has forced the manufacturers to package the heater and sometimes the phase-change material itself in sublithographic dimensions. This results in additional expensive processing, which is a cost disadvantage compared to Flash.

The contact between the hot phase-change region and the adjacent dielectric is another fundamental concern. The dielectric may begin to leak current at higher temperature, or may lose adhesion when expanding at a different rate from the phase-change material. Phase-change memory is susceptible to a fundamental tradeoff of unintended vs. intended phase-change. This stems primarily from the fact that phase-change is a thermally driven process rather than an electronic process. The thermal conditions that allow for fast crystallization should not be too similar to standby conditions, e.g. room temperature. Otherwise data retention cannot be sustained. With the proper activation energy for crystallization it is possible to have fast crystallization at programming conditions while having very slow crystallization at normal conditions. Probably the biggest challenge for phase change memory is its long-term resistance and threshold voltage drift. The resistance of the amorphous state slowly increases according to a power law, which goes by approximately $t^{0.07}$ (see Figure 2). This severely limits the ability for multilevel operation (a lower intermediate state would be confused with a higher intermediate state at a later time) and could also jeopardize standard two-state operation if the threshold voltage increases beyond the design value.

Structure	Sample	Properties
Amorphous		Short range atomic order High reflectivity High resistivity
Polycrystalline		Long range atomic order Low reflectivity Low resistance

Table 1 – Phase Change Memory (PCM) Properties

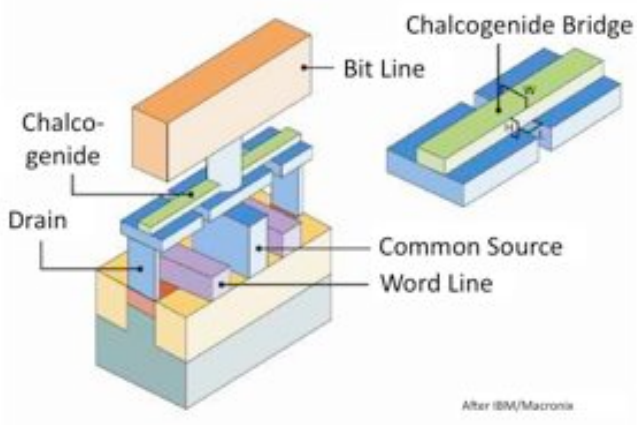
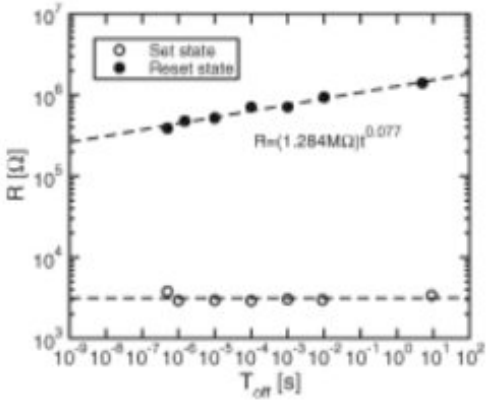


Figure 1 – Cross section cutaway of a Phase Change Memory Cell. 2 cells are shown in the drawing at the left.



D. Ielmini et. al., Trans. Elec. Dev., Vol.54, No. 2, pp. 308-315, 2007.

Figure 2 - Graph showing resistance increase as a function of time in a Phase Change Memory cell.

Ask the Experts

Q: What is the difference between troubleshooting and failure analysis?

A: Troubleshooting and failure analysis have quite a bit of overlap in the semiconductor industry. Troubleshooting usually refers to the process of localizing the problem, whether that be on a chip, inside an electronic component, or within a system. Troubleshooting normally implies finding the problem, and potentially fixing or replacing the component with the problem. As such, we normally think of troubleshooting without regards to fixing the underlying cause. Failure analysis is usually a defined (quite often required) activity that involves not only troubleshooting, but investigation into the root cause of a problem as well as development of a corrective action. Therefore, in failure analysis, we work to fix the underlying cause.

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We look forward to hearing from you!

Course Spotlight: Failure Analysis

February 28-March 3, 2011
San Jose, CA, USA

In today's economy, competent failure analysts are vital to solve these problems before their companies suffer the repercussions. However, as circuits grow more and more complicated, engineers can easily find themselves entangled in a semiconductor "labyrinth"--searching for a microscopic failure among millions of transistors. With the wide spectrum of available analysis tools and the ever-decreasing probability of defect discovery, failure analysis can quickly become overwhelming even for the experienced analyst.

The solution: Failure and Yield Analysis, a multi-day course that covers effective analysis tools and presents systematic process flows that simplify defect localization and characterization. By focusing on a "Do it Right the First Time" approach, the class will give you the appropriate methodology to successfully locate and characterize defects to determine the root cause of failure.

Learn more about this course at:
http://www.semitracks.com/index.php/courses/public-courses/analysis/failure-and-yield-analysis

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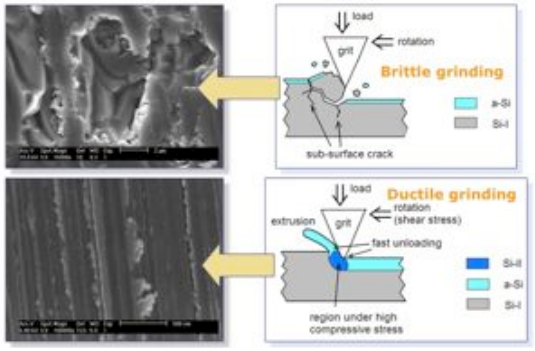
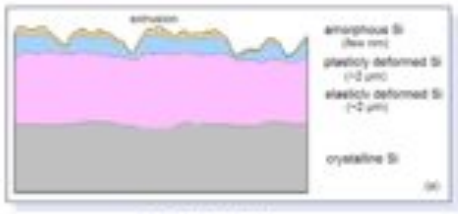
Technical Tidbit - Backgrinding

Wafer backgrinding is a common technique to thin dice for packaging in thin profile applications. Understanding the behavior of silicon during backgrinding is important to achieve success. Generally speaking, silicon is a brittle material, breaking with sharp edges and cracks (similar to glass). However, Si-II (pronounced "silicon-two") has lower yield strength, which is relatively easily deformed with better elongation. This is similar to most metals. For reference, Si-II is a work-hardened phase of silicon, where the stress-strain curve of the material changes somewhat from unworked crystalline silicon, or Si-I (pronounced "silicon-one"). So based on the morphology, a ductile grinding mechanism is dominant in poligrinding. It is preferred as well for rough grinding, it is a mixed mechanism of ductile and brittle grinding. This generates amorphous silicon, or a-Si upon interaction.

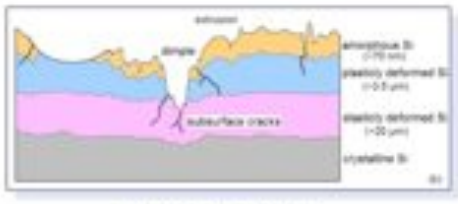


These two images show the results of brittle grinding and ductile grinding. Notice the chunks of material that have been ripped out due to brittle grinding. Ductile grinding tends to leave gouges in the material with extruded material immediately adjacent to the trench.

Poligrinding and rough grinding show multi-layer damage structures, which is the result of ductile grinding. The images on the right show the damage that occurs with both techniques. Notice the amorphous silicon layer in gold, the plastically deformed layer in cyan, the elastically deformed layer in magenta, and the undisturbed crystalline silicon in gray. Due to difference in load pressures, each layer in rough grinding samples is thicker than its counterpart in poligrinding samples. In rough grinding samples, dimples and sub-surface cracks caused by brittle grinding are irregularly distributed.



Poligrinding



Rough grinding

To summarize the grinding process for wafer thinning, there are two identifiable mechanisms: ductile and brittle grinding. In poligrinding, the ductile mechanism is dominant and in rough grinding, both ductile and brittle grinding occur. Both grinding processes create damage that extends for some distance into the silicon. The rough grinding process produces a damage layer of amorphous silicon that is about 70 nanometers thick, a plastically deformed layer of about 3.5 microns, and a stressed region of about 20 microns. Poligrinding generates much less stress. The amorphous silicon layer is only a few nanometers thick, and the plastically deformed and stressed layers are each approximately 2 microns thick.

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January 30-February 1, 2011 - Tel Aviv, Israel

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