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InfoTracks

Semitracks Monthly Newsletter

MEMS Die Attach Issues

By Christopher Henderson

This month, we will begin a new series of Feature Articles that will cover issues related to die attach for MEMS devices. We don't want the die attach material or outgas byproducts to contaminate the MEMS structures causing them to malfunction. This month's article covers the die attach process itself. Since MEMS devices can contain freely moving structures, the die attach process is critical.

Let's begin with a review of the MEMS die attach and wirebond process. We show the basic flow for the assembly process in Figure 1. Even though die attach and wirebond are two individual unit processes in the packaging flow, die attach is usually immediately followed by wirebond. After MEMS wafer fabrication and release, one can then begin the packaging process. This starts with wafer probe testing, followed by inspection, dicing, and a second inspection step. After die attach and wirebond, there is a third optical inspection step, followed by lid attach or seal, or mold injection. This is followed by marking, lead or ball attach, and a final functional test. In the die attach process, engineers typically use a silver-filled epoxy, since it is an inexpensive process. Another option is to use a solder die attach. A solder die attach works well for thermal and hermetic applications.

In this Issue:

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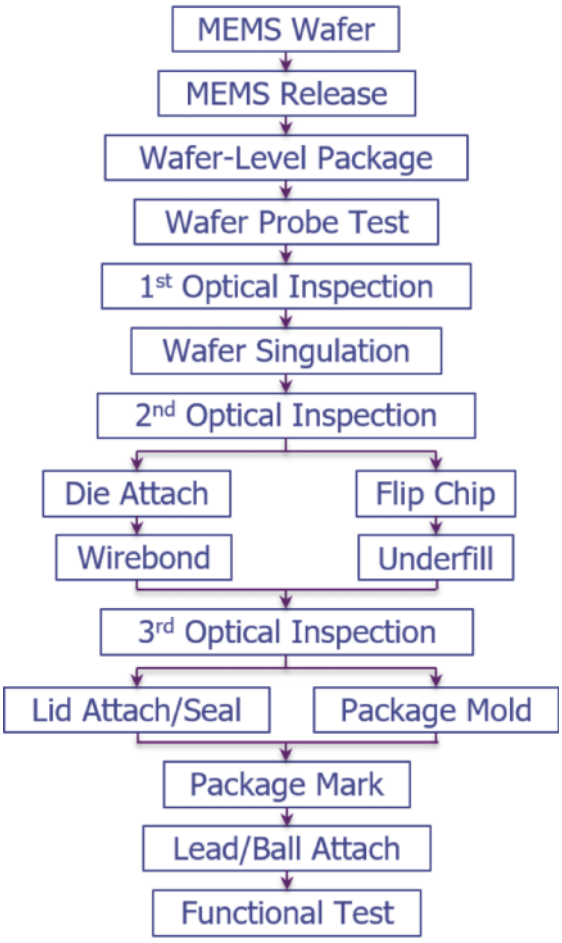


Figure 1. MEMS Assembly and Packaging Process Flow.

Die attach is the method used to attach a MEMS device to a package, and is a general technology applicable to most integrated circuit devices. Presently, MEMS packages use solders, adhesives or epoxies for die attach, and each method has advantages and disadvantages that affect the overall MEMS reliability. We will discuss the materials in further detail in the second part of this series.

Die attach serves several critical functions. First, the main function is to provide good mechanical attachment of the MEMS structure to the package base. This ensures that the MEMS chip (or die) does not move relative to the package base. Second, it must survive hot and cold temperatures, moisture, shock and vibration. Third, the attachment may also be required to provide a good thermal path between the MEMS structure and the package base. Should heat be generated by the MEMS structure or by the support circuitry, the attachment material should be able to conduct the heat from the chip to the package base. The heat can be conducted away from the chip and 'spread' to the package base which is larger in size and has more thermal mass. This spreading can keep the device operating in the desired temperature range. If the support circuitry requires good electrical contact from the silicon die to the package base, the attachment material should be able to accommodate the task. Stability and reliability of the attach material is largely dictated by the material's ability to withstand thermomechanical stresses created by

differences in the Coefficient of Thermal Expansion (CTE) between the MEMS silicon die and the package base material. These stresses are concentrated at the interface between MEMS silicon backside and attach material and at the interface between die attach material and package base.

Silicon has a CTE between 2 and 3 parts per million per degree centigrade, while most package bases have a higher CTE of 6 to 20 parts per million per degree centigrade. Equation 1 below shows the Coffin-Manson relationship that includes a strain component.

$$N_f \propto \gamma^m \left(\frac{2 * t}{L * \Delta CTE * \Delta T} \right)$$

Equation 1. The Coffin-Manson equation that includes strain.

N_f is the number of cycles to failure, γ is the shear strain, m is a material constant, L is the diagonal length of the die, T is the die-attach material thickness, ΔCTE is the difference between the MEMS CTE and substrate CTE, and ΔT is the change in temperature.

There are some important factors to consider in MEMS die attach. The first issue is stress. We should note that MEMS devices are very sensitive to die stress. The pick, alignment, and dispensing processes, as well as the curing process, are critical and affect the stress in the device. If the pick-and-place tool exerts too much stress on the MEMS structure, it can be damaged. If the MEMS die is not aligned properly in the package, the die attach coverage will not be uniform, leading to areas of increased stress. If the dispense process does not uniformly dispense the die attach, or does not create a uniform fillet at the edge of the die, the stress levels will be elevated. We show the pick, alignment, and dispensing equipment in Figure 2.

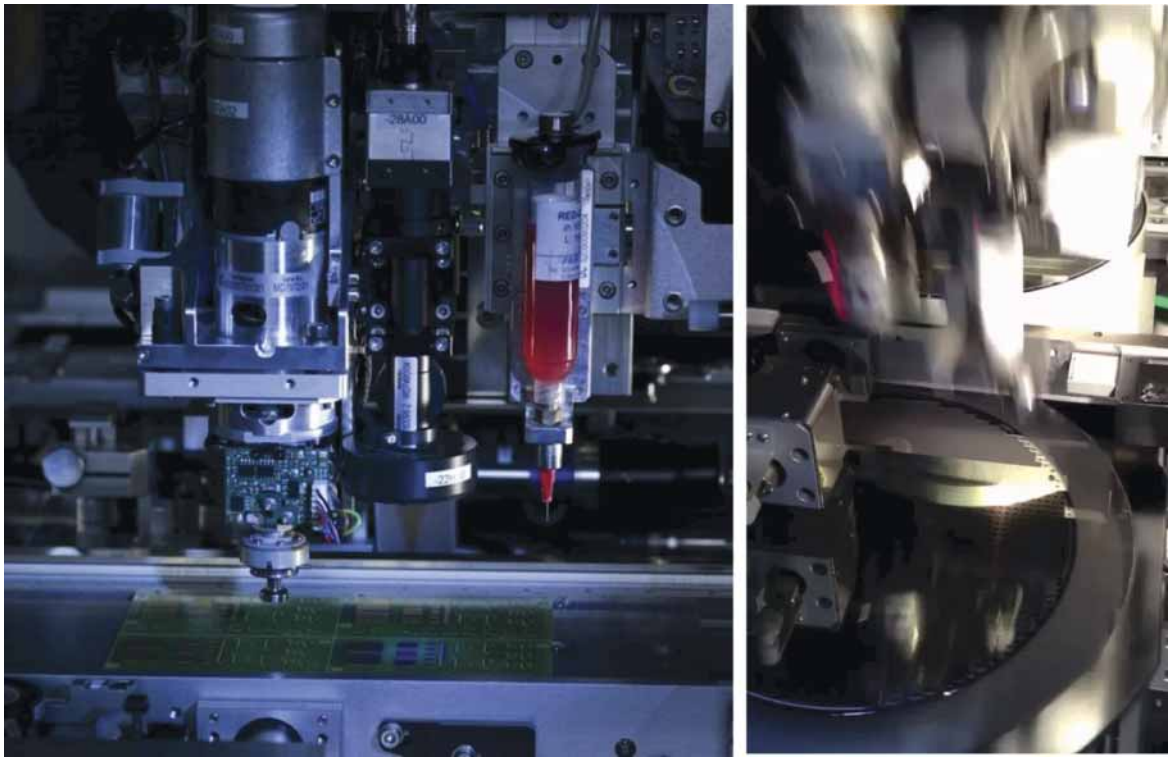


Figure 2. Pick, dispense, and align equipment used for die attach.

A second issue is voiding. Voids in the die attach material can cause areas of localized stress concentration that can lead to premature delamination. Voids can be caused by irregularities in the die attach dispense process. They can be caused by contamination on the back side of the die or the die package, preventing the adhesion of the die attach. They can also be caused by trapped gases that are unable to escape during the curing process.

A third issue is handling the MEMS device during die attach. One of the big difficulties with MEMS devices and die attach is that the MEMS topside is often too fragile to be touched by die pick up tools. However, Wafer Level Packaging does allow the MEMS die to be picked up like an integrated circuit. Equipment picks the die from dicing tape or from a waffle pack. One of the areas of concern for MEMS devices is the ejector pins that lift the device off of the tape. One method of reducing die pickup issues is to use a pyramid collet. The collet places the stress at the edge of the die, away from the sensitive MEMS structures. We show examples of MEMS collets in Figure 3.

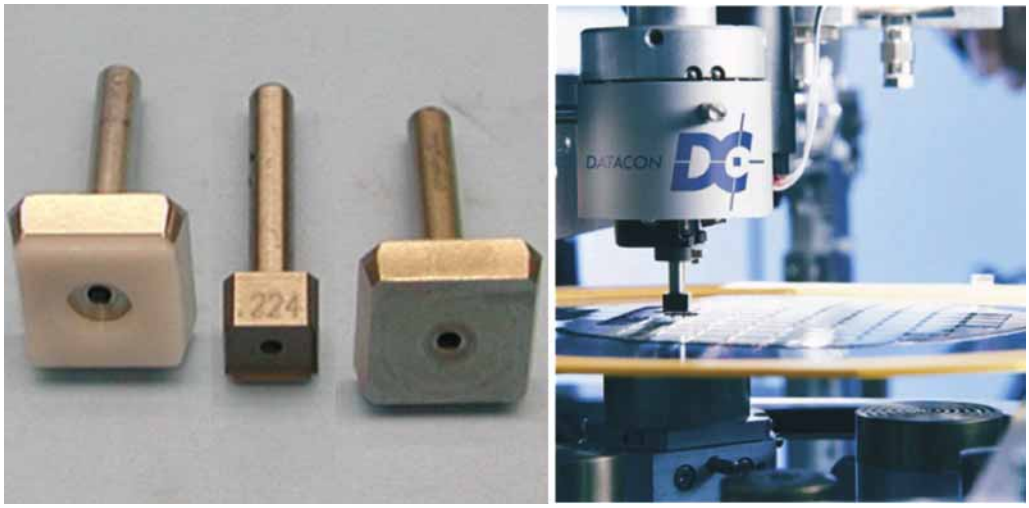


Figure 3. Collets for MEMS die handling.

In Figure 4, we show the process steps for how a collet can work for the pick-and-place operation with MEMS devices.

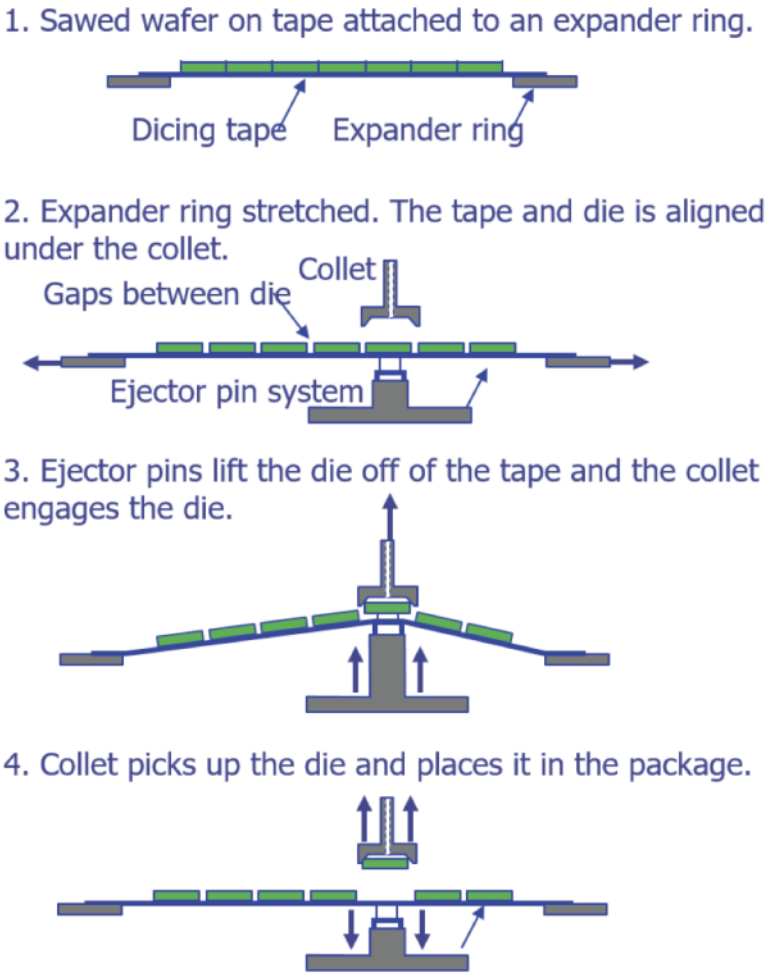


Figure 4. Diagram showing process for using a MEMS collet.

Some other options for die pickup are custom sidewall grip tools, like we show in Figure 5. In this configuration, ejector pins push the die up, while custom sidewall grip tools grab and hold the die during the lifting and placing process. The biggest problem with this approach is yield loss from sidewall chipping of the MEMS die.

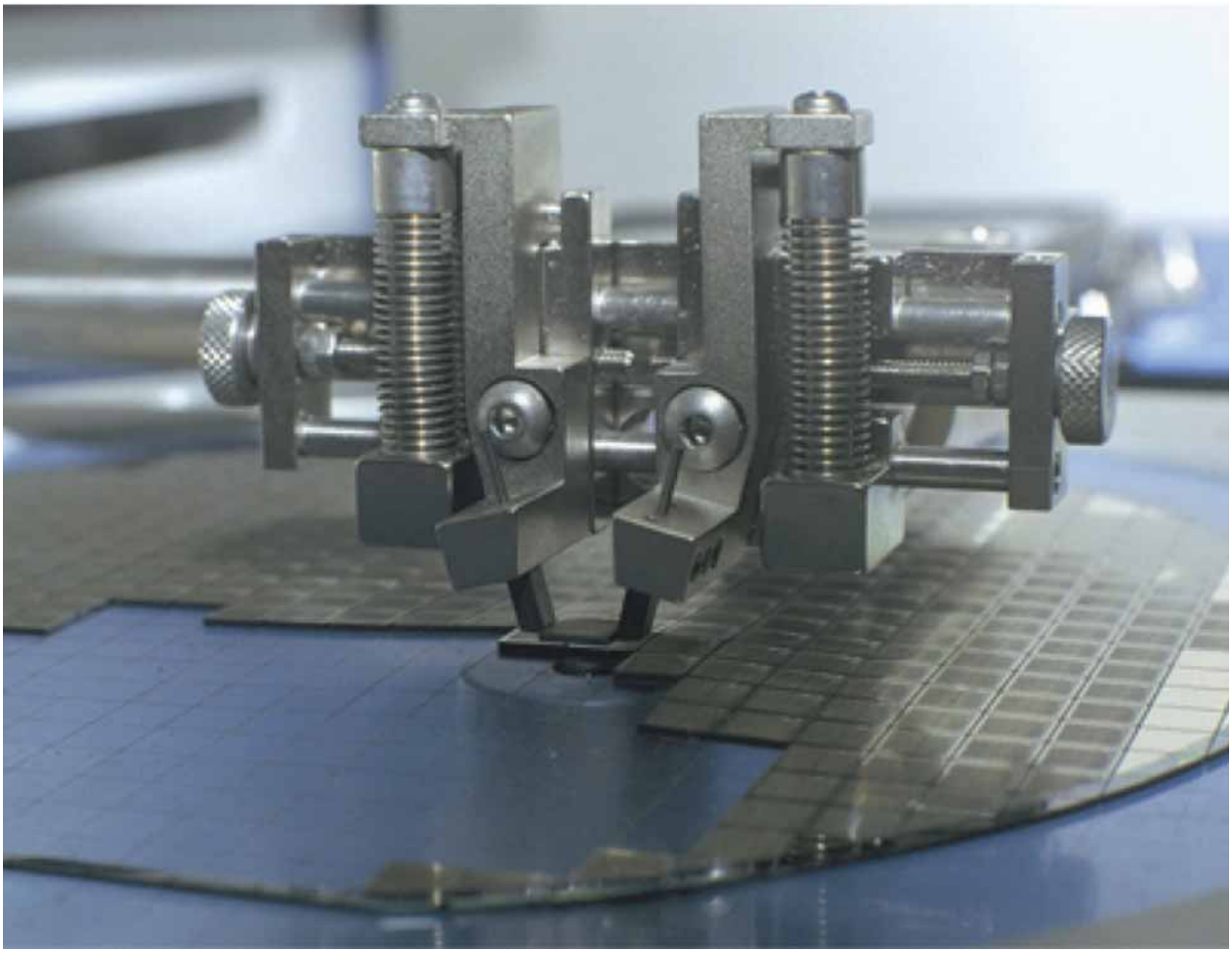


Figure 5. Custom die gripping tool for MEMS die pick and place.

In next month's Feature Article, we will discuss issues with the die attach materials themselves.

Technical Tidbit

Bench to ATE Correlation

This month's Technical Tidbit covers Bench to Automatic Test Equipment, or ATE, correlation. An important consideration is correlation between lab bench results and Automated Test Equipment (ATE) results. Once in production, the parts will be tested on ATE, but the parts need to work in real-world applications. This is where bench testing comes into play. A bench setup can be made to more closely match the system configuration. The results between ATE and bench testing need to correlate. In production test, we normally just get a single value for a parameter, whereas with bench testing, we typically look at waveform results for anomalies. If there are differences, they need to be resolved before finalizing the datasheet limits. Examples of issues might include glitches, spikes, ramp times, or other phenomena that may only be seen in waveform data.

Here is an example. Figure 1 shows waveform results from bench testing for two different integrated circuits. Let's assume that the ATE system measures the parameter Vout_V at 0.005 seconds, denoted by the green arrows. If this is the case, then both devices are passing the ATE tests. However, notice the difference between the Vout_V waveforms for both devices. In the time interval from 0 to 0.003 seconds, the waveforms are noticeably different from one another, denoted by the red boxes. According to the ATE data, these devices would be good to ship, but there are significant differences in the waveforms that could impact the operation of the system into which these integrated circuits might go. One needs to ask, is this a problem? If it is a problem, then we need to determine how to resolve it. This requires collaboration with the customer to ensure the component will work properly, and then additional work to ensure that the ATE tests can detect these differences, if they are important to the operation in the customer's application.

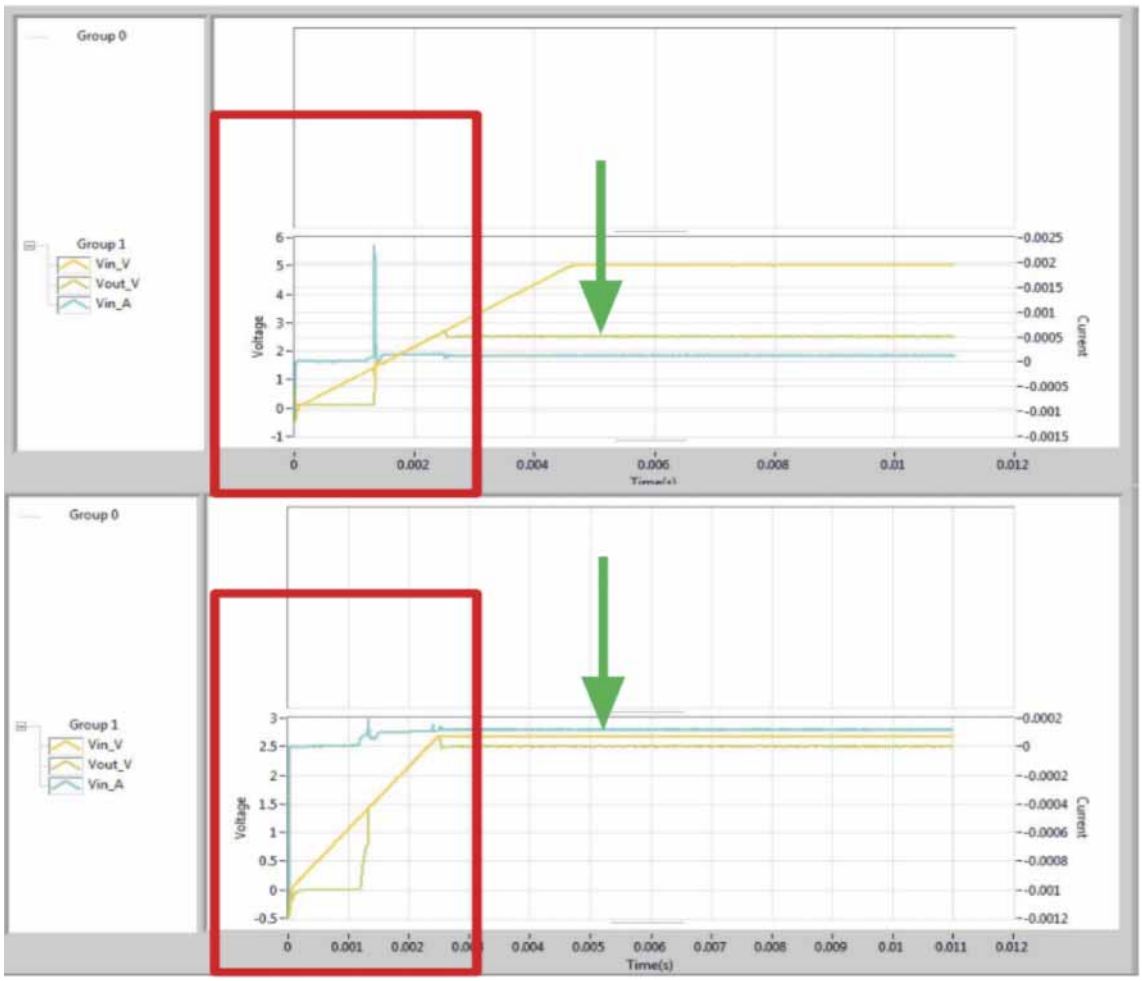


Figure 1. Bench Testing Waveforms.

Ask the Experts

Q: When evaluating failed bond wires in a plastic packaged IC, does the decapsulation process affect the evaluation?

A: It certainly can. The chemicals used to remove the plastic package material can attack or etch aluminum as well as copper. Therefore, it might be necessary to use a Laser Decapsulation method or Oxygen Plasma Ashing Decapsulation method.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

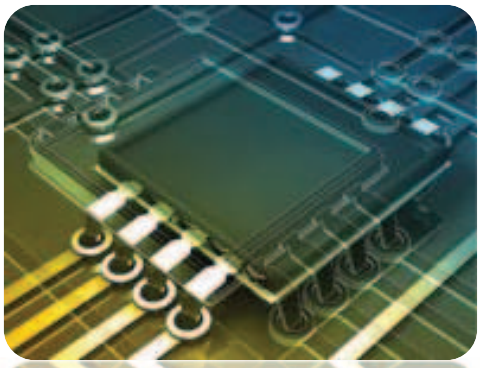
One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques

7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS

14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
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Upcoming Webinars

(Click on each item for details)

Wafer Fab Processing WEBINAR

4 sessions of 4 hours each
US: February 28 – March 3, 2022
(Mon – Thur), 11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 noon PST

Semiconductor Reliability / Product Qualification WEBINAR

4 sessions of 4 hours each
US: March 7 – 10, 2022 (Mon – Thur),
7:00 A.M. – 11:00 A.M. EST;
1:00 P.M. – 5:00 P.M. CET

Failure and Yield Analysis WEBINAR

4 sessions of 4 hours each
US: April 4 – 7, 2022 (Mon – Thur),
7:00 A.M. – 11:00 A.M. PST,
1:00 P.M. – 5:00 P.M. CET