Issue 140 February 2021

InfoTracks

Semitracks Monthly Newsletter

Resistors

By Christopher Henderson

This month, we will continue our series of Feature Articles by discussing the Chip Resistor.

Chip Resistors are typically packaged in surface mount packages. These resistors contain a thin or thick film. Thick film surface mount resistors might use ruthenium oxide on a ceramic substrate, whereas a thin film resistor might use a nickel chromium alloy (nichrome), or a tantalum oxide, nichrome, tantalum mixture, on a ceramic substrate. These resistors might contain a protective coating, such as an overglaze or polymer coating. Engineers typically trim these resistors to a final resistance value. To connect the resistor into the circuit, the package will include terminations made from solder over nickel, or silver, or some other metal used to interface to the resistor film. Nickel is the best option, as it helps prevent leaching of the interface metal during the soldering operation, which can lead to opens.

Figure 1 shows a cross-section of the surface mount chip resistor. The resistive element sits on a ceramic substrate, with terminations on the end, wrapping around the ceramic substrate and touching the resistive element. There will be a protective overglaze or polymer layer to cover the resistive element.

In this Issue:

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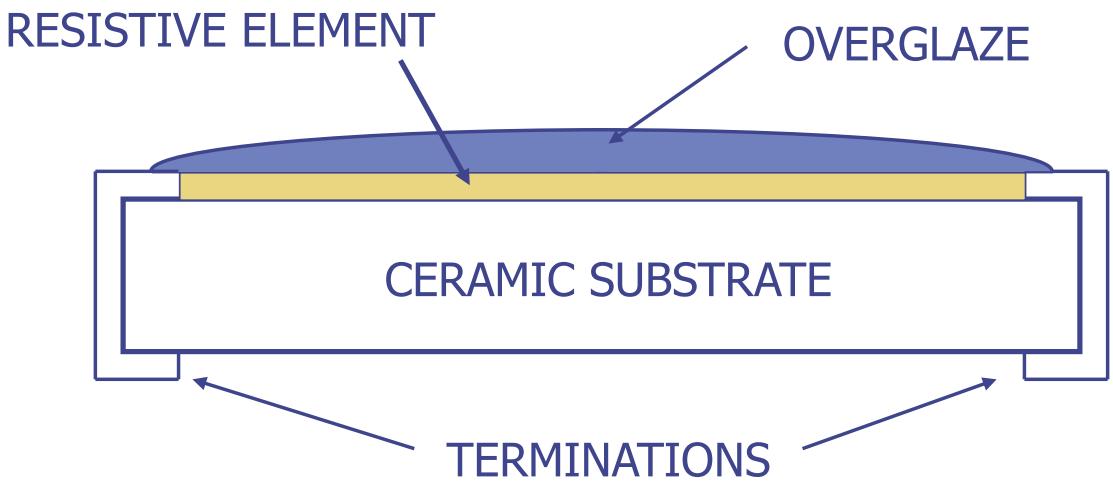
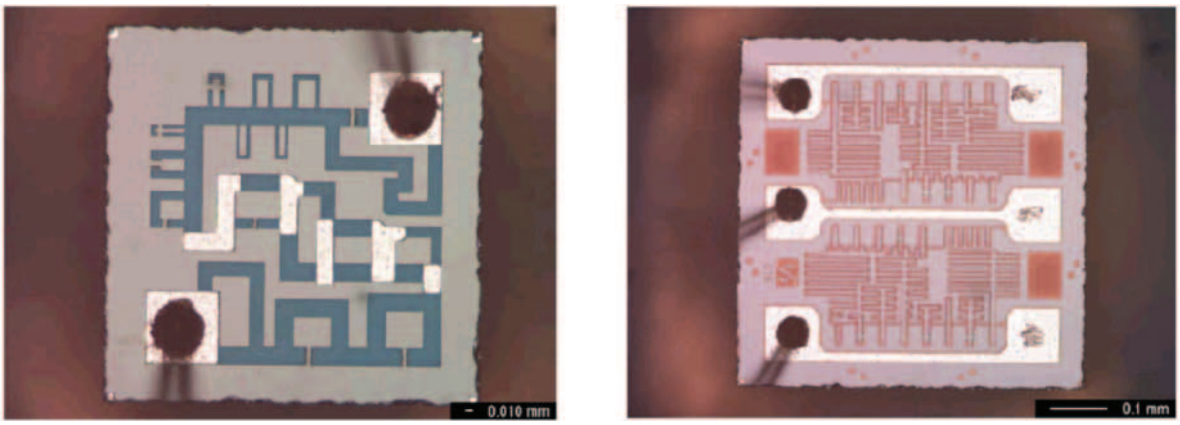


Figure 1. Cross-section of a surface mount chip resistor.

Some typical failure mechanisms for surface mount chip resistors include cracks, electrical overstress (EOS), delamination, and termination damage. Cracks can cause open circuits, and can be due to substrate defects. EOS is a common failure mechanism for almost all components. In chip resistors, it would manifest itself as thermal damage to the protective layer, the resistive element, or possibly, the terminations. Delaminations can occur due to moisture, solder flux, or other chemical processes. Finally, termination damage can occur due to incorrect solder processes, or incorrect termination design.

Chip resistors can also be used in hybrid microcircuits. These resistors can be thin-film on silicon or ceramic substrates, using tantalum nitride or nichrome thin films. Resistors in hybrid microelectronics can also be thick film on ceramic. These thick film resistors can be formed by printing materials directly on the hybrid ceramic substrate.

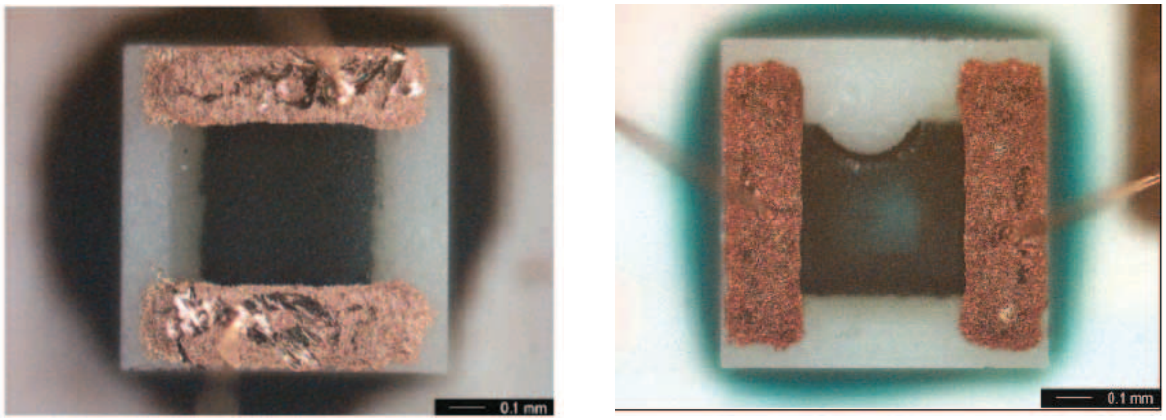
Figures 2 (a) and (b) show examples of hybrid chip resistors. These resistors consist of thin film tantalum nitride on silicon. The tantalum nitride appears as a blue-gray color in Figure 2 (a), and as a red color in Figure 2 (b).



(a) (b)

Figures 2. (a) Hybrid chip resistor with thin film tantalum nitride on silicon, and (b) Hybrid chip resistor with thin film tantalum nitride on silicon.

Figures 3 (a) and (b) are examples of thick film on ceramic hybrid chip resistors. In both figures, the thick film material is visible as a dark gray color.



(a) (b)

Figures 3. (a) Hybrid chip resistor with thick film on ceramic, and
(b) Hybrid chip resistor with thick film on ceramic.

Now we will discuss some typical failure mechanisms associated with hybrid chip resistors. The first is corrosion. Thin film nichrome is very susceptible to corrosion when moisture is present and a bias is applied. This means that circuits containing hybrid chip resistors must be well-protected from moisture. The second is cracking due to substrate defects. This can lead to open circuits in the resistor network. The third is cracking or scratching due to mishandling. Many circuits containing hybrid chip resistors are assembled by hand, so this is a particular concern. The fourth is electrical overstress. Electrical overstress is a common failure mechanism in all electronic systems. One should look for evidence of thermal damage to confirm electrical overstress. The fifth is delamination between layers. This can be due to moisture, solder flux, or other chemicals penetrating into the assembly. The sixth is termination damage due to excessive bonding attempts. The seventh is electrostatic discharge or ESD. Although one would not normally think of a resistor begin susceptible to ESD, arcing can occur between different elements in the array on a thin or thick film resistor network.

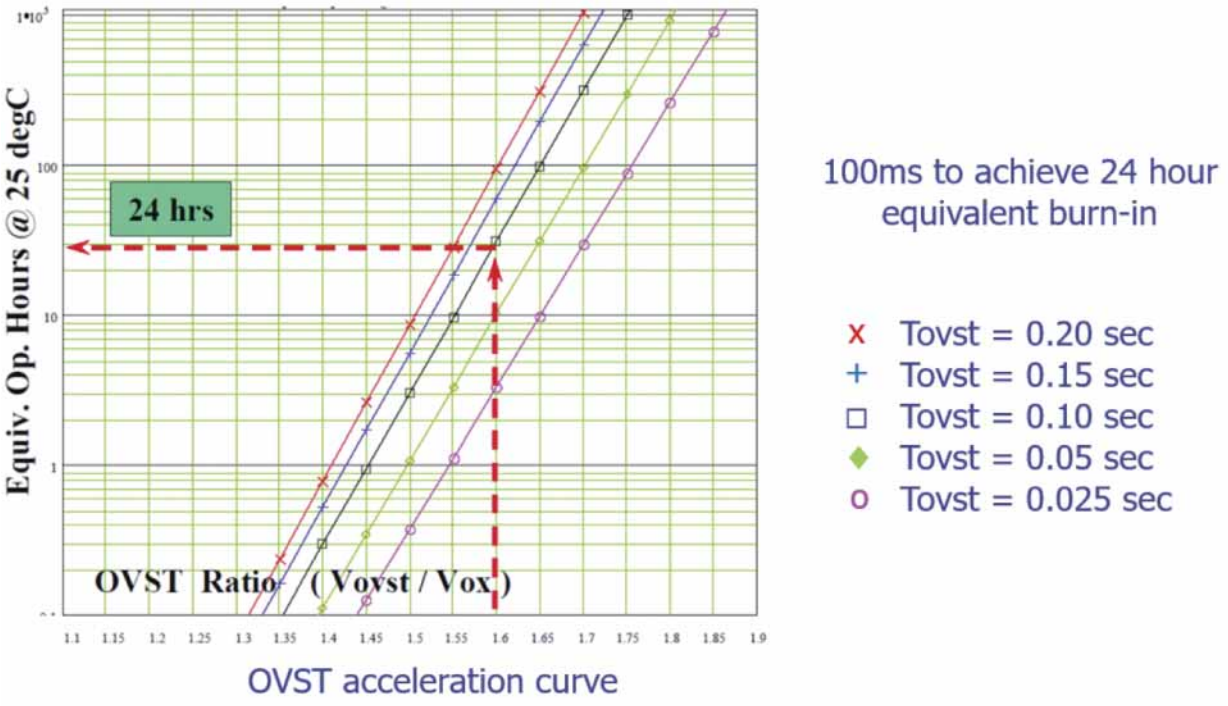
In next month's Feature Article, we will discuss the Wire-Wound Resistor.

Technical Tidbit

OVST Basics

This month's technical tidbit covers Over-Voltage Stress Testing or OVST.

OVST is a necessary test for several reasons. First, it helps reduce Defective Parts Per Million (DPPM) and customer returns due to random defects. Second, it helps to avoid the need for burn-in, due to the fact we can detect the defects upstream during electrical testing. Third, we can get feedback more quickly. OVST can be performed inline in the wafer fab as a probe test, thus providing a shorter loop from probe test to fab, if the defects increase dramatically. OVST is a stress test that accelerates oxide defect failures. Often OVST will be required on devices that have a large gate oxide. For example, an area of greater than 10,000um^2 might require an OVST test. This test provides the equivalent of burn-in without its costs and problems. The target would be to produce the equivalent of 24 hours of stress equivalent to a 25˚C burn-in at the maximum operating voltage. The OVST test sequence is as follows. First, measure the current before stress at the nominal or maximum operating voltage. Next, apply the OVST stress voltage. You can measure the current during the stress, but this would be for information purposes only. Third, measure the current after the stress, using the same conditions as the first step. And fourth, calculate the delta current before and after the stress. It should be, for all intents and purposes, close to zero.

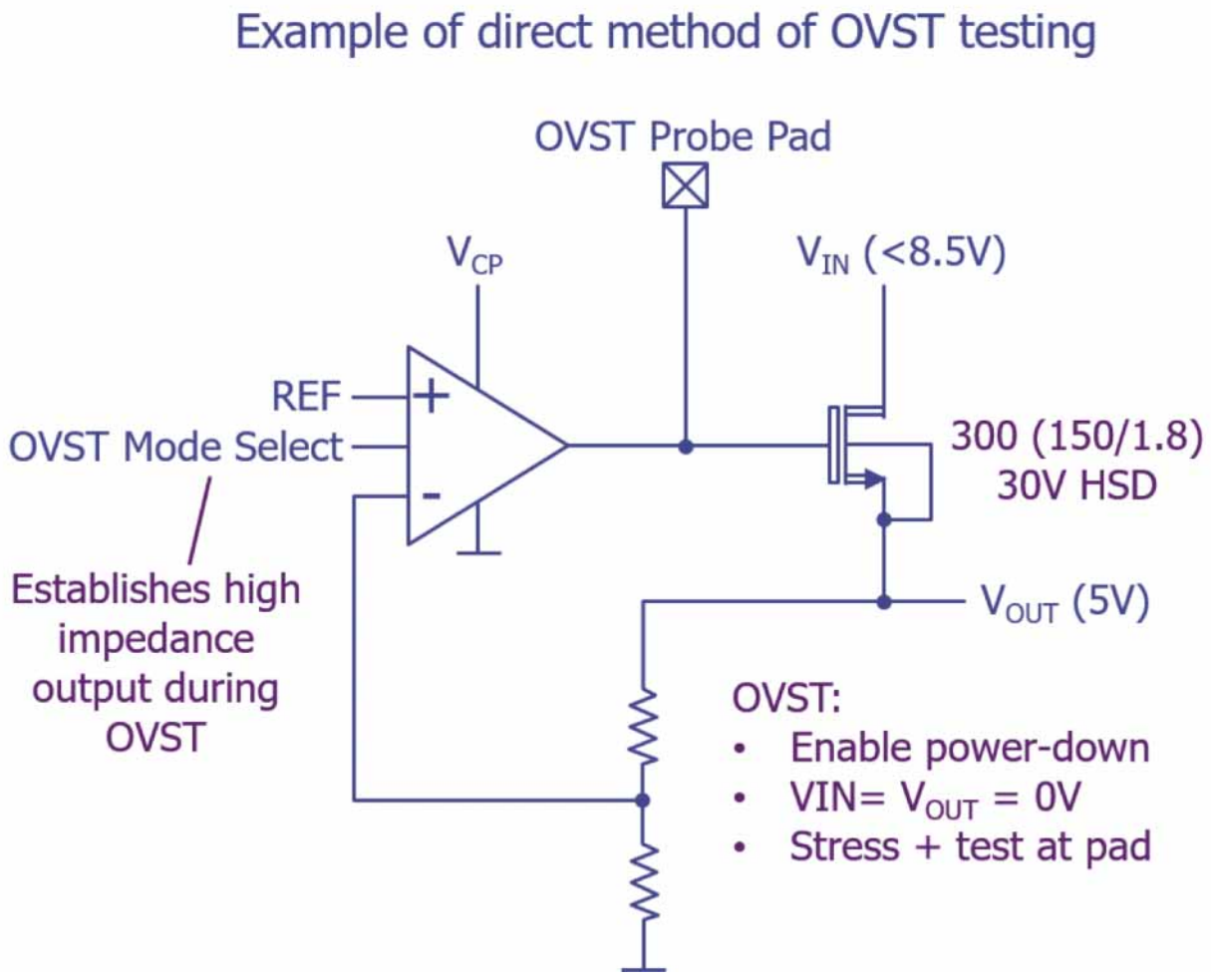


OVST acceleration curve

There is a tradeoff between the ratio of the OVST stress voltage and the test duration. Ideally, it should be equal to the IC's maximum operating voltage to the test time. A typical OVST stress voltage would be 1.6 times the maximum operating voltage for 100msec, and would provide the equivalent of 24 hours of burn-in. The graph shown here depicts the equivalent number of hours versus the voltage acceleration.

When one performs OVST, the circuits need to be in sleep state (current draw should be in the low micro-amp range) and the components should be able to withstand the OVST voltage. Design for OVST testing can be quite challenging. One can implement a direct method (across the DUT) or an indirect

method (accessing the DUT through other devices). Additional probe pads or an OVST test bus may be needed for certain ICs. A bond out option may also be required to implement the test at the package level. One should group devices with similar voltage ratings. You can stress as many of these groups in parallel to save test time. A typical gate oxide short is on the order of a few hundred ohms. Expect nA to mA of leakage current after OVST breakdown. OVST can be implemented in parallel with other tests like digital IDDQ, logic scan, current limit tests, etc. And finally, the OVST current should be simulated during top level design verification by adding a few hundred ohms across the gate oxide.



This circuit diagram shows an example of a direct method of OVST testing. There is an OVST probe pad that connects directly to the gate of the power transistor on the right. There is also an OVST mode select to disable the circuit driving the power transistor so that the OVST test can stress the transistor properly and measure the leakage properly. In conclusion, OVST is a powerful test for eliminating ICs with defective gate oxides from a population to help improve quality levels in products. One must be careful to implement the test properly, which requires coordination with design from the beginning of the IC development project.

Ask the Experts

Q: Customers often ask how long an over-voltage stress test (OVST) should be. What is your recommendation? Is there correlation of voltage time to burn-in time?

A: This is a great question, and it is something that we cover in our Technical Tidbit this month, so please refer to the Technical Tidbit for more details on this.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip

   f. Silicon Nitride
   g. Dry Etch Equipment
   h. Batch Etchers
   i. Single Wafer Etchers
   j. Endpoint Detection
   k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
   a. CVD Basics
   b. PECVD Equipment
   c. CVD Films
   d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
   a. Planarization Basics
   b. CMP Basics
   c. CMP Processes
   d. Process Challenges
   e. Equipment
   f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
   a. Limitations of "Conventional" Interconnect
   b. Copper Interconnect
   c. Cu Electroplating
   d. Damascene Structures
   e. Low-k IMDs
   f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
   a. Process Evolution
   b. Atomic Layer Deposition (ALD)
   c. High-k Gate and Capacitor Dielectrics
   d. Ni Silicide Contacts
   e. Metal Gates

f. Silicon on Insulator (SOI) Technology
g. Strained Silicon
h. Hard Mask Trim Etch
i. New Doping Techniques
j. New Annealing Techniques
k. Other New Techniques
l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
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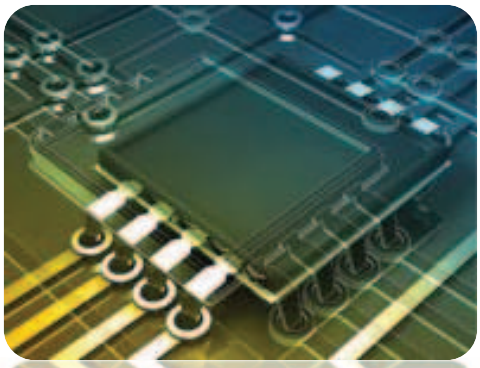

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!

Upcoming Webinars

(Click on each item for details)

Wafer Fab Processing

WEBINAR—4 sessions of 4 hours each
Europe: April 6 – 9, 2021 (Tue – Fri),
1:00 P.M. – 5:00 P.M. CET
US: April 19 – 22 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

IC Packaging Technology

WEBINAR—4 sessions of 4 hours each
Europe: April 19 – 22, 2021 (Mon – Thur),
1:00 P.M. – 5:00 P.M. CET
US: April 12 – 15, 2021 (Mon – Thur),
9:00 A.M. – 1:00 P.M. PST

Advanced CMOS/FinFET Fabrication

WEBINAR—4 sessions of 2 hours each
Europe: April 26 – 29, 2021 (Mon – Thur),
3:00 P.M. – 5:00 P.M. CET
US: April 5 – 8, 2021 (Mon – Thur),
9:00 A.M. – 11:00 A.M. PST