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Chemical Vapor Deposition—Epitaxy Part 1

By Christopher Henderson

In this section we will discuss how process engineers use chemical vapor deposition for epitaxial growth. Engineers will use an epitaxial—or epi—layer in some technologies to provide better control over the performance of the circuit.

We'll begin with basics including definitions and epitaxial growth models. Next we'll discuss applications for epitaxial materials. These include both CMOS and bipolar technologies. We'll spend most of the section discussing the deposition process, including the Deal-Grove model, reaction rates, and dopant introduction. We'll discuss characterization of epitaxial films, and equipment used for epitaxial deposition.

Let's begin by defining some terms. Epitaxy is the chemical vapor deposition process in which one deposits a single-crystal film on the surface of another single-crystal substrate. Most engineers simply refer to this as "epi." An epi layer is therefore a film deposited by epitaxy. There are two types of epitaxy: homoepitaxy and heteroepitaxy. We define homeoepitaxy as an epi film consisting of the same material as the substrate. An example of this would be a silicon epi layer. We define heteroepitaxy as an epi film consisting of a different material than the substrate. An example of this would be SOS, or silicon on sapphire. There are three growth methods for epi layers: solid phase epitaxy, liquid phase epitaxy, and vapor phase epitaxy. We use high-temperature vapor phase epitaxy to produce epi layers on silicon wafers. This

In this Issue:

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provides tight control of film thickness & dopant concentration, low level of contaminants and a high degree of crystal perfection.

Engineers use epitaxial layers for a number of CMOS processes. Typically, this is a thin layer—approximately 2 to 4 microns—of a lightly-doped p-type epi layer grown on a more-heavily doped p+ substrate. We grow this epi layer before any subsequent processing of the wafer. There are a number of device performance benefits associated with the epitaxial layer. One is lower reverse-bias leakage currents. Since the p+ layer has few minority carriers, the diffusion length is small. The minority carriers are generated from only the thin p- layer. Another benefit is improved latch-up performance. Latch-up is caused by turning on the lateral n-p-n-p parasitic transistor between neighboring NMOS and PMOS transistors. The formation of a vertical parasitic p-n-p transistor suppresses this effect. Another benefit is a more reliable transistor gate oxide. Since the presence of oxygen precipitates near the silicon oxide interface degrades the electrical integrity of the gate oxides, the fact that the epi layer is oxygen-free reduces this problem. The final benefit is the fact that the p+ layer getters heavy metals, keeping them away from the active transistor regions.

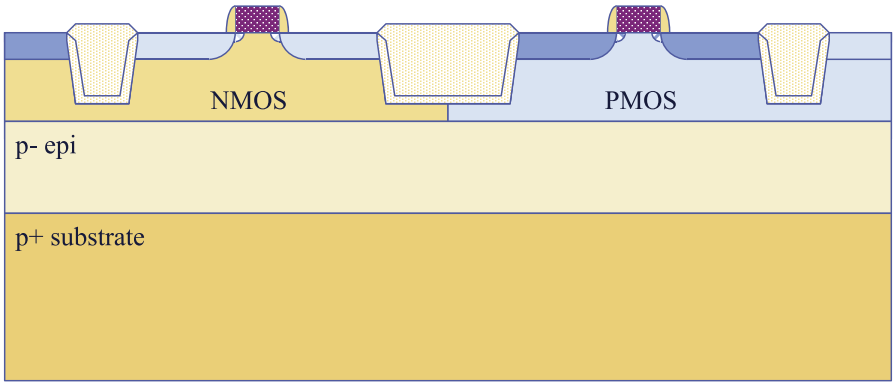


Figure 1. Epi process applications

Figure 1 shows a cross-section image of a twin-well CMOS structure built in a p- epitaxial layer and a p+ substrate. The light tan area between the NMOS and PMOS transistor is a shallow trench isolation structure, which also helps improve transistor performance.

Material	Parameter	CMOS	Bipolar
Epi layer	Conductivity type	p-	n
	Doping concentration (atoms/cm^3)	Low 10^{15}	$10^{15} – 10^{16}$
	Thickness (µm)	2 – 4	1 – 4
Substrate	Conductivity type	p+	p
	Doping concentration (atoms/cm^3)	10^{19}	Low 10^{15}
	Prior processing	none	n+ BL

Figure 2. Epi process applications—bipolar

Process engineers also use epitaxial layers for bipolar and BiCMOS processes. One can grow a lightly-doped n-type epitaxial layer over a patterned, heavily doped diffused layer to produce a structure known as a buried layer. This structure helps to increase the breakdown voltage of the collector-base junction while maintaining a low collector resistance. Figure 2 shows example parameters for epitaxial layers and substrate layers, and how they're used in both CMOS and bipolar processes.

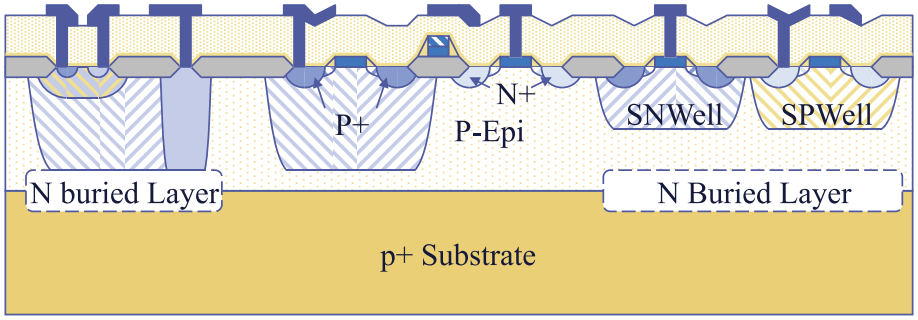


Figure 3

Figure 3 shows a cross-section of a typical BiCMOS process structure built using an epitaxial layer. Notice the n+ buried layer structures at the interface between the epi-layer and the substrate. The CMOS transistors are at the right, and the bipolar transistor is at the left.

Let's move on and discuss the epitaxial deposition process itself. First, one would normally perform a hydrogen prebake on the substrate. This helps remove any native oxide or other contaminants from the silicon so that we start with a defect-free surface. We accomplish the prebake by placing the wafers in ultrapure hydrogen for approximately 1 minute at a temperature between 1050 and 1150°C. In this process, the native silicon dioxide layer on the surface is converted to a volatile sub-oxide, which can be pumped away.

Next comes the deposition step. Silicon epitaxial growth occurs through pyrolysis of a gaseous silicon precursor. The choice of precursor gas is a function of the deposition temperature and other factors associated with the deposition. Some commonly used precursors include silane, dichlorosilane, trichlorosilane, and silicon tetrachloride. Process engineers use trichlorosilane most often for epitaxial processes. They will sometimes dilute the precursor gas in hydrogen to improve the process control. They also will add a dopant gas to provide a source of dopant atoms. We'll have more to say on that later on in this section. In addition to temperature and time, pressure and the mole fraction of the reactant gases are important variables in the reaction.

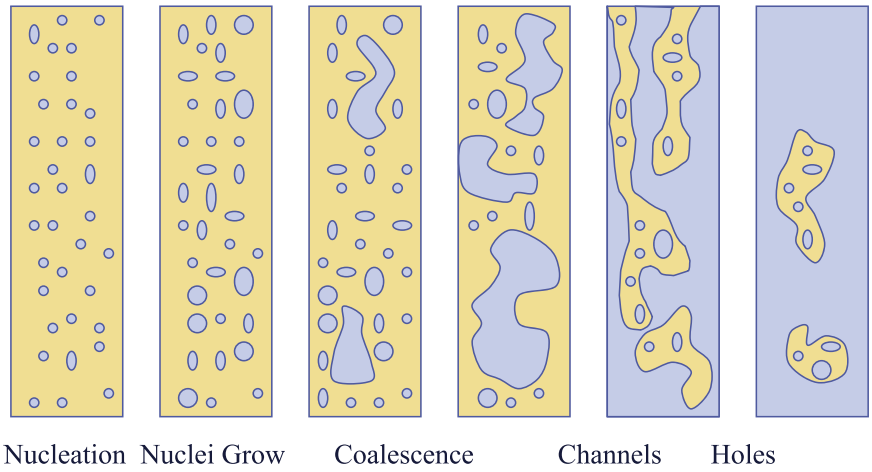


Figure 4. Stages of thin film growth

As precipitates or particulates grow, they follow the free energy principle discussed earlier. The free energy rule states that the total free energy of a system decreases with increasing size of particles. This leads to the growth pattern described in Figure 4. First, particles nucleate. Next, the individual nuclei grow. As they increase in size, the individual nuclei begin to impinge on each other. The overall system lowers the free energy through coalescence. As growth continues, the remaining area forms channels that slowly fill in, leaving holes that are the last to close up.

Let's now discuss epitaxial growth. Epitaxy is derived from the Greek words epi and taxis, which mean arranged upon. There are several reasons that epitaxial silicon wafers have become prevalent in the industry. First, the denuded zone does not result in a high purity surface layer. The process removes the oxygen precipitates, but it does not remove other impurities as well. Second, many applications require a heavily doped substrate for electrical connectivity, but a lightly doped region in which to fabricate devices. This cannot be readily accomplished with a standard silicon wafer. Finally, we would prefer uniform doping across the wafer. If you recall from earlier, the segregation coefficients of dopants cause the doping profile to be non-uniform across the wafer. Although Czochralski growers can grow silicon with dopants in them to help reduce the non-uniformity, it may not be sufficient for modern circuits. The solution is to take a wafer and grow additional crystal silicon on top of it. Epitaxial growth is normally accomplished using chemical vapor deposition. This results in uniform thickness layers with specified doping levels.

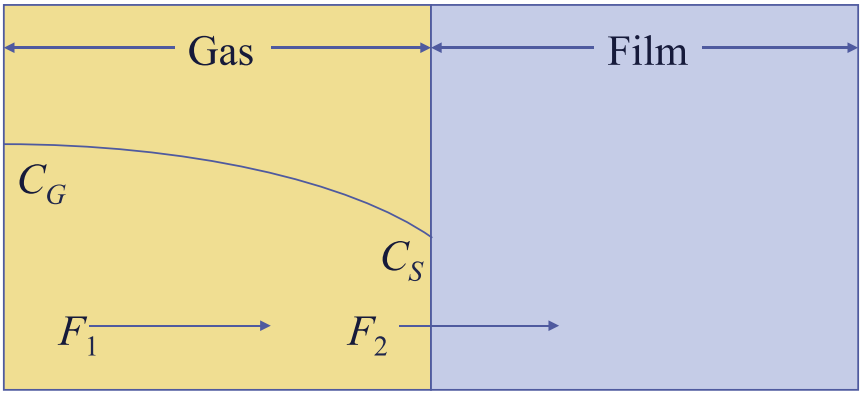


Figure 5. Grove epitaxial film growth model

Epitaxial growth has been studied for quite some time. In fact, Andy Grove—one of the industry's biggest names—developed a model for epitaxial film growth back in the 1960s. Chemical vapor deposition—the technique used for epitaxial film growth—has five main characteristics: a transport mechanism to bring the reactants to the surface, absorption of the reactants at the surface, a chemical reaction that forms the film, desorption of the products from the surface, and transport of the products away from the surface. The equation for this model is shown here: where the flux in the gas medium F1 is equal to the gas-phase mass-transfer coefficient times the difference between the concentration of the reactant in the gas and the concentration of reactant at the surface of the solid. The flux at the gas-film interface is the chemical surface reaction rate constant times the concentration at the surface of the solid.

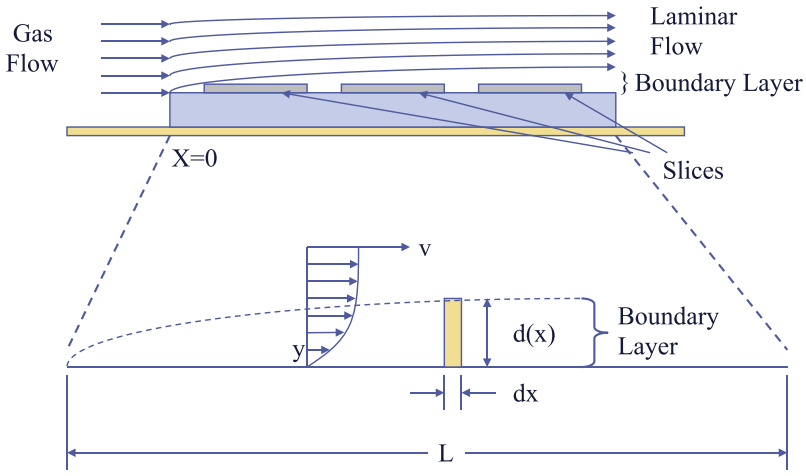


Figure 6. Boundary layer in a gas over a flat plate

One method for achieving higher reaction rates is to increase the gas phase mass transfer coefficient. This can be accomplished by inducing a laminar flow across the wafer. Figure 6 depicts the velocity of the gas across the wafer surface. A boundary layer exists near the surface of the wafer. This means that the velocity of the gas at the wafer surface will be zero. This effectively limits the film growth rate at higher gas flow rates.

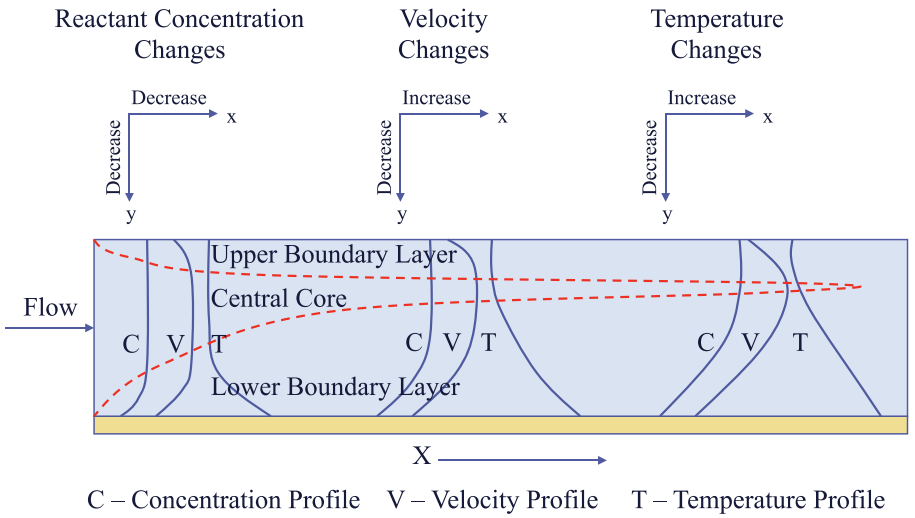


Figure 7. Boundary layer in a horizontal reactor

In a CVD reaction, the gas flow also affects the concentration, velocity and temperature of the airspace within the reaction chamber. Figure 7 illustrates these phenomena in a laminar flow regime. The dashed red line indicates the central core of the laminar flow regime. The boundary layers for the wafer above and the wafer level lie outside the central core of the laminar flow. The concentration begins to spread out from left to right. The velocity decreases near the wafer surface, and the temperature increases near the wafer surface.

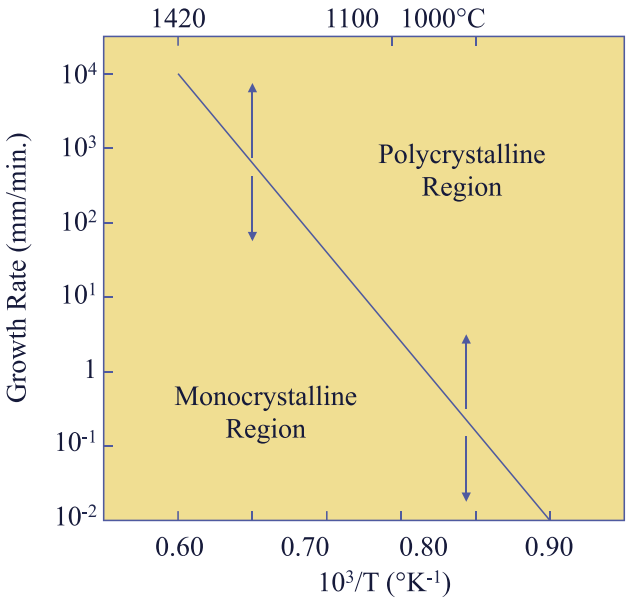


Figure 8. Maximum growth rate of single crystal Si

In a CVD reaction, the growth rate must be kept rather low. Most silicon epitaxial CVD reactions occur at temperatures between 1050 and 1200ºC. If the growth rate is too high, one will form polycrystalline silicon rather than single crystal silicon.

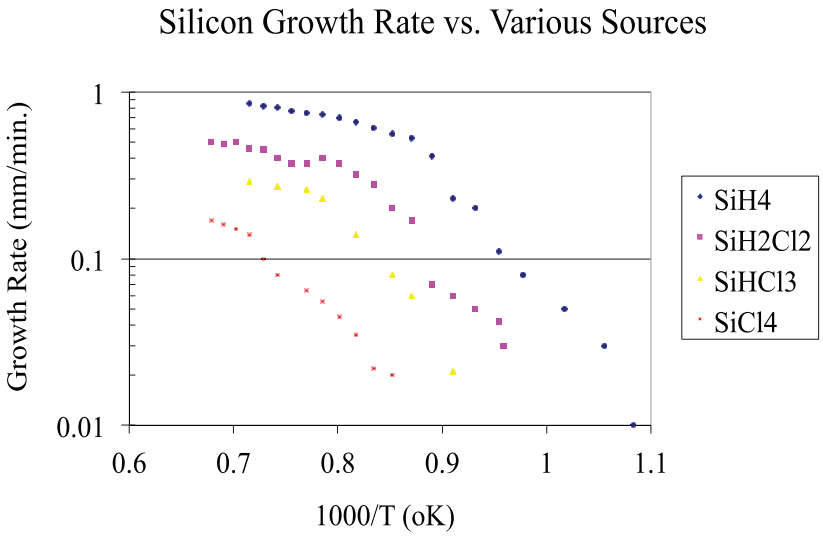


Figure 9. Growth rate of silicon vs. source

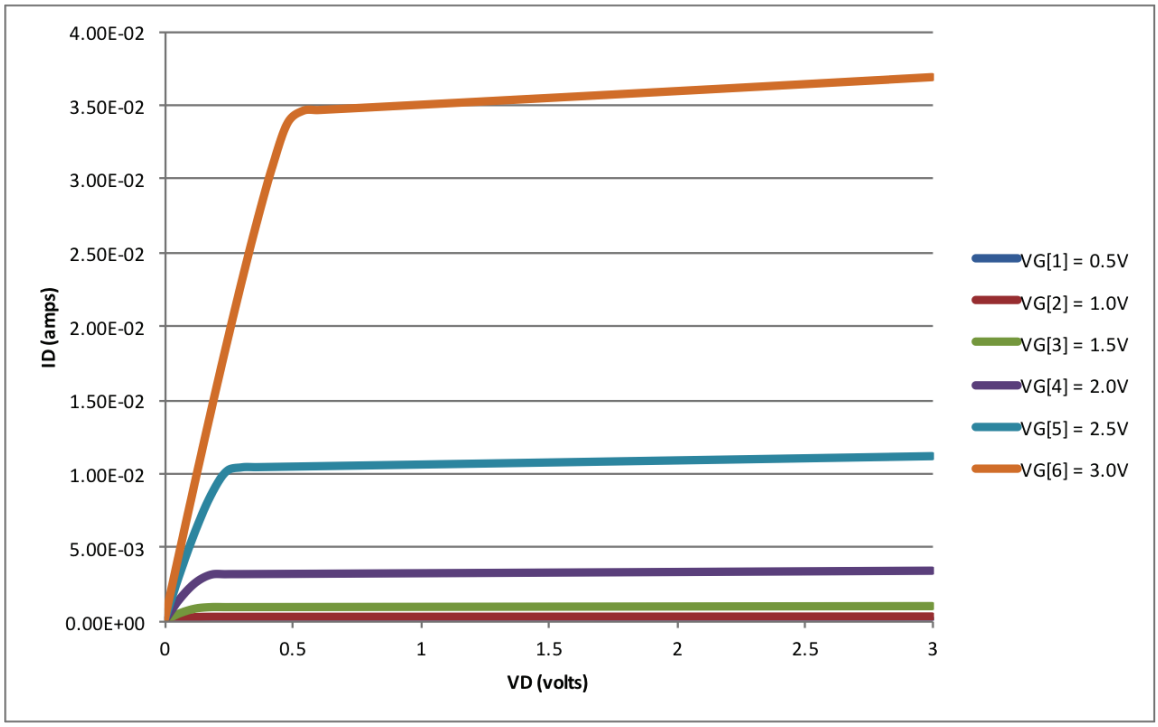
Figure 9 shows the growth rate of silicon versus temperature for several gases used in CVD epitaxy. The growth rate tends to increase as the temperature increases. Notice that one can achieve the highest growth rates with silane, followed by dichlorosilane, trichlorosilane, and silicon tetrachloride. So, at lower temperatures the growth rate is a strong function of temperature since the reaction is surface reaction-rate limited. At higher temperatures, the growth rate is a weak function of temperature since the reaction is gas phase mass transport limited.

[To be continued next issue]

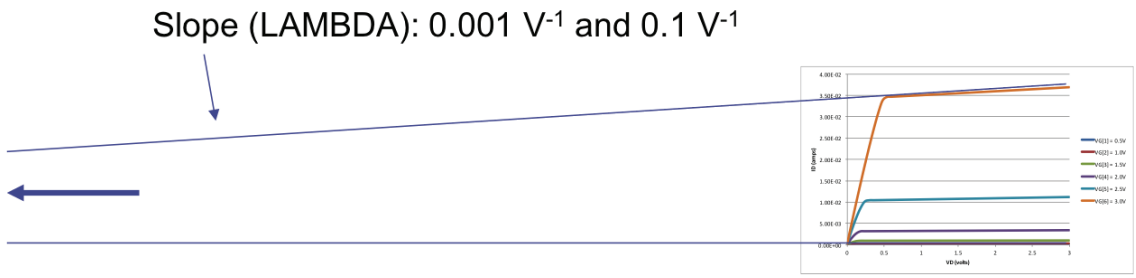
Technical Tidbit

Channel Length Modulation

Channel Length Modulation is an effect that has been known about for many years. Hofstein and Warfield published work describing the effect as early as 1965. This effect is more pronounced today in smaller feature-sized devices.



Basically, as the drain depletion region widens, it will intrude into the back-gate between the drain and the source. This effectively reduces the length of the channel. The voltage dropped laterally across the channel doesn't change (much), so the drain current will increase. This effect is called channel length modulation. It's the MOS equivalent of the Early effect in bipolar transistors. Mathematically, the channel length modulation introduces a Vds-dependent term in Ids, where Ids = 1/2 k (Vgs - Vt) (1 + LAMBDA * Vds), where LAMBDA is the channel length modulation parameter, a small number.



The typical values for LAMBDA are between 0.001 V^{-1} and 0.1 V^{-1}. While this effect is not usually a significant issue for digital circuits, it can be a large issue for analog circuits. In an analog circuit, one requires consistent and stable values, sometimes over a voltage range. Channel length modulation introduces an error that must be either accounted for, or removed using additional circuitry.

Ask the Experts

Q: What are some examples of circuits that use NPNs in the reverse active mode?

A: There aren't many, but a few analog switches have been designed to operate in this region. I also believe there are a few I2L (Integrated Injection Logic) chips that use reverse active mode.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques

7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

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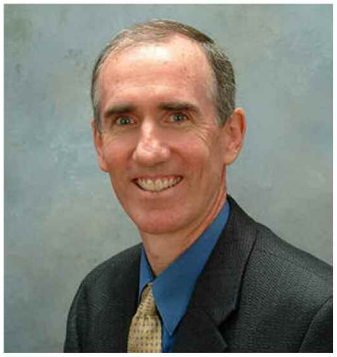
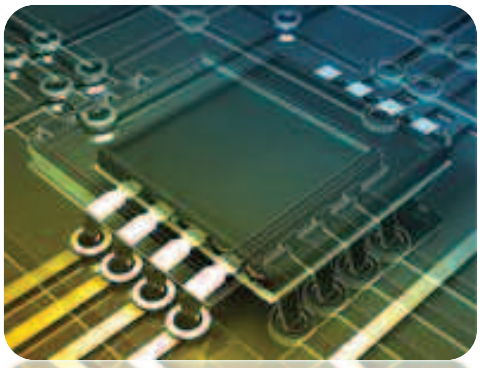


Chris Henderson

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the forum!



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Upcoming Courses

(Click on each item for details)

Defect Based Testing
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Munich, Germany

Failure and Yield Analysis
May 8 – 11, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Reliability and Qualification
May 15 – 18, 2017 (Mon – Thur)
Munich, Germany

Semiconductor Statistics
May 22 – 23, 2017 (Mon – Tue)
Munich, Germany

Wafer Fab Processing
June 5 – 8, 2017 (Mon – Thur)
Portland, Oregon, USA