Issue 56 February 2014

InfoTracks

Semitracks Monthly Newsletter

An Introduction to Quality

By Christopher Henderson

This article provides an introduction to quality for semiconductor components. Quality is an important aspect of semiconductor manufacturing. Customers expect high-quality components, and one must design quality processes, test for quality, and create procedures to handle issues of a quality nature that might arise.

Most companies define and implement quality at the highest levels within the organization, since customer perceptions are important. Anywhere the customer directly interacts with the company or indirectly feels the impact of the organization on quality, we define management practices to measure, control and improve the end experience for the customer. This diagram shows the impact of quality on the major organizations within the company. This diagram shows the roles of management, product engineering, other support functions, and manufacturing (see Figure 1, next page).

Most manufacturers will develop a set of documentation around quality. This is an example of some of the topics that one might address when developing quality documentation.

These are the important components of a quality system:

- Review of customer engineering specifications and requirements, including a process for defining the requirements, assessing the customer needs, our ability to meet those needs, pricing, modifications, and the need to protect confidential information.
- Personnel management, including roles and responsibilities,

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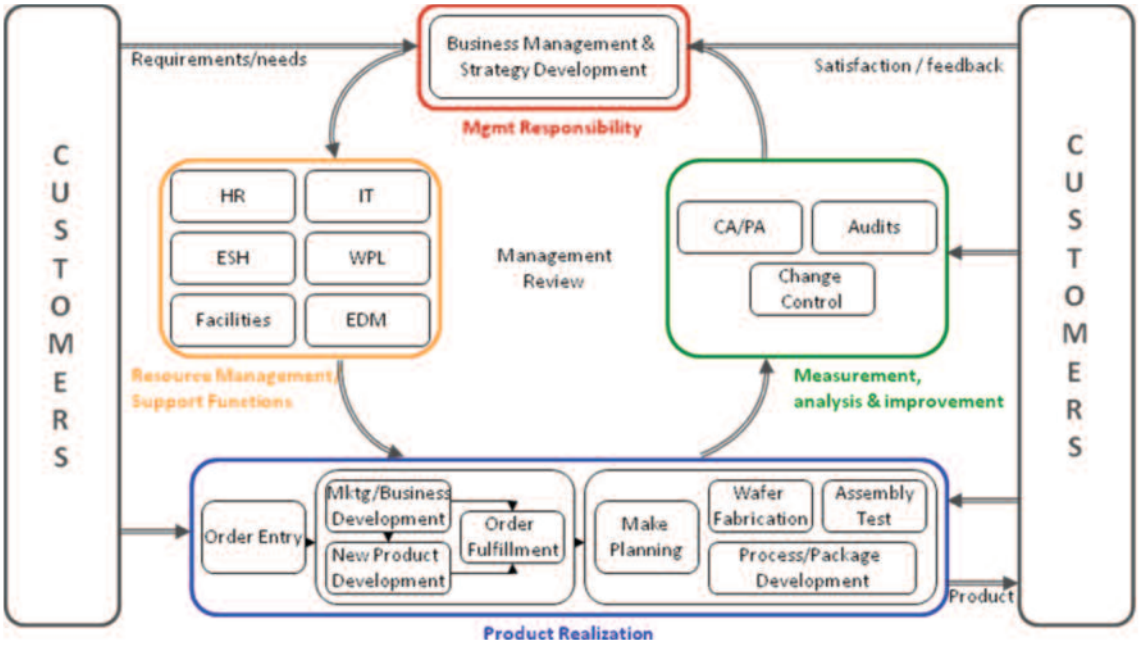


Figure 1. The impact and role of Quality on an organization (diagram courtesy Texas Instruments).

management oversight, training, and work procedures.

- Purchasing and supplier management to ensure we purchase quality materials and services that meet customer requirements and government regulations. This includes assessing our suppliers.
- Process management such as controlled specifications, work instructions, process flows, feasibility reviews, and risk analysis.
- Product assurance activities like product safety, inspections, tests, control of non-conforming material, handling requirements, protection from ESD, and inventory management controls.
- Control of all documents and specifications, including current revisions and a robust revision control policy.
- Product and inventory control, which would include unique identifiers, recording the appropriate inspections and steps, pass/fail data, parametric data, and traceability.
- Environmental control to ensure low defect levels and a safe environment.
- A formal change management process to inform customers of upgrades, changes, and end-of-life notifications.
- Continuity of supply in case of unexpected manufacturing shutdowns.
- A manufacturing process development plan.
- The appropriate inspection, measurement and test points and the associated corrective action plan when there are problems.
- A process for dealing with customer returns and timely failure analysis.
- The appropriate procedures to protect devices from electrostatic discharge damage.
- A process for continual quality improvement
- A system for quality records management for legal, statutory and customer requirements.
- Periodic internal audits.
- Management responsibilities, including communication the quality policy, ensuring it is appropriate, enforcing it, and monitoring it.

- A process for new product of technology sign-off.
- A process for dealing with sub-contractors.
- Review of the policy deployment and quality objectives.
- A system for documenting corrective action and preventing future failures or problems.
- Maintenance of the company's infrastructure.
- A structured product development process.
- And finally a software quality-assurance plan to ensure the integrity of software development, compliance to customer requirements, configuration management, and quality control.

An important aspect to quality is the time-zero quality. Many engineers also refer to this as initial quality. For a component, it should be free of defects, both visual and electrical. It should perform all of its functions correctly. A component that works partially would be low quality. For instance, if five percent of a shipped 12-bit analog-to-digital converter converted the six most significant bits correctly, but not the six least significant bits, we would think of this component as a low quality component. Not only should the component perform all of its functions, but it should be able to do it over its operating conditions. For instance, if a component is specified to work from 0 to 70°C, but only works correctly up to 65°C, then this would be a low-quality component. A good way to think about this is to think about your expectations with a new car. You expect not only the engine to start are run correctly, but also the brakes to work correctly, the power mirrors, heater, door locks and so on. You also expect it to start on cold mornings, as well as run properly on a hot day.

Figure 2. New car (left), used car in good condition (center), used car in poor condition (right).

The second aspect of quality is the time component. A high quality semiconductor component should work correctly for its intended lifetime, whether that be four months or four decades. It should pass its functional and parametric testing at the end of its life, just as it did at the beginning of its life. The failure rates should be at or lower than expected. For instance, we would consider a component to be low quality if the observed failure rate was 60 FIT (failures in time) when it should have been 50 FIT. There should also be no degradation or drift in parameters. This can lead to system failures. Again the automobile analogy can work well here. After five years and 75,000 miles, we would think about the automobile on the left as being a higher quality automobile, compared to the one on the right.

There are many steps to a qualified product. We can consider two areas that affect the qualified product: the product qualification process and the quality system. Under product qualification, we can define a technology reliability component, which tracks the goodness of the wafer fab process to create a working product, a product reliability component, which includes specific items related to the product design and its package, functionality, or the ability of the component to work over a specified operating range, and manufacturability, or the ability to create a high-yielding component that can be consistently produced.

Under the quality system, we have the process for creating a qualified product, monitoring of the line for potential problems, change management to control product revisions, and returns management, to correct problems that might occur. These systems should lead to a quality product, if implemented and monitored correctly.

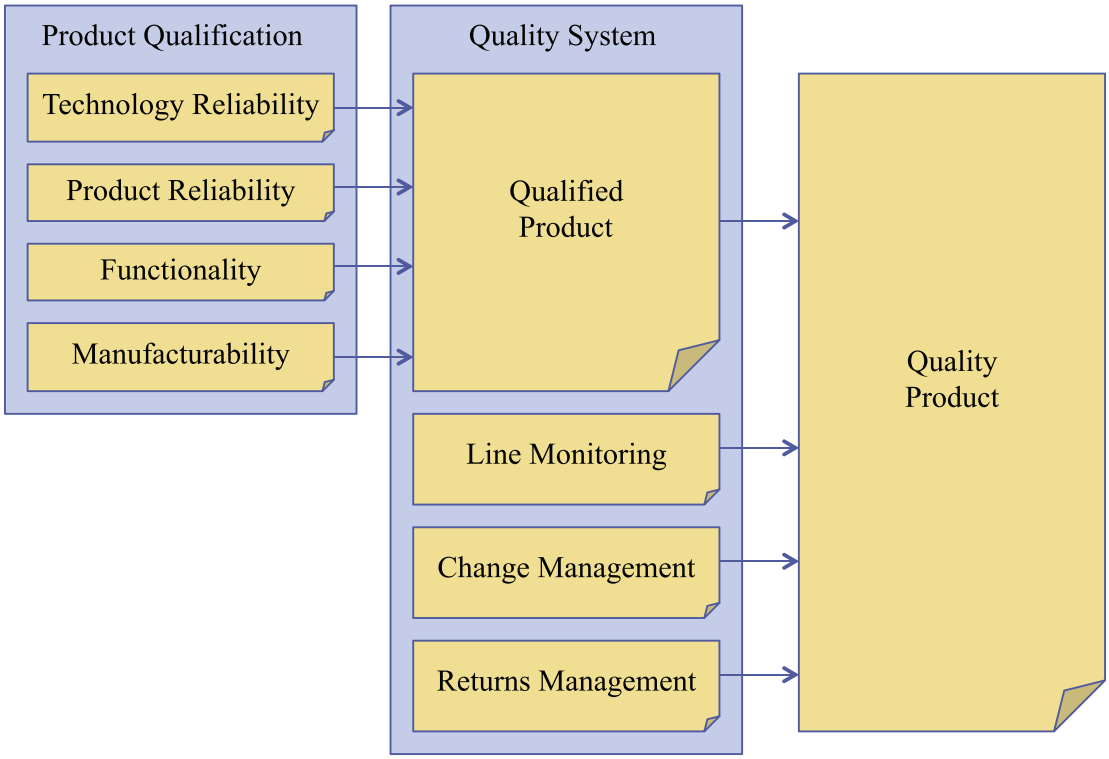


Figure 3. Diagram showing steps leading to a quality product.

Technology qualification is the qualification of the chip fabrication process, so this activity deals with the die. Engineers are primarily concerned with the failure mechanisms, so they research existing and potential new failure mechanisms, develop models for them, and then perform accelerated stress tests to understand the distribution of the failures due to those mechanisms. Then with the distribution data and the model, they can predict when a population of chips might fail due to this mechanism. They can then combine the various failure mechanisms and the information they have on the use profile for the end products, and generate an estimate of the reliability. This approach is sometimes referred to as knowledge-based qualification.

Let's briefly turn our attention back to standards based qualification. This is a common approach, and is still used widely in the industry. There are four major standards-based qualification processes used in the industry. The United States Military uses MIL-STD 883 for qualification. JEDEC, the Joint Electron Device Engineering Council, developed JESD47, a stress-based qualification standard. The Automotive Electronics Council has a standard for qualification, and Zentralverband Elektrotechnik- und Elektronikindustrie (ZVEI), or the Central Association of Electrical and Electronics Industry in Germany, also has a qualification standard that is used for some European electronics systems, including automotive systems. Several of these standards are discussed elsewhere in this workspace.

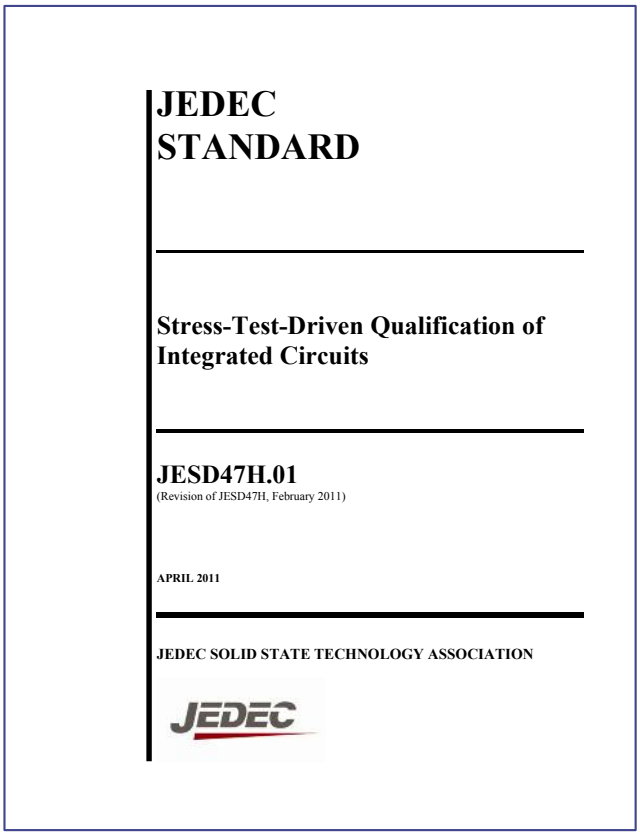


Figure 4. The JEDEC JESD 47 Qualification Standard.

Qualification provides upfront evidence that the product will work as intended in the application, but how do we ensure quality during production? Things can change, so we need a process to evaluate quality while the product is manufactured. We do this through testing. The more thorough the testing we do, the more evidence we can provide that we are shipping a quality product. Of course, the product has to pass the electrical testing.

There is a simple equation one can use to model the defect level, or quality as a function of yield and test coverage. Basically, the defect level will drop to zero if the yield can reach 100%, or if the test coverage can reach 100%. This model is known as the Williams and Brown model and is a simple way to make these estimations. One can do it for separate test sections like stuck-at-faults, transition faults, and IDDQ faults, or as an integrated fault coverage.

$$DL = 1 - Y^{(1-T)}$$

Williams & Brown model

DL = Defect level (escapes)
Y = Yield
T = Test (fault) coverage

For reliability prediction, engineers will use the results from the die-level accelerated testing and package modeling to develop an estimate of what the reliability should be at the outset. Once the manufacturer starts producing components, the reliability engineers can use the results from the standards-based testing to provide a more refined estimate of the reliability of the component. There are numerous

factors to consider when doing this. First would be the scale factors to map from the test die to the product die. Parameters such as chip area, gate area, transistor count, metal lengths, and package size and thickness all will play an important role. Also, power dissipation and heat dissipation play an important role. The customer use conditions and mission profile are critical as well. Parameters such as a thermal profile, the on-time of the component and system, the number of cycles, the mechanical stress, as well as the possibility for overstress like Electrical Overstress (EOS), Electrostatic Discharge (ESD) and latchup will all impact the reliability of the component.

This brings us to the qualification process itself. A part is considered qualified when all of the qualification objectives are met. These can be standards based, or knowledge-based objectives. If they're not met, then one needs to define a reliability and/or manufacturing screening strategy to remove potential failures from the population. Second, one might define a product guardband strategy to ensure that a mechanism does not proceed far enough to cause product failures. This strategy will need to be validated through testing to demonstrate that it is effective. If the strategy is deemed effective, and your customer agrees on the strategy, then one can qualify the product with these additional screens and guardbands.

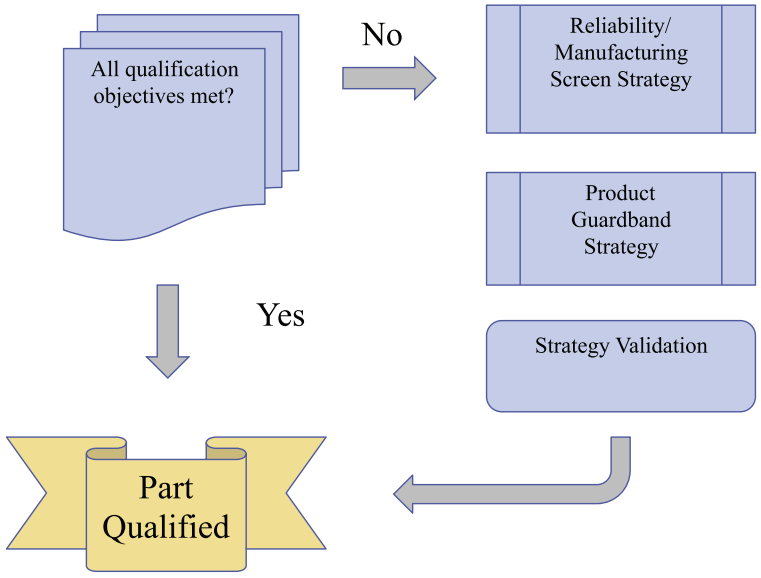


Figure 5. Steps to ensure one meets the qualification goal.

All customer returns should be treated seriously. Most companies have an established method for initiating and processing returns through a Return Material Approval or RMA process. Once the manufacturer receives the returned product, it undergoes appropriate testing and analysis to confirm the failure or problem. Those steps usually include:

- Problem notification & submission by the customer
- Receipt of samples by the manufacturer
- Initial problem verification
- Complete Failure or problem analysis
- Complete final corrective action plan
- Corrective and preventive actions implemented and verified
- And potentially a customer incident process flowchart

Many manufacturers use an information system to track customer returns. In a large company, one might compile and distribute monthly customer incident metrics. These can then drive continuous improvement. Some companies also use failure mechanism pareto's to drive continuous improvement in the various quality areas.

Failure Analysis is a critical step in the process where the analyst works to uncover physical evidence that clearly identifies the cause of failure. The analyst seeks this evidence through investigation on a case-by-case basis of failed integrated circuits. He or she uses electrical and physical analysis to perform an array of straightforward but sophisticated analytical measurements and techniques. Using the appropriate equipment and work processes, the analyst can isolate the location of the cause of failure on the die and physically characterize it. Failure analysts need to collaborate with other engineering disciplines; *e.g.,* product, test, design, assembly and process, in order to solve the analysis. The customer quality engineer and failure analysts communicate their progress, results and conclusions to both internal and external contacts so that the manufacturer can implement changes that will eliminate or at least mitigate the cause of failure.

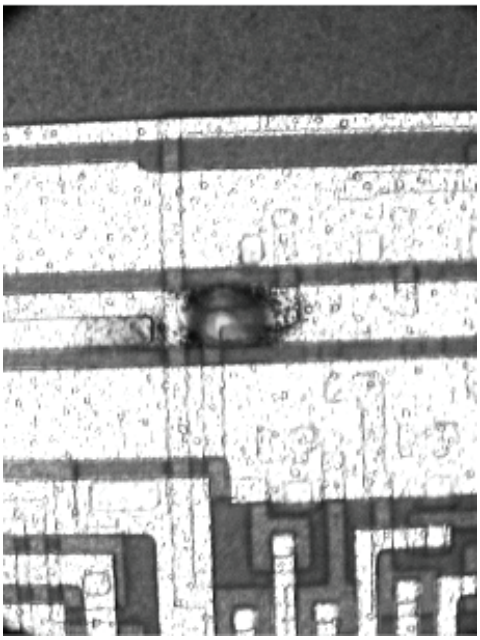


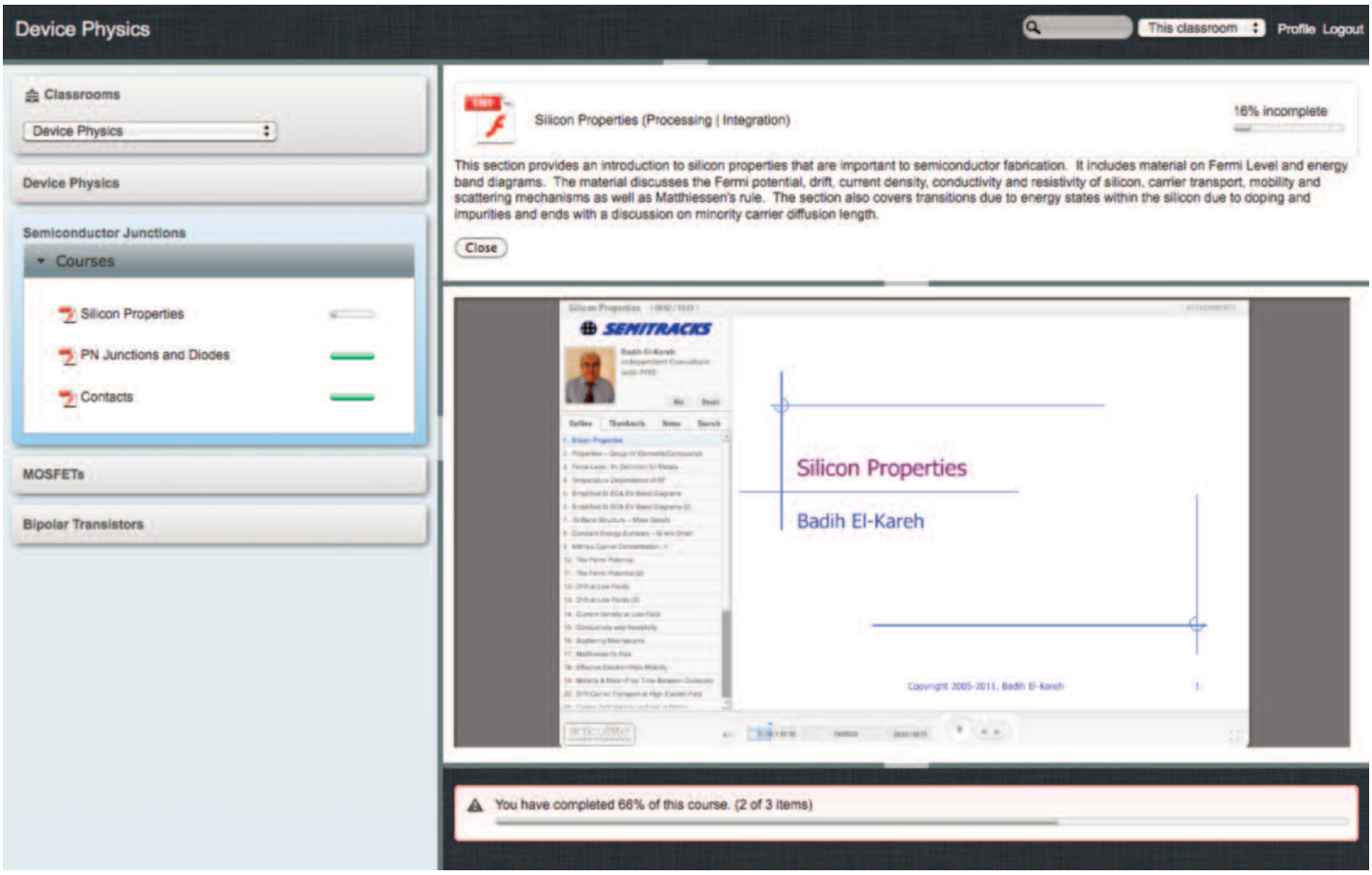
Figure 6. Example of a customer return failing from Electrical Overstress (EOS).

In conclusion, IC quality is part of a larger corporate strategy. From an engineering perspective, the activities that primarily fold into a quality process include the manufacturing process, reliability engineering, the qualification process, test engineering, a robust return material tracking system, and failure analysis. Ultimately though, what the customer perceives as a whole from the manufacturer impacts their view of quality, so there are many intangible aspects to it. This includes support, service, and other functions beyond the engineering aspects we discussed in this section.

Online Training System Update

We wanted to make you aware of some developments with our Online Training System. We recently completed an upgrade of our system. We are also in the process of adding additional content into the system. In the new system you can log in more easily, access a wider range of videos, and easily run the presentations in an inline mode (which avoids the need for configuring a pop-up blocker), or run the presentations in full-screen mode (for easier viewing on small screens). The new system is also compatible with the iPad tablet, so look for content that can run on your iPad in the near future. The New Year is underway. Why not invest in yourself and purchase one-year access to the system? You can find out more information about our system and register at

http://www.semitracks.com/index.php/online-training



Ask the Experts

Q: We are looking to develop the EBIC technique on our FA lab (we have a Kleindiek system) mainly on Silicon power device; any help or comments on our activities would be greatly appreciated (defect detected, technical details, limits, advantages over other methods…)

A: This is an overlooked technique that is great for isolating failures. It can be especially useful in conjunction with a nanoprobing solution in the SEM, like you mention. Another approach is to use an AFM Probing System (Multiprobe is a manufacturer of this type of system). If you do a lot of fault localization, then this can be a great way to isolate things further. We discuss this technique in our Online Training System, and can do a one-day course on this topic as well.

Spotlight: Product Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can also involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types can create difficulties. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. Customers expect fast, smooth qualification, but incorrect assumptions, use conditions, testing, calculations, and qualification procedures can severely impact this process. Your company needs competent engineers and scientists to help solve these problems. ***Product Qualification*** is a two-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor technology and product qualification. This course is designed for every manager, engineer, and technician concerned with qualification in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues and how to resolve them.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and relationship to qualification.
2. **Failure Mechanisms.** Participants learn how product qualification and failure mechanisms relate to one another. We provide an overview of these mechanisms. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, EOS, ESD, latchup, drop tests, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to qualify today's components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled in qualification.
4. The seminar will discuss the major qualification processes, including JEDEC JESD47, AEC Q-100, MIL-STD, and other related documents.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement additional tests that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

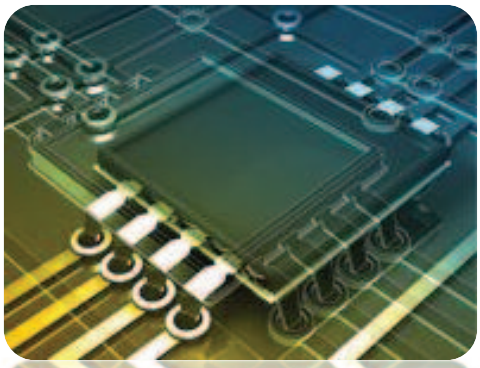
COURSE OUTLINE

1. Introduction to Reliability
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Statistics and Distributions
   a. Basic Statistics
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Which Distribution Should I Use?
   d. Acceleration
   e. Number of Failures
3. Overview of Die-Level Failure Mechanisms
   a. Time Dependent Dielectric Breakdown
   b. Hot Carrier Damage
   c. Negative Bias Temperature Instability
   d. Electromigration
   e. Stress Induced Voiding
4. Overview of Package Level Mechanisms
   a. Ionic Contamination
   b. Moisture/Corrosion
   c. Thermo-Mechanical Stress
   d. Interfacial Fatigue
   e. Thermal Degradation/Oxidation
   f. Solder Joint Reliability

5. Overview of Board Level Reliability
   a. Solder Joint Reliability
   b. EOS/ESD/LatchUp
   c. Single Event Effects

Day Two (Lecture Time 8 Hours)

6. Test Structures and Test Equipment
7. Developing Screens, Stress Tests, and Life Tests
   a. Burn-In
   b. Life Testing
   c. HAST
   d. JEDEC-based Tests
   e. Exercises
8. Developing a Qualification Program
   a. Process
   b. Standards-Based Qualification
   c. Knowledge-Based Qualification
   d. MIL-STD Qualification
   e. JEDEC Documents (JESD47H, JESD94, JEP148)
   f. AEC-Q100 Qualification
   g. When do I deviate? How do I handle additional requirements?
   h. Exercises



Upcoming Courses

(Click on each item for details)

Fault Isolation
March 19-21, 2014 (Wed – Fri)
Singapore

Fault Isolation
March 24 –26, 2014 (Mon – Wed)
Penang, Malaysia

CMOS, BICMOS and Bipolar Process Integraion
March 25 – 26, 2014 (Tue – Wed)
Austin, Texas, USA

Semiconductor Package Design, Simulation, and Technology
April 7 – 9, 2014 (Mon – Wed)
San Jose, California

Product Qualification
April 15 – 16, 2014 (Tue – Wed)
San Jose, California

Failure and Yield Analysis
May 5 – 8, 2014 (Mon – Thur)
Munich, Germany

MEMS Technology
May 12 – 13, 2014 (Mon – Tues)
Munich, Germany

Semiconductor Reliability
May 12 – 14, 2014 (Mon – Wed)
Munich, Germany

Product Qualification
May 15 – 16, 2014 (Thur – Fri)
Munich, Germany

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!
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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!