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# InfoTracks

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## Failure Analysis Procedures – Part IV

By Christopher Henderson

This article is the conclusion of our series on failure analysis procedures. As we have been discussing over the past several months, sometimes failure analyst's can best understand the FA procedure for a component by thinking about the process in terms of the type of failure. This is a flowchart that describes how to analyze a short or a leakage failure at either the wafer or package level. Both flows are very similar, so we will discuss them together.

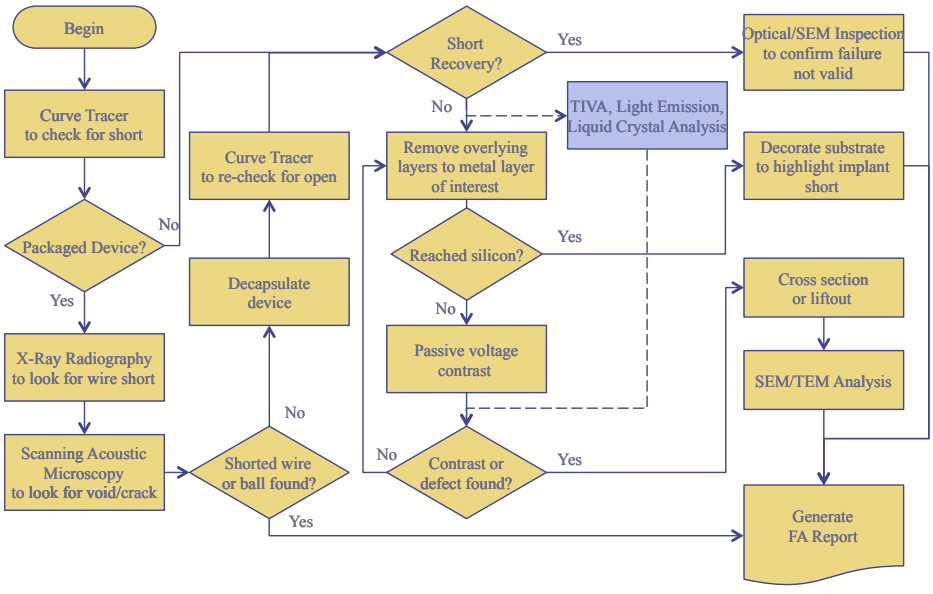


Figure 1. Flowchart for a short circuit failure

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Figure 1 shows a flowchart that describes how to analyze a short circuit. We begin by examining the device with a curve tracer to check for the short. The pin or bump exhibiting the short should be identifiable from the automatic test equipment (ATE) datalog for the device. If the device has not been tested it should be tested using ATE to confirm the failure. We can also do this directly with the curve tracer, but it can be very time-consuming for a device with many pins, bumps, or bond pads if we're doing this at the wafer level. The flow now branches if we have a packaged device. If we have a packaged device, we can perform x-ray radiography and scanning acoustic microscopy to look for a wire or bump short, void, crack or some other anomaly. There are other advanced techniques one can try like time domain reflectometry or Superconducting Quantum Interference Device (SQUID) microscopy as well to help localize this type of problem. If we are able to locate a shorted wire, shorted ball, or other obvious anomaly, we can document it and proceed to the report generation. If there is no obvious defect or problem, then the problem most likely lies on the die itself. It makes sense to decapsulate the device to expose the die surface. After decapsulation, one should re-check the pin in question to make sure the short is still present. If the failure is no longer present, then an optical or SEM inspection might be in order at this point to look for anything that might have been missed. If the failure is still present, then we can begin to isolate it on the die. If the package structure is still present, we can use a technique like Liquid Crystal Thermography for a front-side analysis approach, Light Emission, or laser-based techniques like TIVA (Thermally-Induced Voltage Alteration) or OBIRCH (Optical Beam-Induced Resistance Change) to localize the short from both the front or the backside. However, if the package structure is no longer present, then we will need to use a more traditional technique like passive voltage contrast. We then enter a loop where we remove overlying layers to expose the layer of interest, and perform voltage contrast. We can continue in the loop until we identify the failure site or reach the silicon substrate. If we don't see incorrect contrast, then we can remove the chip layers down to the next metal layer in the node, or down to the upper-most metal layer in the next candidate. We would continue this process down through the backend of the process, or through the interconnect and dielectric layers. Once we see incorrect contrast or the defect itself, we can determine if we need further analysis. This might involve a cross-section or liftout of material. We can then examine the defect with the SEM or TEM as appropriate. If we do not see the defect after removing all of the interconnect and dielectric layers, we can decorate the substrate to highlight potential defects in the silicon. At this point, we can write up our findings in a failure analysis report.

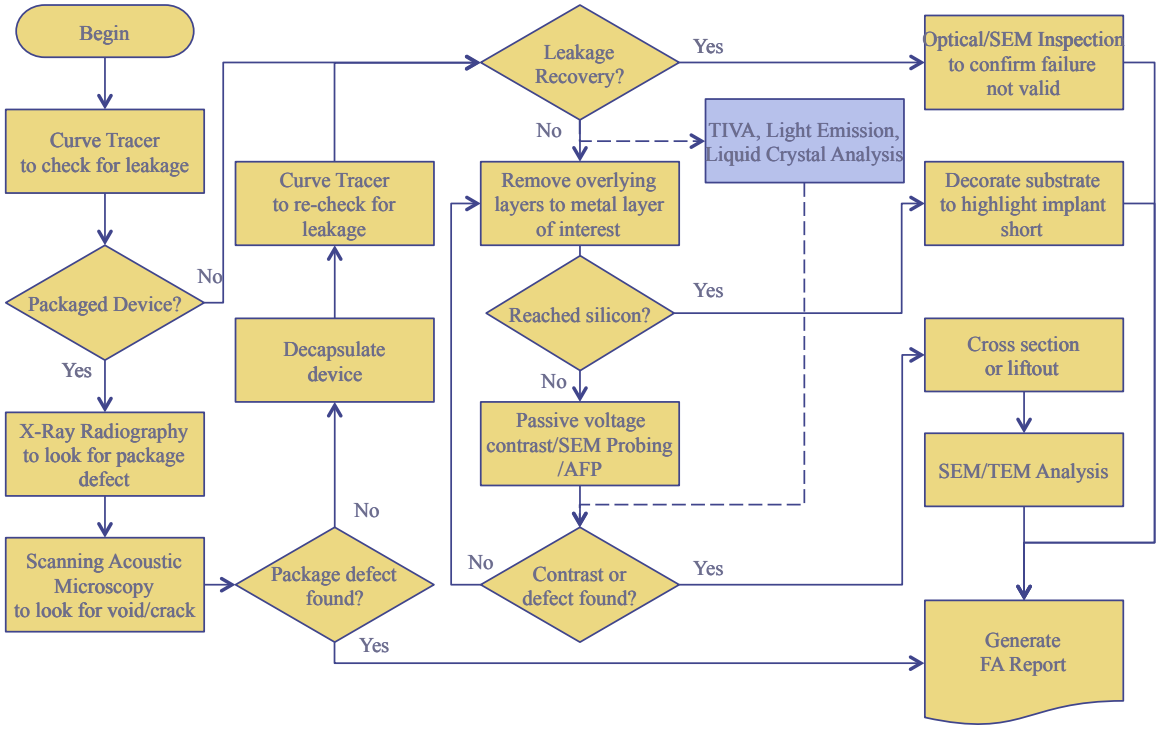



Figure 2. Flowchart for a leakage failure

Figure 2 shows a flowchart that describes how to analyze a leakage failure. This flowchart is quite similar to the flowchart we showed in Fig. 1 to describe how to analyze a short circuit failure. Therefore, we will just point out the differences. The main difference in looking for a leakage path as opposed to a short is the magnitude of current involved. A leakage path is likely to have a much lower current than a short. Furthermore, a leakage path may still allow the device to function properly. Therefore, electrical test techniques like IDDQ (Quiescent Power Supply Currrent) testing become more important. Furthermore, the curve tracer also becomes more important as characterization tool. A leakage path in the package can be quite difficult to detect. Superconducting Quantum Interference Device (SQUID) microscopy is an important technique to help localize this type of problem. Leakage isolation at the die level can also be challenging. Maintaining the package structure becomes more important, since techniques like Passive Voltage Contrast are less effective. If the package structure is still present, we can use techniques like Liquid Crystal Thermography for a front-side analysis approach, Light Emission, or laser-based techniques like TIVA (Thermally-Induced Voltage Alteration) or OBIRCH (Optical Beam-Induced Resistance Change) to localize the leakage path from both the front or the backside. Analysts use passive voltage contrast to identify opens and shorts. If we don't see incorrect contrast, then we can remove the chip layers down to the next metal layer in the node, or down to the upper-most metal layer in the next candidate. This may require some manual probing with probes in the SEM or an Atomic Force Probe system. We would continue this process down through the backend of the process, or through the interconnect and dielectric layers. Once we see incorrect contrast, identify the defective transistor, or interconnect segment, or the defect itself, we can determine if we need further analysis. This might involve a cross-section or liftout of material. We can then examine the defect with the SEM or TEM as appropriate. If we do not see the defect after removing all of the interconnect and dielectric layers, we can decorate the substrate to highlight potential de-

fects in the silicon. At this point, we can write up our findings in a failure analysis report.

While FA becomes more challenging as we go to smaller and smaller feature sizes, there are some standard flows that work well. These five FA flows we have discussed in this and previous articles can help the analyst structure their work in a logic manner to increase the chances for success. If you would like to learn more about FA processes, we would encourage you to sign up for access to our Online Training System. The system contains a number of presentations that talk not only about this topic, but also other procedures used in failure analysis. The link to learn more is shown here:

http://www.semitracks.com/index.php/online-training

## Technical Tidbit

### Analyzing Basic Circuit Behavior with Matlab

This Tidbit will focus on demonstrating a method to solve for an unknown voltage in a simple circuit like this one (see Figure 1 below) using Matlab. It might be useful to know what the voltage is between the two, four and eight ohm resistors. This is not very difficult to find by hand, but it is even easier with Matlab, and you can set it up so that you can test various voltages quickly.

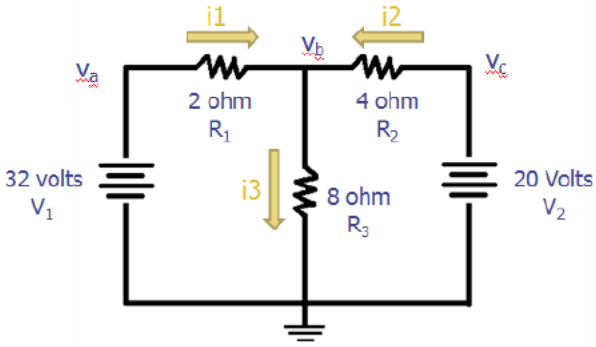



Figure 1.

Decide on a reference node, which is usually the ground. Label all remaining nodes. You will need to apply Kirchhoff's current law to each node not connected to the voltage sources. Kirchhoff's Current Law states that the sum of the input currents into a certain point must equal the sum of the output current. In our example, both current 1 and current 2 feed into current 3, so the sum of current 1 and current 2 must be equal to current 3. Take each current 'I' and split it up according to Ohm's law. Because V1 feeds directly into v sub a, V1 is equal in voltage to v sub a. The same is true of V2 and v sub b. Because of this, we can replace v sub a and v sub b in our equations with V1 and V2. Now that we've minimized the amount of unknowns in the equations, we can solve with Matlab. This equation will be easy to set up, due to the fact there will only be one unknown, V sub b.

Here's an example of a way this might be coded in Matlab (see Figure 2 below). We'll provide a few notes on the coding for people who might be a little rusty with Matlab. 'syms vb' on line three defines v sub b as a symbolic variable with no set value. Line four sets the equation you entered equal to the variable 'equation'. The 'sym()' command takes the string inside of it and recognizes it as a symbolic equation instead of the string of numbers it usually expects. Failure to use 'syms' or 'sym()' will cause errors, because it usually needs variables like vb to be defined in a solid, numerical way. You could solve the equation for any defined variable by changing the text that is currently 'vb' in line eight to the variable you want to solve for. Line nine solves the equation in terms of vb. The solve(x,y) function takes the equation x and solves in terms of y. Line ten displays the newly arranged equation when you run the

program. It is understood that the equation is equal to 'vb', so when it displays the equation, instead of being in the format 'y = mx –b', it'll be in the format 'mx-b' . Lines twelve through sixteen set each variable in the equation equal to a numerical value. These values are from the initial circuit. Line seventeen takes the rearranged equation and evaluates it using the numerical values. Line 18 displays the value of the equation. Since the equation is equal to 'vb', this is the unknown voltage 'vb' that we were trying to solve for.

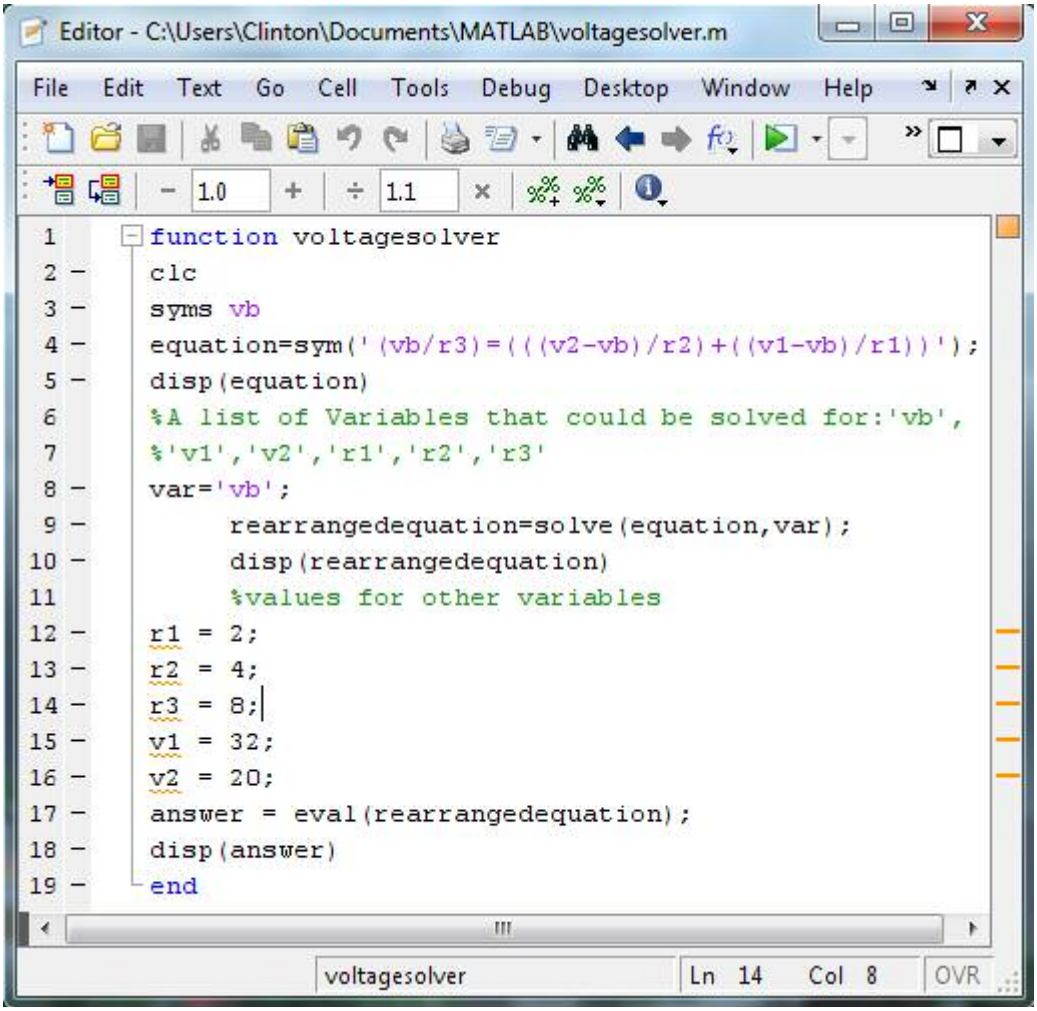



Figure 2: Matlab code as seen in a MATLAB window.

This completes the generation of the function. If you run it exactly like this, the output will show you the initial equation, the rearranged equation, and the answer. You can hide the first two by adding semicolons to the ends of lines five and ten.

Here's the code, if you'd like to copy and paste it into Matlab.

```
function voltagesolver
clc
syms vb
equation=sym('(vb/r3)=(((v2-vb)/r2)+((v1-vb)/r1))');
disp(equation)
%A list of Variables that could be solved for:'vb',
%'v1','v2','r1','r2','r3'
var='vb';
rearrangedequation=solve(equation,var);
disp(rearrangedequation)
%values for other variables
r1 = 2;
r2 = 4;
r3 = 8;
v1 = 32;
v2 = 20;
answer = eval(rearrangedequation);
disp(answer)
end
```

## Ask the Experts

**Q: Today, you see a lot more equipment using Dry Pumps. Why is this?**

**A:** This is primarily due to the fact that oil-based pumps suffer from a phenomenon known as backstreaming. Oil vapor can be sucked back into the system chamber. In a wafer fabrication tool, this can lead to contamination on the wafer surface, which can interfere with processing and limit the yield. In an analytical tool like a scanning electron microscope, the oil vapor on the surface can be carbonized or polymerized by the electron beam, creating a thin layer that interferes with imaging. Furthermore, this material is difficult to completely remove. The best way to avoid these problems is to use a dry pump instead.

## Spotlight on our Courses: Thin Film Photovoltaics Reliability

Thin-film photovoltaics are a cost-effective alternative to crystalline silicon photovoltaics. Although thin-film efficiency is not as high as crystalline silicon, researchers have made significant progress improving the efficiency. As a result, the cost-per-watt is favorable to crystalline silicon. Reliability is a significant issue though. These systems must survive in a harsh environment for many years, so engineers continue to study this problem. This is a great opportunity to hear from an expert in the field about the current testing approaches, failure mechanisms, and approaches to mitigate the failure rates. If you are interested in attending this course, or if you are interested in having this done as an in-house course for your staff, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

### COURSE OVERVIEW

***Thin Film Photovoltaics Reliability*** is a one-day course that goes in depth to describe thin-film photovoltaic reliability. This course is designed for every manager, engineer, and technician entering the photovoltaic field, whether it be working directly for a photovoltaic manufacturer, system integrator, or selling to the PV manufacturers.

Participants learn to the basics of thin film photovoltaics: the technology, the fabrication processes, and reliability. The course covers seven major topic areas.

1. **Introduction and History of Solar Cells.** Participants learn about the history and development path behind thin-film photovoltaics.
2. **Thin-film Device and Module Manufacturing.** Participants will learn how thin-film solar cells are manufactured. They discuss the fabrication, packaging and module assembly steps.
3. **Thin-film Device Physics.** Participants learn how the solar cell operates. They learn about the properties that make a cell efficient and low loss.
4. **Thin-film Reliability Testing.** Participants learn about the tests currently performed on solar cells and modules to ascertain their reliability. They learn how the industry makes measurements and analyzes the results.
5. **Design of Experiments.** Participants learn how to design experiments to help optimize cell durability.
6. **Data Management Systems.** Participants investigate the data management systems for correlating cell fabrication and reliability, and how to trace data from the manufacturer to the module assembler and into field use.
7. **Case Studies.** Participants cover several case studies involving CdTe and CIGS thin-film cell reliability issues.

### DESCRIPTION

Thin-film photovoltaic CdTe and Cu(In,Ga)$Se_2$ (CIGS) modules consist of a large-number of series-connected, individual cells that are packaged to withstand 10 – 20 years of outdoor exposure. Thin-films represent a technology departure from conventional, single-crystal approaches for converting sunlight to electricity. High manufacturing throughput—with production costs less than $1/watt—result in polycrystalline microstructures with thickness and grain sizes on the order of a micron. These structures are inherently more sensitive than their single-crystal counterparts to ambient conditions both external and internal to the package.

Direct correlations between accelerated lifetime testing (ALT) of cells and outdoor field testing of

modules is difficult due to the many, complex ways modules fail. However, cell-level ALT is useful for understanding degradation at the cell component level.

This short course will discuss how thin film solar cell modules are constructed, the primary ways such products fail in the field, and how packaging effects and intrinsic cell durability are separate, but equally important in determining the total module reliability. Focus will be placed on the experimental methodology by which the intrinsic durability of thin-film solar cells have been measured, studied, and improved through cell modifications

Thin film solar cells consist of numerous layered components, each with varying degrees of susceptibility to external stressors. For example, polycrystalline CIGS solar cells show considerably better performance during low-humidity ALT but with increasing humidity degrade faster due to the moisture sensitivity of the transparent conducting oxide (TCO) layer used in these cells. The type of TCO used in CdTe devices is also shown to significantly affect CdTe cell durability. In CdTe-based solar cells, the intrinsic durability of the CdTe semiconductor is also shown to be dependent on how the CdTe layer is deposited. The ability to control the Cd/Te stoichiometry by varying growth temperature has a pronounced effect on the voltage stability of these devices. Lower growth temperatures are shown to favor a Cd-rich stoichiometry and with a resulting defect chemistry that reduces diffusion processes in CdTe. Recent comparisons of degradation in CdTe devices with models based upon reaction-diffusion models used in the CMOS semiconductor industry (*e.g.,* NBTI) suggest that diffusion control may be one path towards making thin film solar cells more robust.

Finally, the historical development (and underlying physics) of using cell hysteresis for predicting future cell durability will be discussed. Thin film cells and modules can exhibit performance characteristics which are dependent upon prior electrical and optical history. For example, the magnitude and direction (*i.e.,* sign) of electrical bias can result in two different values for the same cell performance measurement as well as other dependent parameters like open-circuit voltage, $V_{oc}$, short-circuit current, $I_{sc}$, depletion width, carrier density, etc. Recent data shows a good correlation between future $V_{oc}$ degradation and the magnitude of hysteresis observed in cells immediately after fabrication thus providing an important discussion point: Is it possible to predict the future stability of modules?

## COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the photovoltaic technologies and manufacturing methods.
2. The participant will be able to understand the properties of a variety of photovoltaic cells.
3. The seminar will identify the major issues associated with cell efficiencies.
4. The seminar will also identify the major tradeoffs associated with each technology and reliability.
5. The participant will be able to understand how to ascertain the reliability of PV modules from reliability test methods.
6. The participant will be able to make informed decisions regarding manufacturing processes for various silicon solar cell technologies.
7. The participant will be able to understand his/her role regarding reliability/durability of PV modules.

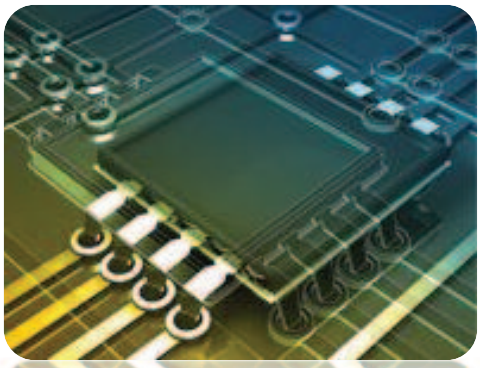
## INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, problem solving and question/answer sessions, and participants will learn practical information about the solar photovoltaic industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

## COURSE OUTLINE

1. Introduction and history of polycrystalline thin-film solar cells.
2. Thin-film module manufacturing
    a. Introduction
    b. Thin-film manufacturing
    c. Module assembly
    d. Testing
3. Thin-film device physics
    a. Solar Cell Operation
        i. Ideal Solar Cells
        ii. Solar Cell Structure
        iii. Light Generated Current
        iv. Collection Probability
        v. Quantum Efficiency
        vi. Spectral Response
        vii. Photovoltaic Effect
    b. Solar Cell Parameters
        i. IV Curve
        ii. Short-Circuit Current
        iii. Open-Circuit Voltage
        iv. Fill Factor
        v. Efficiency
    c. Resistive Effects
        i. Characteristic Resistance
        ii. Effect of Parasitic Resistances
        iii. Series Resistances
        iv. Shunt Resistances
        v. Impact of Both Resistances
4. Thin-film device fabrication
    a. Substrate Material
    b. Thin-film Growth/Deposition
    c. Texturing
    d. Diffusion
    e. Isolation
    f. Anti-Reflection Coating

5. Thin-film device durability procedures, measurements and analysis
   a. Similarities/differences with modules
6. Design-of-Experiment (DOE) techniques for optimizing cell durability
7. Data management systems for correlating cell fabrication and cell durability
8. Thin-film cell hysteresis – observations and correlations
9. Case studies involving CdTe and CIGS thin film cellsSolar Cell Properties



# Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

*To post, read, or answer a question, visit our forums.*
*We look forward to hearing from you!*

# Upcoming Courses

(Click on each item for details)

**Wafer Level Chip Scale Packaging**
February 25 – 26, 2013 (Mon – Tue)
Penang, Malaysia

**Copper Pillar Bumping**
February 28 – March 1, 2013 (Thur – Fri)
Penang, Malaysia

**Failure and Yield Analysis**
March 18 – 21, 2013 (Mon – Thurs)
San Jose, California

**Wafer Fab Processing**
March 26, 2013 (Tues)
San Jose, California

**Fundamentals of Yield (co-sponsored by SEMI)**
March 27, 2013 (Wed)
San Jose, California

**Semiconductor Reliability**
April 3 – 5, 2013 (Wed – Fri)
San Jose, California

**Failure and Yield Analysis**
April 8 – 11, 2013 (Mon – Thurs)
Penang, Malaysia

**Photovoltaics Reliability (co-sponsored by SEMI)**
April 18, 2013 (Thurs)
San Jose, California

**Advanced Thermal Management and Packaging Materials**
April 22 – 23, 2013 (Mon – Tues)
Philadelphia, Pennsylvania