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## Silver Loaded Leaded Glass Die Attach

Developed by American scientists in the mid-1980s, silver-glass adhesives are a potential substitute for gold-silicon eutectic, as they have high thermal conductivity and a coefficient of thermal expansion (TCE) close to that of silicon. Silver-glass has been evaluated for the manufacture of power hybrids and for attaching active devices with gold or silver back metallization to substrates plated with nickel or silver-plated copper. A number of military and space customers now use silver-loaded glasses for die attach since the TCE reduces the stress in the package.

A typical silver-glass paste contains 80–85% by weight of silver flake and lead borate glass dispersed in an epoxy-resin-based system. The paste is dispensed into the package cavity, the die placed on the paste, and the package inserted in a furnace. The heat removes the organic vehicle and then centers the residual solder and glass to bond the die strongly to the ceramic.

The material should form a smooth fillet free of voids and cracks. To achieve this, the conventional process includes a pre-drying step of 2–10 hours at 60–80°C, depending on die size. Sufficient solvent needs to be eliminated to avoid the formation of voids, and the void density depends on the drying temperature. However, too high a drying temperature can reduce shear strength because there is no intimate contact between die and glass. Optimized conditions should yield voids less than 1%. Several researchers have determined this level of voiding experimentally using radiographic techniques.

The figure below illustrates the sequence of events which happen to silver glass paste during firing. Solvent evaporation (50–200°C) is followed by polymer resin burn-out (300°C).

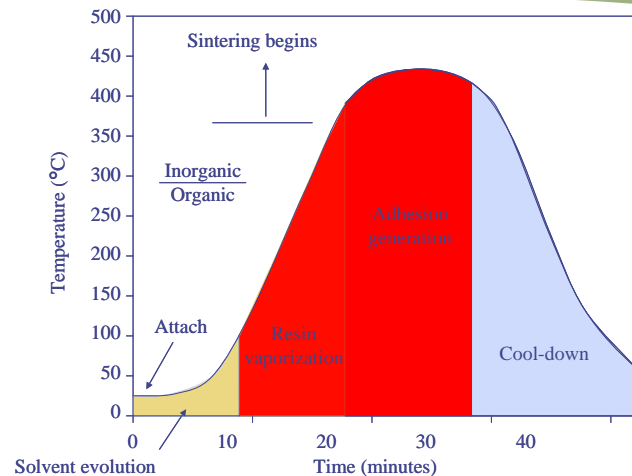


Figure 1. Firing profile for silver glass.

The glass starts to soften at 340°C, which causes silver-glass sintering to accelerate and further wet the surfaces of die and substrate. Reaction bonding of silver-glass with silicon and alumina also starts at about 340°C, and the reaction is completed when the temperature has been maintained at 410–430°C for approximately 10 minutes.

The shear strength of the material increases with sintering temperature towards an asymptotic value, probably due to the densification of silver particles. Therefore, one must take into account degradation mechanisms on the die. For example, too high of a temperature can cause aluminum to silicon ohmic contacts to degrade.

SEM observation shows that the attachment to the die is not continuous, that there is a high concentration of lead at the interface between the silver-glass and the substrate, and that adhesion seems to be the result of diffusion of silver into the gold layer. Researchers like Dequidt explained the absence of gold in the silicon and gold-silicon eutectic by the nickel or titanium under-layer preventing migration of gold into the silicon. Similarly, bonds between the silver glass and the plated package are probably interdiffusion mechanisms, whereas bonds between alumina and silver glass are chemical and similar to conventional thick film.

In investigating the process, thermogravimetric analysis (TGA) is used to determine the temperature

[Continued on Page 2]

at which solvents are eliminated from the binder and differential thermal analysis (DTA) is used to characterize the glass and show its recrystallization.

Advancements in silver-glass die attach materials have mainly been focused on:

- stress relief for large area dice
- a single pass firing process with no pre-drying
- precise rheology for high speed dispensing
- lower firing temperature

As with resin attach, the TCE of the bonding material is not a significant factor in die stress. This assumes that the thickness and modulus of the die bonding material is small compared to the thickness and moduli of die and substrate. However, cracks due to thermally induced stresses arising from a TCE mismatch between silicon and ceramic have been reported by Nguyen for die larger than 10mm on a side. Furthermore, the bond line thickness has to exceed a

minimum value for acceptable performance.

The stress in the bonding material is related to the sintering behavior of the silver/lead borate glass mixture. Control of the sintering rate is typically achieved by small quantities (0.1–1%) of proprietary additives which increase the surface roughness and slow down regrouping of the particles. This helps to eliminate cracks without adversely impacting on adhesion and void formation.

Despite the claim that silver-filled glass offers lower cost, faster processing, high yield, better thermal performance, and a lower die stress than gold-silicon eutectic, it has not replaced eutectic or other solders for high power chips. This seems to be because companies are reluctant to change. However, the material is widely used in the fabrication of Ceramic Dual Inline Packages because it resists the high temperature of the furnace sealing involved.



## Ask the Experts

*Q: I've heard that nitric and sulfuric acids behave differently with silicon/CMOS and GaAs technologies. Basically, one or the other acid destroys one (or the other) die. Do you know which acid is compatible with which die type?*

*A: Sulfuric acid tends to be more of a problem with*

GaAs. There is an etch system based on Sulfuric-Hydrogen Peroxide-Water for GaAs. If you can keep any oxidizing agent away (and nitric might act as one in this case if you mix the two) then you shouldn't be etching the GaAs substrate at an appreciable rate with sulfuric acid. In my experience, the bigger problem is etching the metals on the die. Both sulfuric and nitric in conjunction with water will etch aluminum.

To post, read, or answer a question, visit <http://forums.semitracks.com/>.

We look forward to hearing from you!



## Announcements

IRPS 2010

May 2-6, 2010 • Anaheim, CA

For nearly 50 years, the International Reliability Physics Symposium (IRPS) has been the premiere conference for engineers and scientists to present new and original work in the area of microelectronics reliability. [Learn more.](#)

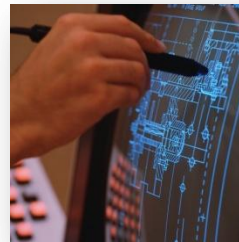
Advanced Materials Failure Analysis

Workshop 2010

May 21, 2010 • Reston, VA

This year's AMFA program consists of presentations covering emerging topics in microelectronics and biotechnology.

Presentations include applications of computed x-ray tomography for microelectronic and biological structures, counterfeit microelectronics issues and risk management, characterization of physical and mechanical properties of amorphous materials, government funding of circuit analysis tools, and visualizing cells and viruses using 3d electron microscopy. The unique capabilities of one community may have surprising results for the other. [Learn more.](#)



## Upcoming Courses

[MEMS Technology](#)

March 8-9 • Cambridge, UK

[Defect-Based Testing](#)

March 24-26 • Malaysia

[Semiconductor Reliability](#)

April 12-14 • San Jose, CA, USA

[Wafer Fab Processing](#)

April 19-22 • Enschede, Netherlands

[Packaging Technology & Metallurgy](#)

May 26-28 • Malaysia



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2. **No travel costs.** Unless you have been on another planet, you know that traveling is no longer very enjoyable (long check-in lines, security screens, cramped seating, poor service, and non-existent amenities). With our online training, you can access material from work, travel, or even home. Plus, as long as you have high speed Internet, a commonly available web browser like Internet Explorer or Mozilla Firefox, and the Adobe Flash player plug-in (version 6.0 or later), you can access our material from anywhere in the world.
3. **No stress.** With our online training website, the material is available 24 hours a day, 7 days a week. You can log on first thing in the morning, at lunchtime, or even at the end of the day once the kids are in bed. When you subscribe to our online training website, you can watch whatever material you would like for up to one year. If you need longer, simply renew your subscription. You'll want to, since we constantly upload new material and update existing material.
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## Technical Tidbit [Megasonic Cleaning]

Two types of mechanical cleaning methods are used in semiconductor wafer cleaning: ultrasonic and megasonic. Ultrasonic cleaning uses frequencies between ten and one hundred kilohertz. The generation and collapse of bubbles creates shockwaves that impact on the surface. The shockwaves can be effective in loosening and removing particles. Most ultrasonic techniques use either de-ionized water or a one-to-one acetone-ethanol mixture. Megasonic cleaning uses higher frequencies, typically between 700 kilohertz and 1

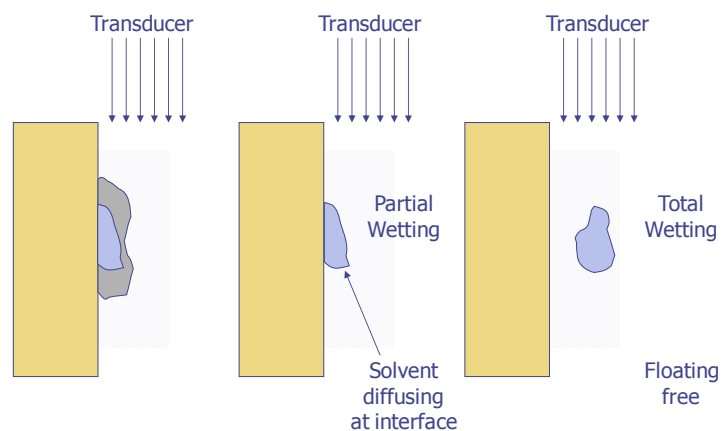
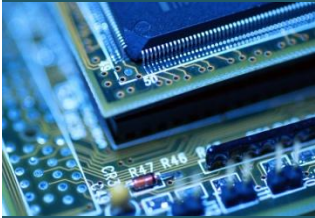


Figure 2. Diagram showing how Megasonic cleaning removes particles.



## Customer Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials or if you wish to suggest a new course or location, please feel free to call us at 1-505-858-0454 or e-mail us at [info@semitracks.com](mailto:info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the December newsletter, please contact Alicia Constant by email at [alicia.constant@semitracks.com](mailto:alicia.constant@semitracks.com).

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megahertz, hence the term megasonic. Megasonic cleaning is becoming more important since the higher frequencies generate smaller bubbles, creating smaller shockwaves, resulting in less surface damage. This technique is safer on fragile materials like low-K dielectrics.

This is a cross-sectional view of a megasonic cleaning tank. The transducer, responsible for generating the sonic energy, is on the right-hand-side. A typical energy for megasonic cleaning is 300 watts at 800 kilohertz. The wafers are placed parallel to the wave action. As the waves pass by, they interact with the surface removing particles. To prevent return wave action, a quartz deflector plate is placed at the

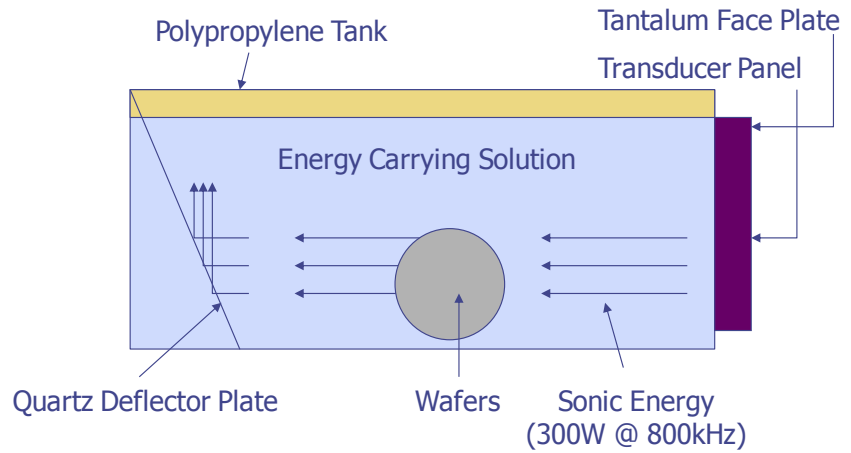


Figure 3. Configuration of Megasonic cleaning system.

left end to deflect the wave action to the surface.

As the wave interacts with the particle, small shockwaves hit the particle. If we perform the megasonic clean in a solvent solution like acetone, the solvent can attack material that might be holding the particle impact. The combination of energy and chemical action speeds up the cleaning process.

## Semiconductor Reliability

### [Course Spotlight]

A semiconductor device is only as good as its reliability: the probability that it will perform its function under specified conditions for a set time. Today's ICs possess shorter lifetimes and reduced reliability margins, and rapid developments have led to the use of materials that are not well characterized. While reliability levels are at an all-time high level in the industry, rapid changes may lead to unintentional failures and the inability to predict when devices might fail.

Your company needs competent engineers and scientists to solve reliability problems. Semitracks' 3-day course on [Semiconductor Reliability](#) offers detailed instruction on how to determine what failure mechanisms might occur, test for them, develop models for them, and eliminate them from the product.

The course covers four main topics:

1. Overview of Reliability and Statistics
2. Failure Mechanisms
3. Test Structures
4. Test Strategies

### What makes ours different?

**Our courses are dynamic.** We use a combination of instruction by lecture, problem solving, and question/answer sessions to give you the tools you need to excel in the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. The course notes offer hundreds of pages of reference material that the participants can apply during their daily activities.

**Our instructors are internationally recognized experts.** Our instructors have years of current and relevant experience in their fields. They're focused on answering your questions and teaching you what you need to know.

**Our analysis instructional videos help you visualize the process.** Semiconductor reliability analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding defects. Many tools output video images that must be interpreted by analysts. Our videos allow you to directly compare material you'll learn with your actual analysis work.

Find out more information by visiting our website, [www.semitracks.com](http://www.semitracks.com). There you can view a course outline, sample slides, and dates of a course near you.