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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In this month's Feature Article, we will continue our discussion of Cleanroom Technology and the topic of storage and delivery of Chemicals and Gases in a Cleanroom. We will briefly cover Water Usage within the fab in this month's Article. When constructing a new cleanroom facility, one must pay close attention to water usage, since fab usage can be quite high. This will play a key role in planning and implementing the delivery system, and determining storage and recycling requirements.

An individual fab can use tens of millions of liters of water per day. To put this into perspective, average water usage in the U.S. is about 82 gallons, or about 310 liters, per person per day, making 40 million liters equivalent to the daily household water consumption of a small city (population 122,000). Figure 1 (below) shows the breakdown of usage in the fab. The largest use of water in a fab (about three-quarters) is process related, with much of that being converted to ultra-pure water (UPW) needed for production itself, followed by the facility scrubber and cooling tower, which are each about 10% of the overall usage. Fabs typically have separate systems for UPW, which can be hot and cold, and lower purity (LP) water. UPW generation is a complex, multi-step process that also consumes significant amounts of power. Most fabs have some level of UPW reclamation, although rates vary widely among fabs and processes within a fab. We will discuss UPW later in this section.

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Upcoming Courses:

- IC Packaging Technology
- Advanced CMOS/FinFET Fabrication

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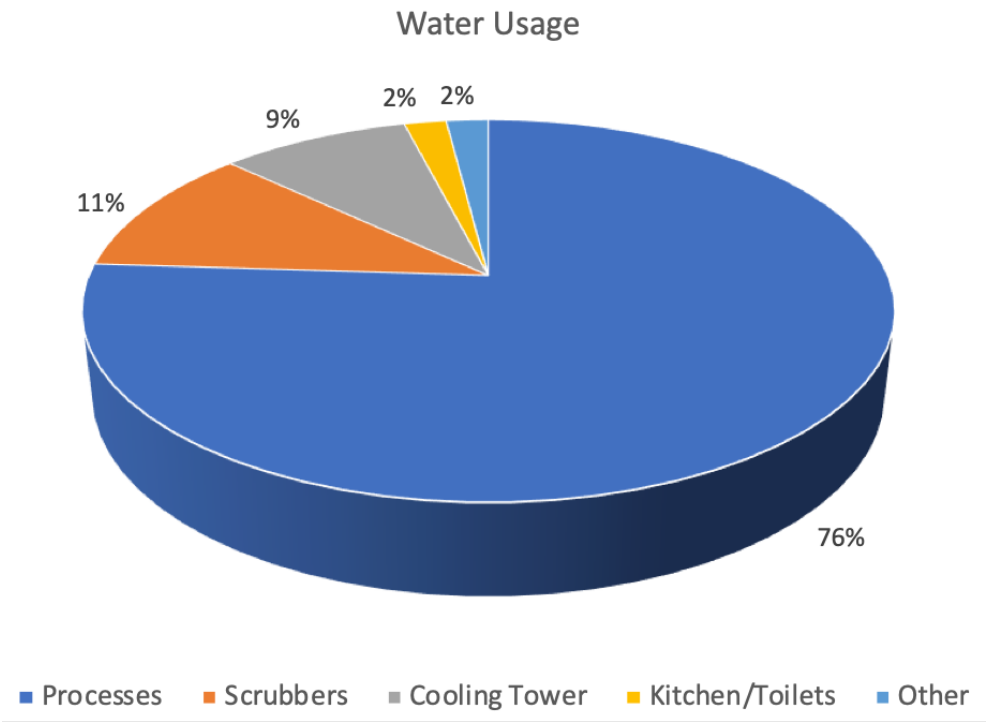


Figure 1- Breakdown of water usage within a modern semiconductor fabrication facility.

Chilled water is a major item used in the fab. It is primarily used for cooling. Since fabs use a lot of chilled water, approximately 10% of the overall water usage, it is important to monitor. The good news is that chilled water can mostly be recycled. Semiconductor chillers have several key differences from a standard "off-the-shelf" chiller. The key differences are found in the method of heat removal, and the features and/or safety mechanisms incorporated into semiconductor chillers.

First is heat removal. Chillers that use electro-mechanical refrigeration remove heat either to the air or to a water source. Most semiconductor manufactures prefer units that remove heat to a water source, known as a water-cooled chiller, as these do not have fans which circulate dust and other small particulates around a cleanroom. Water-cooled chillers are generally designed to use the minimum amount of facility cooling water to produce the needed cooling effect. This is accomplished through proper sizing of the evaporator. For any water-cooled chiller, a minimum amount of water will be required to allow the refrigeration system to operate for a given heat load. It is this low amount of water flow that is targeted to reduce water usage, energy consumption, reduce plumbing sizes, and therefore, material costs.

Next is safety. The biggest difference between an off-the-shelf chiller and a chiller for semiconductor processes, is the SEMI-S2-0703 code. This is a safety code that states what a chiller must include and not include in order to maintain the high safety standard demanded from the semiconductor industry. The key points of this code state the following prerequisites for a semiconductor chiller: a drip tray with 110% reservoir or tank containment capacity; an Emergency Off, or EMO, switch; other safety switches such as tank level, low flow, and high temperature. Other safety monitors include pump overload devices; water quality/purity monitors, such as resistivity or conductivity monitors; monitoring of the facility cooling water; electrical shock mitigation; and seismic restraints.

Ultra-Pure Water, a form of completely deionized water, or DI water, is the most important fluid to control. It is the single most critical process fluid, because a wafer may experience water more than 70 times during processing. A fab may use between 8 to 16 million liters of Ultra-Pure Water, or UPW, every day, which is approximately equivalent to the water use of a city with a population of 40 to 50 thousand. Since wafer fabrication facilities use a lot of ultra-pure water, it is produced in-house from city water. The contaminants that need to be removed include particulates, dissolved minerals, bacteria, and TOC or total organic carbon. The treatments to the city water include: multiple-stage filtration; demineralization, where engineers use reverse osmosis and ion exchange processes to remove minerals; and sterilization. Demineralization increases the resistivity of the water to approximately 18 megohms per centimeter, making it very reactive to copper piping. Therefore, the delivery system for UPW uses high-purity plastic piping. Furthermore, these systems require continuous monitoring of the resistivity and particulate levels. Engineers perform the sterilization by exposing the water to ultraviolet light and ozone. Also, these systems require continuous circulation to avoid bacteria growth. The delivery system, or the process of bringing the water from the plant to the process tools, is a highly critical system that affects wafer yield. Figure 2 shows an example of an in-house UPW system.

Figure 2- In-house Ultra-Pure Water (UPW) generation system.

Figure 3 shows the process flow for creating ultra-pure water. The feed or raw water first goes through a clarifier to remove aluminum and/or iron sulfates. It then goes through sand filtration to remove ammonia and chlorine. These first two steps of purification are done by the city. At this point, the water can continue into the semiconductor plant. Next, acids and scale inhibitors may be added to the water to balance the pH level. Then, the water goes through a heat exchanger and additional filtration to remove particles less than 5 microns in size. The water then goes through two stages of reverse osmosis to remove ions from the water. At this point, the water may be stored for later use. Next, the water goes through vacuum degasification, followed by total organic carbon removal and ultraviolet irradiation to kill bacteria and other living organisms. Additional ion removal occurs in a primary ion exchange bed, followed by additional radiation to remove any remaining bacteria. There is another filtration step to remove particles less than 1 micron in size,

followed by storage. At this point, the water is now classified as purified deionized water. After additional total organic carbon removal, irradiation and filtration steps, the water is ready for manufacturing. After the manufacturing process, there may be an ozone treatment to allow for reuse in certain circumstances.

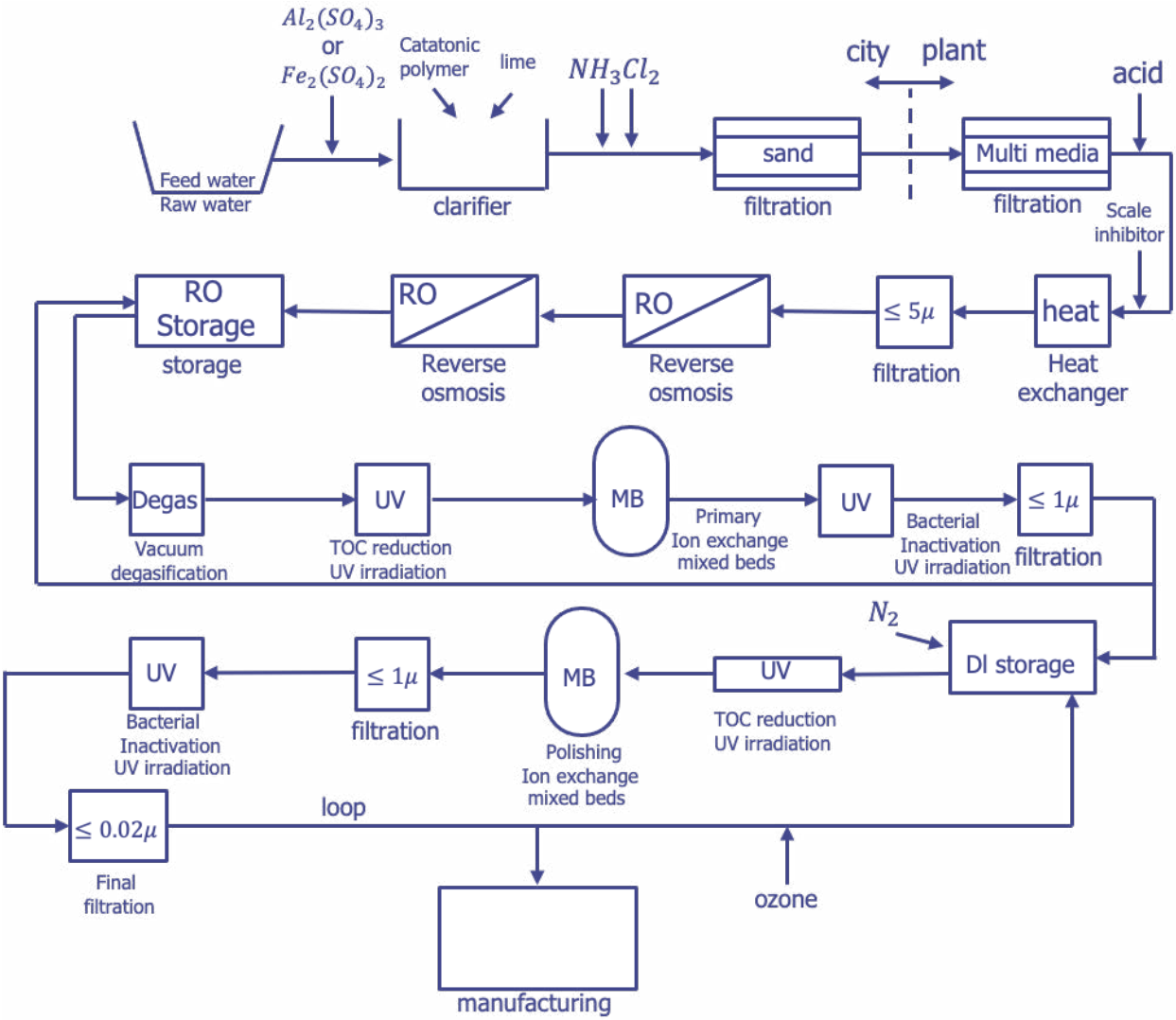


Figure 3- Process flow for creating ultra-pure water.

Bulk Chemicals and Gases, and Purified Water are often stored and delivered from a Central Utility Plant. Depending on the site configuration, the Central Utility Plant may be located adjacent to a single cleanroom facility, or in between multiple cleanroom facilities on the site, like we show in Figure 4.

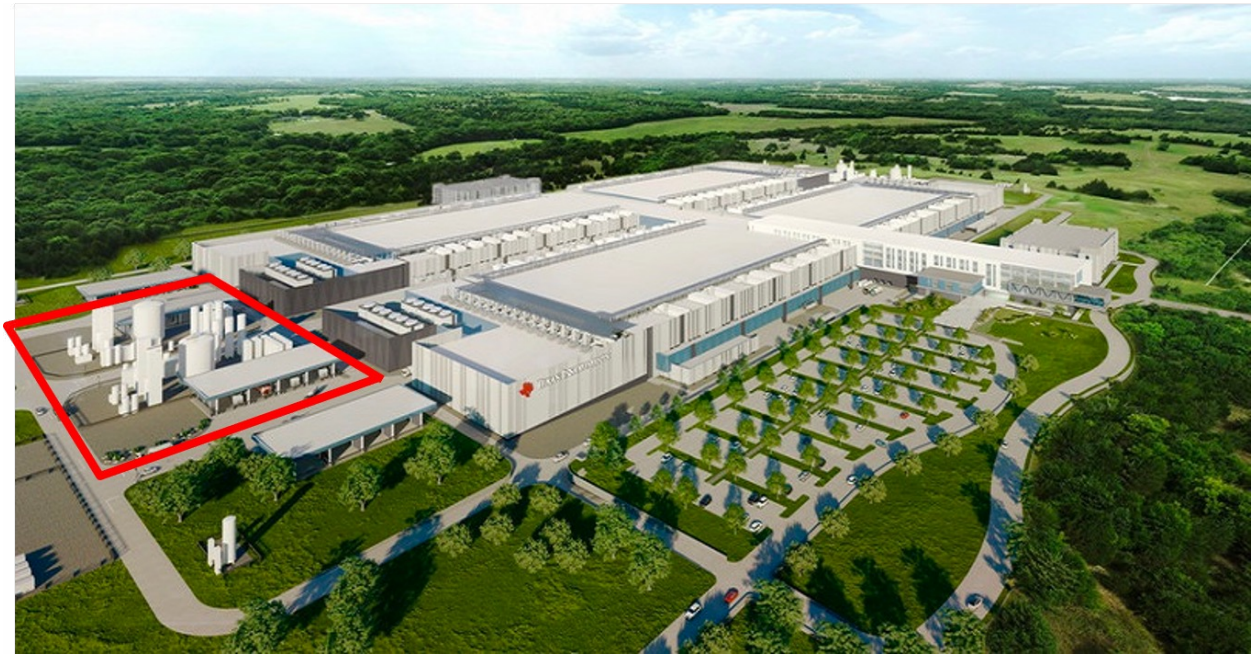


Figure 4- Location of the Purified Water storage and delivery system.

While there are many options available to semiconductor manufacturers with respect to bulk Gas installations, the primary driver is correctly sizing the demand. Adequate supply must be available for the fab, but without excess, so that cost is optimized. Once demand is calculated, two other major project requirements can be determined: land and utilities. Let's now touch on these three factors in a little more detail. First, let's discuss demand. Well-established manufacturers have existing fabs and processes from which they adapt and scale the Gas demand and purity requirements for new fabs. New manufacturers, or those with new processes, need to make estimates based upon OEM recommendations and engineering models. In addition to average demand, peak demand – associated with recovery from an unplanned shutdown – must be calculated. Lastly, redundancy and back-up storage requirements are added. The aggregate demand and purity determine cost, and drive the optimized equipment solution. Next, let's discuss land requirements. Once the equipment solution is determined, the footprint of land can be calculated. The manufacturer will need to include the area of the Central Utility Plant in their overall land requirement. The Gas yard can be contiguous to the fab site, or can be located on a separate parcel several kilometers distant. However, higher delivery pressures and larger pipeline diameters are needed the greater the separation of generation and use. Equipment plus land are the major capital expenses of the project. Finally, let's discuss utilities requirements. The equipment solution will also determine the utility requirements, which are primarily electrical power, water, and, potentially, natural gas for hydrogen generation. These, too, must be determined and included in the overall utility supply to the fab site.

In conclusion, we discussed the use of Purified Water in semiconductor manufacturing, and how it affects cleanroom design and construction. Semiconductor fabs use large amounts of chilled and UPW, so generation, storage, distribution, and recycling are an important part of the cleanroom design and construction. In next month's Feature Article, we will the topic of Access to the Cleanroom.

Technical Tidbit: The Return of Electron Beam Probing

In this month's Technical Tidbit, we will discuss the return of Electron Beam Probing as a fault isolation tool for Failure Analysis. Electron Beam Probing was a common technique for fault isolation in the late-1980s and early-1990s, but fell out of use in the mid-1990s. We will discuss why it has returned to use for modern integrated circuits.

In order to perform Electron Beam Probing, the interaction of the electron beam needs to reach the interconnect or structures of interest. In the mid-1990s, many advanced IC designs moved to a "flip chip" format, where the die is placed in the package upside down. This allows for shorter connections within the package, and the elimination of bondwires to provide connections between the die and the package leadframe. This in turn facilitates high frequency devices, high pin-count devices, and better heat removal from the die. In order to address the need for fault isolation, new optical beam techniques were developed. Optical Beam Probing in the Near Infrared frequency ranges allow for the beam to transmit through the silicon to interact with structures in the silicon, like diffusion and implant regions. However, the Optical Beam is stopped by metallization, so significant amounts of frontside metallization preclude the use of Optical Beam Probing from the frontside of the die. For more information on these techniques, one can consult our Online Training System for more details.

The advent of technologies like Backside Power Distribution is now creating additional limitations with backside Optical Beam Probing. We show a comparison between Frontside Power Delivery and Backside Power Delivery in Figure 1.

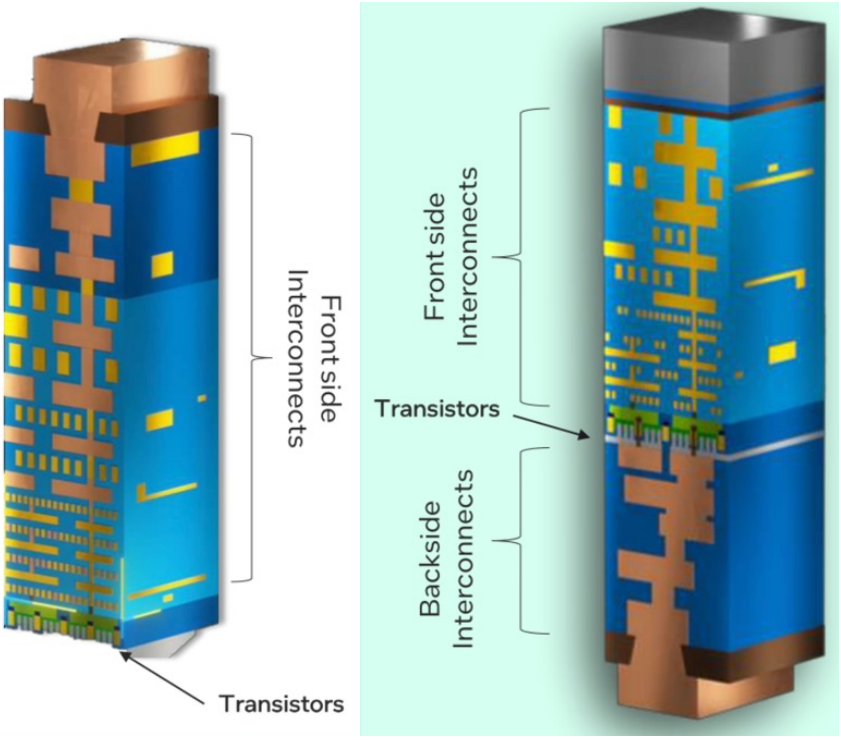


Figure 1- A comparison between Frontside Power Delivery (left) and Backside Power Delivery (right). Figures courtesy Intel Corp.

As was the case with metallization from the frontside, metallization from the backside prevents the optical beam from penetrating to the active structures in the silicon, preventing signal generation, like we show in Figure 2.

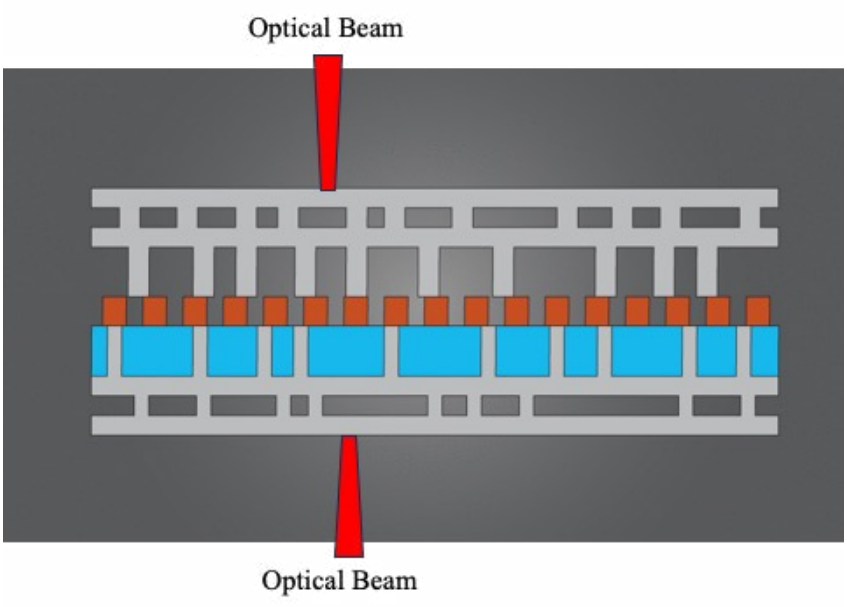


Figure 2- Limitations of Optical Beam Probing.

Electron Beam Probing, in conjunction with deprocessing techniques, can allow the analyst to overcome some of these problems. The Electron Beam can penetrate through some material, allowing buried structures to be reached. Also, the Electron Beam has a smaller spot size than one can achieve with Optical Beam Probing, allowing for better resolution. We show those advantages in Figure 3. The biggest limitation with Electron Beam Probing is the interaction volume between the Electron Beam and the sample. Even at high voltages, the depth the Electron Beam can penetrate is no more than 5 microns. This means that the structure to be probed needs to be close to the outer surface of the sample. Techniques like Laser Microchemical Milling and Focused Ion Beam milling can remove material from the same so that the Electron Beam can reach the structures of interest.

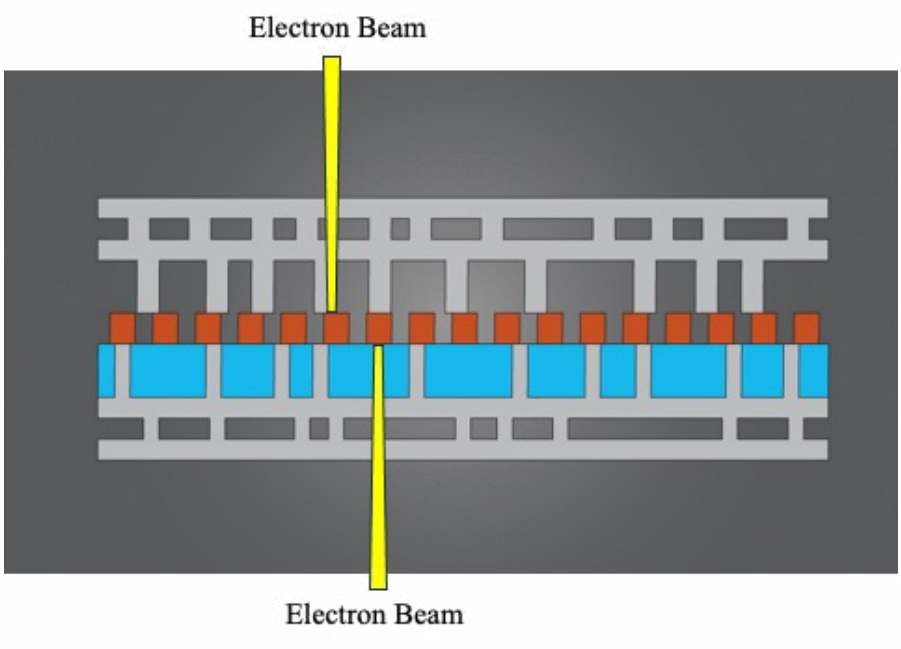


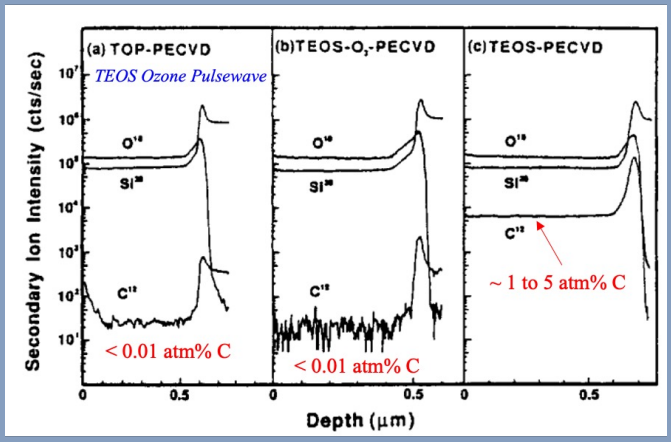
Figure 3- Advantages of Electron Beam Probing.

In conclusion, as ICs become more and more complex, different approaches are required to analyze failures. Sometimes it can be useful to "revisit" existing techniques from the past to see if they can be used in new and innovative ways to solve analysis problems. The use of Electron Beam Probing is just such as example. Sometimes in the semiconductor industry, we use outdated process technologies to accomplish new things. This leads to the phrase "what is old is now new again." The current use of Electron Beam Probing is definitely an example of this phrase.

Ask The Experts

Q: How much Carbon is in TEOS-based SiO2?

A: Thanks for your question. The amount of carbon that is present is highly dependent on the type of deposition process used, along with the specific variables and conditions surrounding the deposition process. Here is data from NEC in Japan from a number of years ago that shows a specific set of examples you can use for reference purposes.



Reference: Y. Ikeda et al., "TOP-PECVD": A New Conformal Plasma Enhanced CVD Technology using TEOS, Ozone and Pulse-modulated RF Plasma", IEDM, 1992, p. 289-292.

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Course Spotlight: DEFECT-BASED TESTING

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's application-specific ICs and microprocessors can contain upwards of 100 million transistors. Traditional testing relies on the stuck-at-fault (SAF) to model defect behavior. Unfortunately, the SAF model is a poor model for defects. Other models and strategies are required to catch killer defects on integrated circuits. As transistor sizes decrease, the types and properties of the killer defects change. This has created a number of challenges related to the testing of components. Defect-Based Testing is a 2-day course that offers detailed instruction on the electrical behavior and test strategies for integrated circuits. We place special emphasis on electrical behavior, fault models, and test techniques. This course is a must for every manager, engineer, and technician working in IC test, IC design, or supplying test hardware and software tools to the industry.

By focusing on the fundamentals of circuit behavior and the impact of defects on circuit behavior, participants will learn how to design, write, and implement test strategies to catch defects. Our instructors work hard to explain semiconductor test without delving heavily into the complex algorithms and computer science that normally accompany this discipline.

Participants will learn basic, but powerful, aspects about defect-based testing. This skill-building series is divided into four segments:

1. **Electrical Behavior of Defects.** Participants will study the electrical behavior of defects. They will learn how open circuits, resistive vias, shorts, and transistor variations affect the electrical behavior of the individual transistor, as well as gate elements and larger blocks.

2. **Fault Models for Defect-Based Testing.** Participants will learn about the historical underpinnings of the stuck-at-fault (SAF) model. They will also learn about other testing models, including IDDQ testing, at-speed testing, and delay testing.

3. **Production Test Methods.** Participants will learn about standard digital testing, SAF testing, IDDQ, timing, low voltage tests, and other types of stress tests. They will explore the strengths and weaknesses of each test type.

4. **The Economic and Quality Impact of Defect-Based Testing.** Participants will learn how defect-based testing can actually improve test economics. They will also study the impact on quality and reliability.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of defect-based testing and its technical issues.

2. Participants will understand the basic concepts of test economics, yield, test time and the cost of test. They also learn how defect-based testing can reduce the possibility of failures in the field.

3. The seminar will identify underused test techniques like IDDQ and Very Low Voltage (VLV) test techniques that can successfully find defects that are difficult to catch using conventional test techniques.

4. The seminar offers the opportunity to discuss specific test problems with our expert instructors.

5. Participants will be able to identify basic and advanced principles for defect-based test.

6. Participants will understand the difficulties in extending IDDQ testing to leading edge products and how to overcome some of these limitations.

7. Participants will become familiar with Design for Test (DFT) and Automatic Test Pattern Generation (ATPG) tools used for defect-based testing.

8. The seminar will introduce fundamental and advanced concepts related to extending defect-based testing to future designs.

9. Participants will learn what tools are available today to implement defect-based testing.

COURSE OUTLINE

DAY 1

1. What is Defect-Based Testing?
    a. Introduction
    b. Terminology
    c. Existing test techniques

2. CMOS IC Defect Mechanisms and Detection Techniques
    a. Normal transistor and gate behavior
    b. Sources of random and systematic defects
    c. Types of Defects and How to Detect Them
        i. Bridging defects
        ii. Resistive defects
        iii. Open circuit defects
        iv. Delay defects

3. Fault Models for Defect-Based Test
    a. Stuck-at-fault (SAF)
    b. Delay fault

DAY 2

    c. Leakage fault
    d. Methods for implementing fault models
    e. Existing software tools

4. Production Test Methods
    a. Functional testing (At-speed testing)
    b. IDDx Testing
    c. Timing Test
    d. Low Voltage Testing
    e. Stress Testing

5. Defect-Oriented test Economics and Product Quality
    a. Test set reduction
    b. Effectiveness in catching defects
    c. Yield and fallout

6. Case Histories

Upcoming Courses:

Public Course Schedule:

IC Packaging Technology - January 23-24, 2024 (Tues.-Wed.) | Phoenix, Arizona - $1,295

Advanced CMOS/FinFET Fabrication - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $995

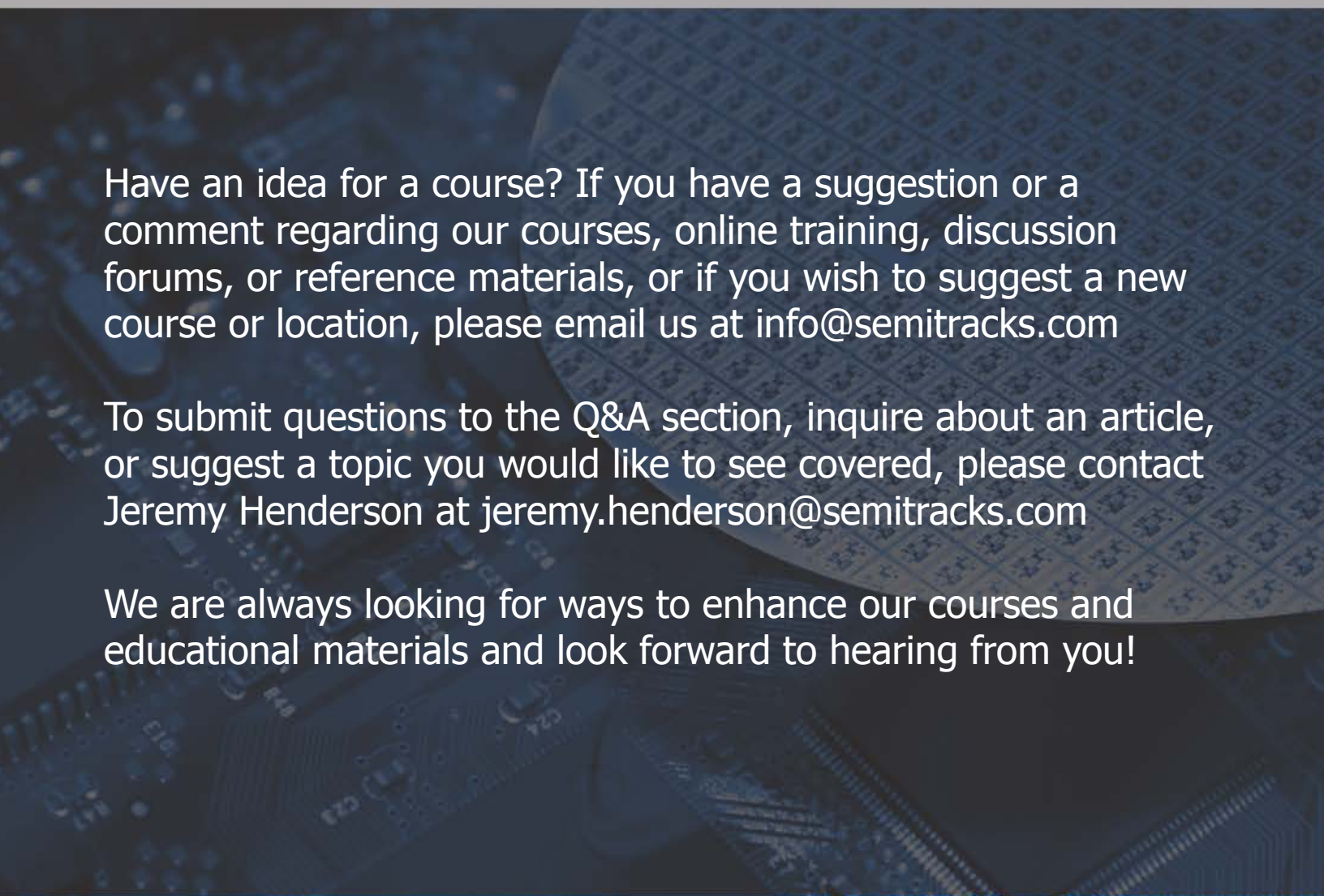
Fundamentals of High-Volume Production Test - January 29-30, 2024 (Mon.-Tues.) | Phoenix, Arizona - $1,295

Wafer Fab Processing - February 26-29, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Failure and Yield Analysis - March 4-7, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Semiconductor Reliability and Product Qualification - March 11-14, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095

Defect-Based Testing - March 20-21, 2024 (Wed.-Thurs.) | Munich, Germany - $1,195



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!