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Electronic Design Automation Tools Part 2

By Christopher Henderson

This article provides an overview of the Electronic Design Automation (EDA) design tools. The EDA industry is an interesting ecosystem and bears discussing, so that the design engineer can understand the environment.

In last month's feature article we discussed the three major EDA tool suppliers: Cadence Design Systems, Synopsys, and Mentor Graphics, which is now owned by Siemens. Here in Part II we will briefly discuss interoperability issues between the three major platforms. We'll also discuss other suppliers developing tools in this area. Finally, we'll discuss the use case and the strengths and weaknesses of the tool suites.

Each of the three major EDA firms creates products that work well within their own portfolio, but what about across the three major providers? What if you want to create designs using tools from across two or more of the providers? This is a major challenge because it requires that one work with different formats for different files, which requires translators, scripts and additional programs. What would be most useful is a good interoperability standard, and the good news is that there is one. It is called OpenAccess and is supported and promoted by the Silicon Integration Initiative. OpenAccess actually had its start as the result of a lawsuit against Cadence. Users sued Cadence, claiming that their internal format gave them a controlling monopoly in the design area, and a judge agreed with them. As a

In this Issue:

Page 1	Electronic Design Automation Tools Part 2
Page 5	Technical Tidbit
Page 8	Ask the Experts
Page 10	Spotlight
Page 13	Upcoming Courses

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result, the courts forced Cadence to make their software more accessible to others. The way that Cadence complied with this order was to place their database into the public domain, and that database is now called the OpenAccess database.

The Silicon Integration Initiative—or Si2 (www.si2.org) as they normally call themselves—maintains the OpenAccess database.

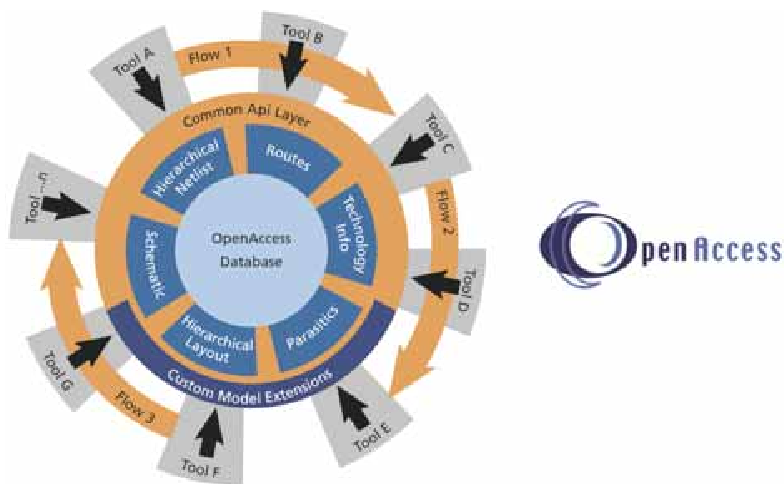

Figure 5. The OpenAccess Standard.

The OpenAccess standard API and reference database implementation is developed through the OpenAccess Coalition, an organization of the world's leaders in IC design. The OpenAccess interoperability platform is based on a common, open and extensible architecture that allows the integration and use of the most effective design tools available from multiple vendors to support the design of complex digital, analog, and mixed signal ICs. A common API enables a unified information backbone for the semiconductor industry.

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There is an industry-wide body called the OpenAccess Coalition that Si2 organizes to help in this effort. Cadence still provides updates to Si2, but Si2 does the bulk of the maintenance and documentation for using the Database. One can access the database through class libraries and through scripting languages, like C++, Perl, Tcl and Python. Many engineers will use scripts to perform different types of tasking, while tool developers might interface with the database through the class libraries when developing a new tool.

Here we list a number of the more minor players in the EDA industry.

- Agnisys — IP Design/Verification
- Aldec — HDL Simulation
- Altera — FPGA Design Tools
- Ansys — Modeling Software
- EMWorks — EM Simulator
- Dolphin Integration — IP Design
- Ferrochip — Magnetic Simulation
- Intellitech — Si Debugger
- Invionics — Custom EDA Tool Builder
- JEDA Technologies — SystemC Tools
- juspertor — Layout/Design Tools
- Keysight — Electrical Modeling
- Lauterbach — InCircuit Debug
- VisualSim Architect — ESL Modeling
- NanGate — Standard Cells IP
- National Instruments — Simulation
- POLYTEDA — DRC & LVS
- Silvaco International — TCAD and other modeling tools
- Solido Design Automation — Monte Carlo Simulation
- Teklatech — SoC Optimization
- Xilinx — FPGA Design Tools

Some of these companies are spin-outs from the major EDA providers, while others are start-ups based on an idea from a university project or some other effort. Some of these companies have been independent for a while but, as we explained near the beginning of this presentation, the companies are likely to be bought by the major players should their tools become successful.

Here are some of the minor EDA players at the Printed Circuit Board level.

- Altium — PCB Design
- EasyEDA — PCB Design
- AutoTRAX — PCB Design
- Eremex — PCB Design/Layout
- gEDA — PCB Layout
- Ing.-Buro FRIEDRICH — PCB Layout
- KiCAD — PCB Layout
- National Instruments — Simulation
- Pulsonix — PCB Design/Laout
- Upverter — PCB Layout
- Zuken — PCB, Cable Design

The three major EDA companies all have efforts at the PCB and system level, so these companies are possible takeover targets as well.

Let's move on and discuss use case issues. Many people new to chip design might ask, is there a difference between the three major EDA providers? Some might also ask, should I use a low cost provider instead of one of the major providers? Still others might ask, can I pick and choose tools, and is that a good idea? The answers to these questions are complex, but there are some general factors of which one should be aware. First, major companies will typically develop a flow using one or more providers, so if you are working with a major company, the chip design process is likely to be defined for you, and these questions are probably not relevant. Second, startups will quite often use one provider to simplify the

interaction. Since tool licenses from the three major EDA suppliers are very expensive, most startups can only afford a basic set of tools. There are exceptions however.

If you are part of a team deciding which tools to use, there are many issues to think about. For example, what technology node do you plan to use? What foundry do you plan to use if you are a fabless company, or if your company is using the services of an outside fab? Do you plan to use multiple foundries to reduce risk? Are you using intellectual property blocks or cores? These factors will play a role in what makes sense to do. Because chip design at the leading edge is so complex, different EDA firms will partner with different foundries at different technology nodes. Therefore, there may be limited EDA options if you want to use a particular foundry and/or use a particular technology node. Second, different EDA firms will partner with different IP providers at different nodes. For example, you may want to use a particular core, like an ARM core. This ARM core may have only been demonstrated to work in particular processes with particular foundries, so this would be another limiting factor. If you are deciding on a tool flow, these issues should be addressed before choosing the tool providers, if you're not already using an EDA provider.

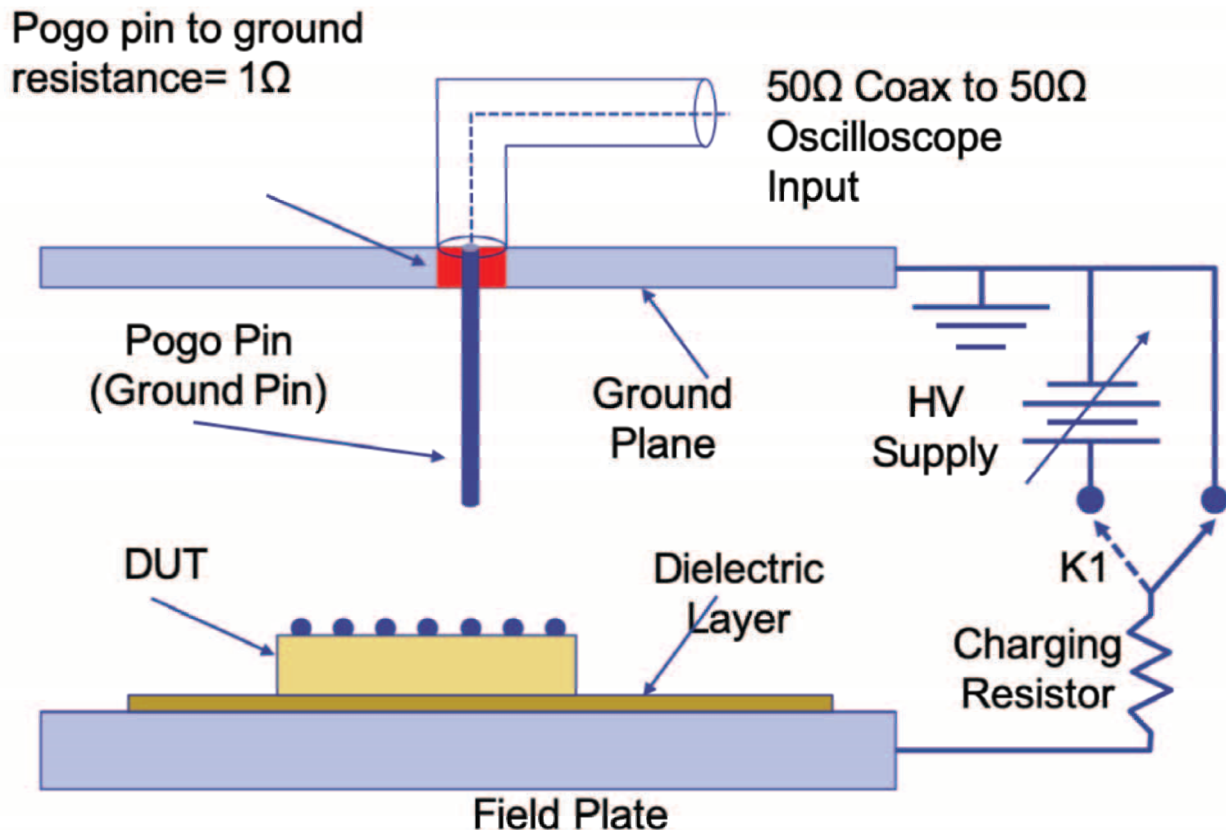
Should I choose a low-cost provider? Given the cost of licenses from the major tool providers which can easily run into the hundreds of thousands of dollars, does a low-cost provider make sense? Here are some of the major concerns to think about. Will you have support from the foundry? The tool provider may not have been able to afford a thorough check of their software to create working designs at a particular foundry. Does the EDA company provide an end-to-end solution? If not, you may need to integrate other tools into your flow. If it doesn't provide an end-to-end solution, does the EDA company operate well with other EDA providers? You will need to get outside opinions on this question in order to get an unbiased answer. Here are some recommendations regarding low-cost EDA providers. If you are designing a simple chip like a sensor, a low cost provider can work fairly well. If on the other hand you are designing a complex SoC, you should use one of the big three EDA tool providers and their recommended flow to help improve your chances at a first or early pass design success.

Should you pick and choose tools? The upside is that you might be able to gain advantages by using the "best of breed" from the different suppliers, but there are concerns here. The formats will likely be different between tools, so this will require scripts or translators to transfer data back and forth. There is always the risk of errors when translating files. You can potentially use OpenAccess to address this issue at the netlist, schematic, or layout levels, but translating a high-level abstraction of the design in HDL may be more problematic. At the Electronic System Level there are definitely not good options, as there are no robust standards for ESL as of this writing.

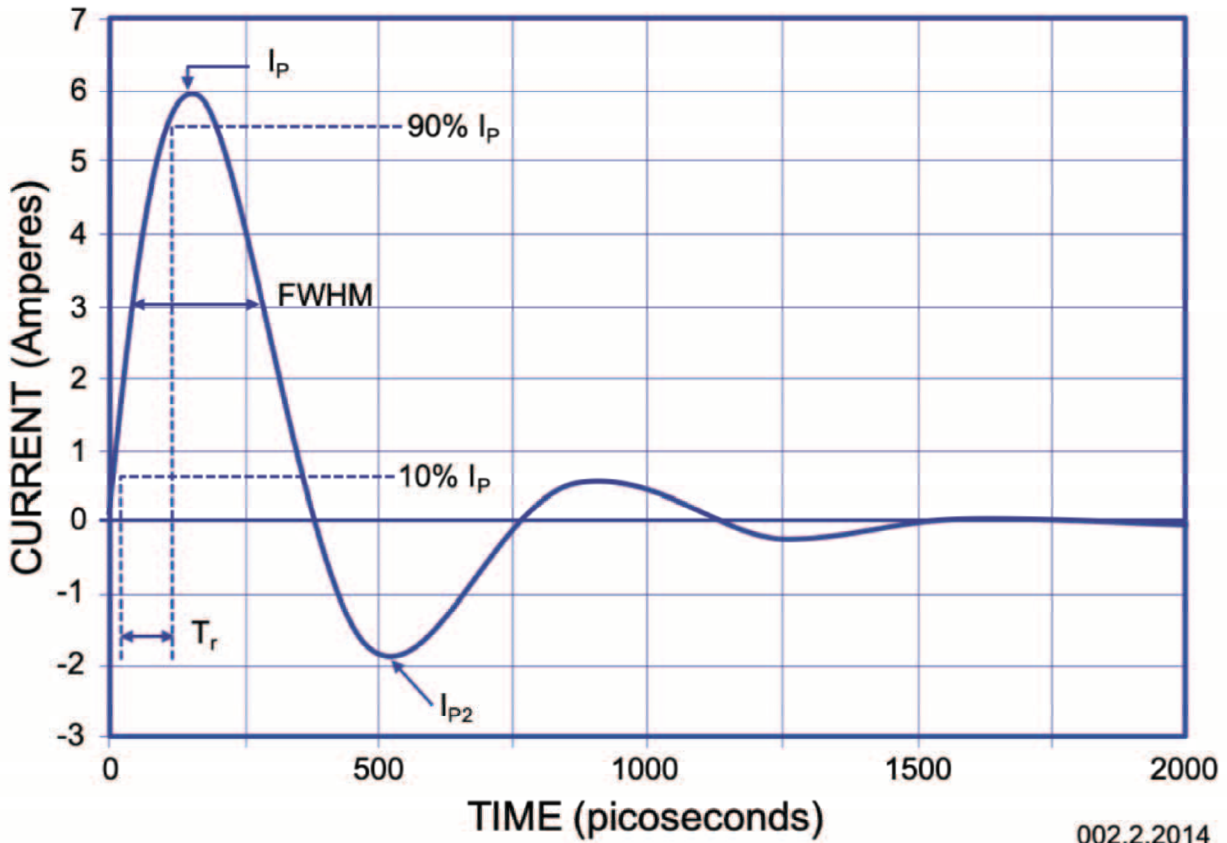
Technical Tidbit

CDM ESD Testing

In this month's technical tidbit, we will give a brief overview of Charged Device Model ESD Testing.



This diagram shows the hardware schematic for the ANSI JEDEC joint standard for charged device model testing. One uses a pogo pin to ground, with one ohm resistance, as the discharge pin. We place the device under test, or DUT pins or pads up on a thin dielectric layer, and use the high voltage circuitry, shown at the right, to charge the device under test using a field plate. One can use 50 ohm coaxial lines to a 50 ohm oscilloscope input to measure the waveform.



This is an example of the expected waveform for a CDM discharge pulse. We characterize the rise time as the time between 10% and 90% of the peak current, or IP. We measure the Full Width Half Maximum at the 50% peak current value.

6+GHz BW Oscilloscope		**Test Condition**									
Verification Module	Sym.	TC 125		TC 250		TC 500		TC 750		TC 1000	
Verification Module	Sym.	Small	Large	Small	Large	Small	Large	Small	Large	Small	Large
Peak Current (A)	I_p	1.4-2.3	2.3-3.8	2.9-4.3	4.8-7.3	6.1-8.3	10.3-13.9	9.2-12.4	15.5-20.9	12.2-16.5	20.6-27.9
Rise time (ps)	Tr	<250	<350	<250	<350	<250	<350	<250	<350	<250	<350
Full width at half maximum (ps)	FWHM	250-600	450-900	250-600	450-900	250-600	450-900	250 -600	450-900	250-600	450-900
Undershoot (A, max. 2nd peak)	I_p2	<70% I_p	<50% I_p	<70 % I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p	<70% I_p	<50% I_p

The waveforms shall appear as shown in the previous figure for both the positive polarity and its inverse for the negative polarity. The average waveform parameters, including IP, as gathered shall meet the specifications in this table for a 6 GHz high bandwidth oscilloscope. The standard also contains a table for a 1GHz bandwidth oscilloscope. If a high bandwidth oscilloscope is used for qualification, quarterly, and routine waveform verifications, the 1 GHz requirements need not be considered.

Classification Level	Classification Test Condition (in Volts)
C0a	< 125
C0b	125 to < 250
C1	250 to < 500
C2a	500 to < 750
C2b	750 to < 1000
C3	> 1000

ESD sensitive devices are classified according to the test procedure described in this standard. CDM test results are specific to the particular package type used. The device classification is the highest ESD stress voltage level (both positive and negative polarities) at which a sample of at least three devices has passed full static and dynamic testing per data sheet parameters following ESD testing. The CDM ESD sensitive device classification levels are presented in this table. Please note that the standard uses the "C" prefix to indicate a CDM classification level. Also, the Classification Test Condition is not equivalent to the actual set voltage of the tester. Please see Section 6.5.1 and Annex G in the standard for further details.

Ask the Experts

Q: Why do people sometimes call the FinFET a triple gate device?

A: Early on in the development of the FinFET, engineers thought of the device as having a left surface, a top surface, and a right surface. Today, the fins are very tall and extremely narrow, so the contribution from the top surface is becoming negligible.

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Chris Henderson, Semitracks President

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Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

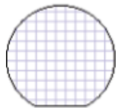
COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues

4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
5. FinFET Reliability
    a. Defect density issues
    b. Gate Stack
    c. Transistor Reliability (BTI and Hot Carriers)
    d. Heat dissipation issues
    e. Failure analysis challenges
6. Future Directions for FinFETs
    a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
    b. Scaling

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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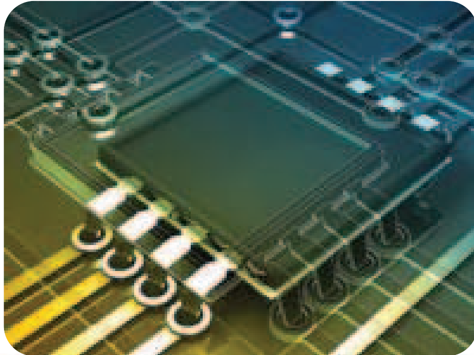

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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Upcoming Courses

(Click on each item for details)

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Failure and Yield Analysis
March 2 – 5, 2020 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
March 4, 2020 (Wed)
Portland, Oregon, USA

IC Packaging Technology
March 5 – 6, 2020 (Thur – Fri)
Portland, Oregon, USA

Semiconductor Reliability / Product Qualification
March 9 – 12, 2020 (Mon – Thur)
Portland, Oregon, USA

Wafer Fab Processing
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 30, 2020 (Thur)
Munich, Germany