Issue 102 December 2017

InfoTracks

Semitracks Monthly Newsletter

Fault Diagnosis Algorithms Part 1

By Christopher Henderson

In this article we will discuss fault diagnosis algorithms. Fault diagnosis algorithms are used to predict where failures might occur and locate failures on ICs. We'll discuss the role of a diagnosis algorithm, scoring methods associated with faults that the diagnosis algorithm finds, and the types of diagnosis algorithms.

A diagnosis algorithm is designed to compare the observed behavior on the tester with predicted behaviors gathered from fault simulation or fault dictionaries. The algorithm essentially tries to match the failure observed on the tester with a defective condition identified through fault simulation or the fault dictionary. The algorithm is designed to report the best possible fault candidates. The algorithm uses a scoring method to find the best fitting "fault" to the failing data.

Scoring can be done by a number of different methods. Two common scoring methods include match and mismatch points, and fault candidate probability. Some other common methods include hamming distance, set intersection overlap, and nearest neighbor. Hamming distance is the number of bits that have to change from one binary value to make it another binary value. The Nearest Neighbor technique first selects a single failed run, and computes the passed run that has the most similar code coverage. Then it creates the set of all statements that are executed in the failed run but not in the passed run.

In the match and mismatch point scoring method, one is awarded

In this Issue:

Page 1	Optical Pyrometry Part 1
Page 6	Technical Tidbit
Page 9	Ask the Experts
Page 10	Spotlight
Page 15	Upcoming Courses

points for matching observed failures. One can also optionally deduct points for not predicting failures. A non-prediction is a behavior not predicted by a candidate fault, and a mis-prediction is a prediction not fulfilled by the behavior of the fault. Mentor Graphics FASTscan is an example of a tool that uses this method. It is biased to lowest non-prediction.

In the probabilistic scoring method, the probability score is based on matches, mismatches and error assumptions. There are weights for non- and mis-prediction, and different prediction probabilities for different fault candidates; for example, bridging faults versus stuck-at faults. This is normalized so that the total of all candidates equals 1. David Lavo, a UCSC researcher, used this method to compare stuck-at candidates to bridges in the same diagnosis.

Diagnosis algorithms fall into two main groups: stuck-at and IDDQ. There are also diagnosis algorithms for other types of defects like open circuit or delay defects as well. The stuck-at diagnosis algorithm is the most common, since it deals with digital data and is therefore best supported by design tools. It is quite effective. A good algorithm can usually find exact matches at least 60% of the time. It is also very fast. IDDQ is another type of diagnosis algorithm. It is not as common and not as well supported by design tools. It also requires interpretation of tester results. It is a different set of test data, so it does provide additional capabilities beyond the stuck-at fault algorithms.

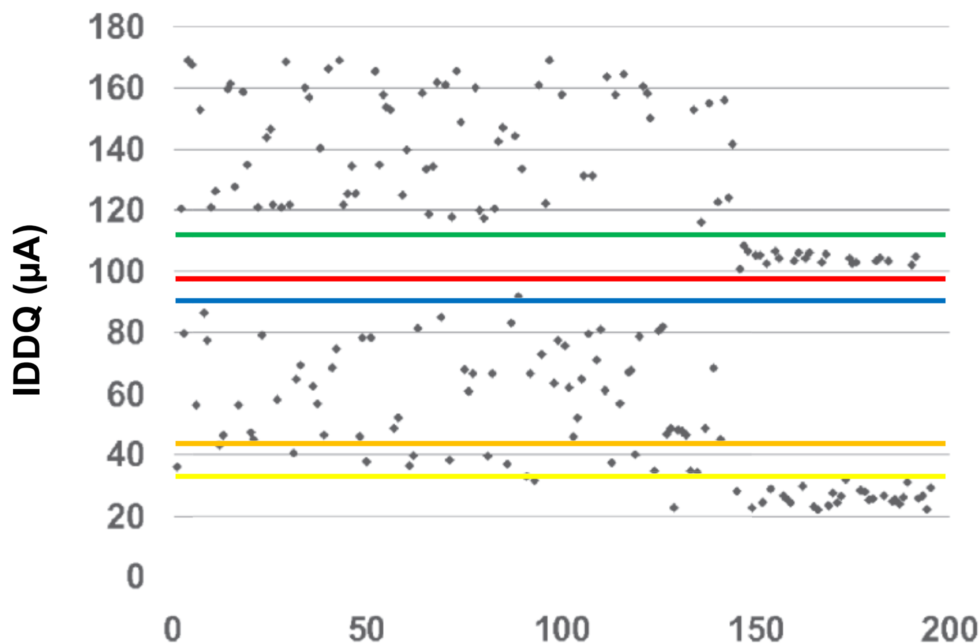


Figure 1. IDDQ threshold setting.

One of the biggest problems with IDDQ fault diagnosis is where to set the boundary or threshold between pass and fail. In this graph we show IDDQ values for approximately 200 vectors. The vectors appear to be clustered into two different groups: one above 100A and the other below 100µA. We could place the threshold here (red line). Perhaps though the limit should be some distance further below to provide margin, like this (blue line). However, this results in the inclusion of an additional point. Perhaps the later vectors that have values clustered between 100 and 110µA are actually good. This would argue for setting the limit higher, like this (green line). It could be that the scatter is associated with a problem that should be examined. This would argue for a threshold that is much lower, like this (orange line), or this (yellow line). Choosing an IDDQ threshold is a major challenge, and is addressed further in the IDDQ testing section.

Another type of diagnosis algorithm is the bridging fault algorithm. The bridging fault diagnosis algorithm may better represent CMOS faults, but it is a more complicated model. The biggest problem is candidate selection. Bridging defects each have a unique resistance, and therefore a unique effect on the IC. It can be difficult to select a candidate because of this. Some other possible fault diagnosis algorithms include algorithms based on functional failures, delay failures, or other parametric failures. These ideas are now fairly well developed and are now being turned into commercial algorithms to be placed in products.

Let's walk through the process of using a diagnostic algorithm to localize a failure on an IC. We'll talk about how to use the diagnosis, how to translate the results from a node into a circuit location, and how to evaluate the quality.

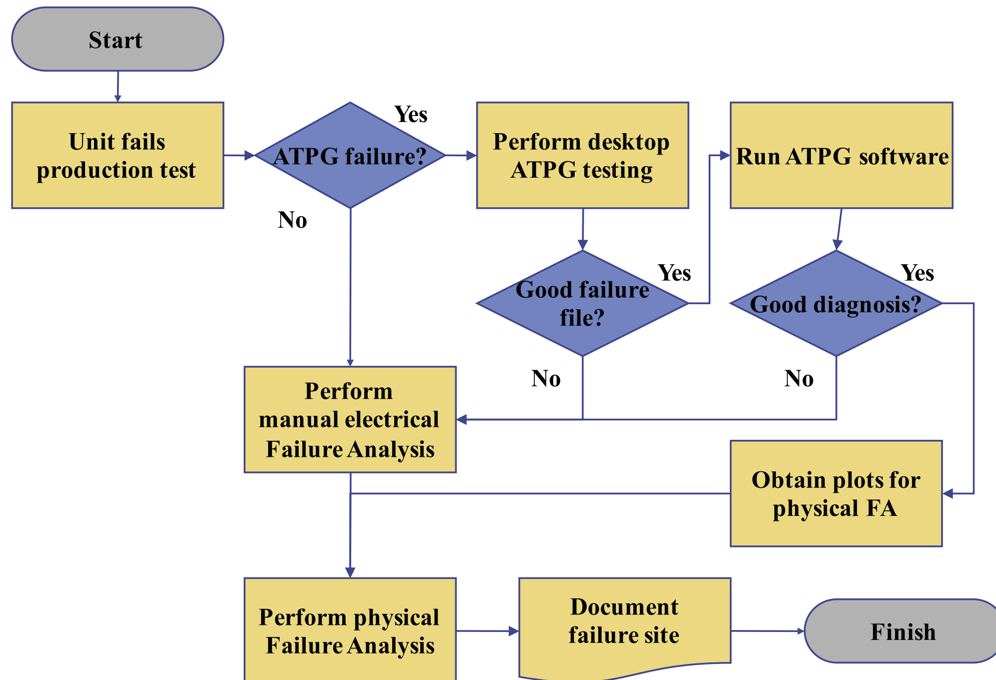


Figure 2. Flowchart for ATPG diagnosis process.

This is the basic flowchart for the Automatic Test Pattern Generation Diagnosis Process. Once the device has been verified as a failure, the scan chains must be verified. If the failure affects the scan chains, then the results of the fault simulation will be inaccurate. Normally, the software simulates selected faults to determine the set of faults whose simulated failures most closely match the actual failure. In the case of a real failure, we instead perform desktop ATPG testing using a less expensive structural or scan test system and capture a failure file. If the file contains observable failures, then the ATPG software can be run and compared against the desktop ATPG results. If the ATPG software results yield a good diagnosis, then one can bypass the time-consuming manual fault isolation activity. One can simply obtain the plots of the suspect nodes and go directly to the physical characterization step.

The most common way to use a fault diagnosis is to aid in the localization of the failure site so that one can go directly to physical inspection and root cause identification. The diagnosis output is logical and tied to a node, or a gate. There is no information regarding location or size. One must translate from a node or gate port to a physical location to be able to locate the defect.

There are three ways that one can navigate a complex circuit: using the netlist, using the schematic, and using the physical layout features. Netlist navigation involves using the register transfer language like VHDL or Verilog to locate gates and data paths. A common format for this type of navigation is the SPICE format. One can follow the data path through gates and along nodes, as well as traverse the hierarchy of the chip. Schematic navigation uses a symbolic view of the gates and wires. This can be much easier for a design engineer to interpret over a netlist view, since the gates are displayed with their defined shapes, rather than as rectangles. Layout navigation uses the polygon shapes associated with the metal lines, vias, polysilicon, diffusions and implants to allow the user to examine the circuit. A common format for this type of view is GDSII.

```
module TOP (CLK, Reset, StartOut, SiReady, Rst_CntN, Up_DnN, Wr, SDin, Wr_RAM, Wr_Rreg,
RAM_Addr, ATG_TESTMODE, BIST_TESTMODE, SDout,  TwoOnes, OneOne, NoOnes, TwoZeros,
OneZero, NoZeros);

input               CLK;
inout      Reset, StartOut, SiReady, Rst_CntN, Up_DnN, Wr, SDin, Wr_RAM;

inout [2:0] RAM_Addr;
inout      ATG_TESTMODE;
inout      BIST_TESTMODE;
inout      SDout, OneZero, NoZeros;
inout               TwoOnes, OneOne, NoOnes, TwoZeros, Wr_Rreg;

// Tie off cells
TLOW tielow1 (.Q(tielow));
THIGH tiehigh1 (.Q(tiehigh));

// Inverted CLK
wire  CLK_N;
INVFF clkinv (.Q(CLK_N), .A(CLK));

//PADS

PADNMIOSCM0H08N05B50 PAD001_StartOut (.PUEN(tiehigh),
      .PDE(tielow),
      .IEN(tielow), .I(StartOut_I), .SIGNAME(StartOut),
      .INMODE(in_mode_avail), .TESTI(jumper001),
      .TESTIEN(tiehigh), .SCANIN(jumper001),
      .OUTMODE(out_mode_avail), .TESTO(tiehigh), .TESTOEN(tiehigh),
      .O(tielow), .OEN(tiehigh));
```

Figure 3. Circuit netlist.

This is an example of the netlist navigation view of a circuit. This view is compact and can be examined quickly, but the information is more difficult for the designer to interpret. To locate circuits and

nodes of interest, one must search the text file.

Netlist navigation can be performed using something as simple as a text editor with search capabilities, since the file is text-based. A more common method is to use the browser function in the simulator or design software. Most browsers contain features that allow the user to trace forward and backward through the netlist, and expand or collapse the hierarchy of the chip. It can be quite slow to diagnose faults using this approach.

We will continue with Part 2 of this article in our January 2018 Newsletter.

Technical Tidbit

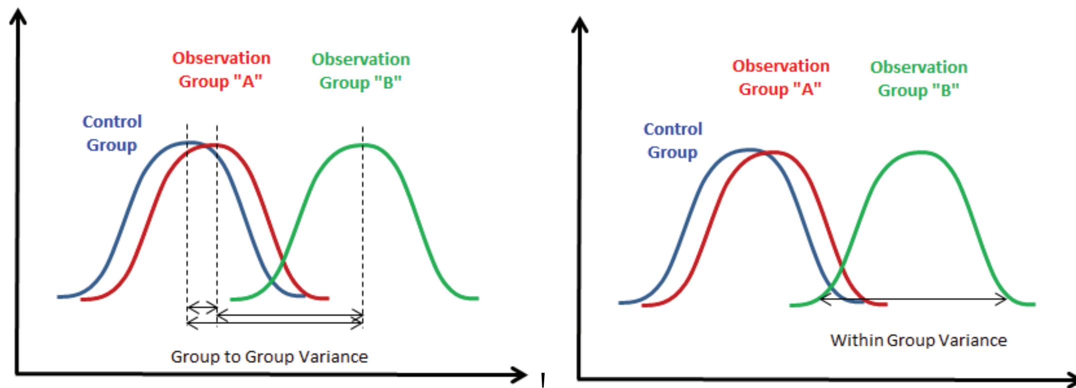
ANOVA Part I

Our technical tidbit this month is Analysis of Variance, or ANOVA. ANOVA provides a statistical test of whether or not the means of several groups are all equal, and therefore generalizes the T-Test to more than two groups. ANOVA is a very useful statistics technique in semiconductor and electronics manufacturing, especially when the engineer wants to compare wafers to each other, wafer lots to each other, or assembly lots to each other. This can be especially useful during process development or assembly development, as well as during yield analysis to look for potential differences that indicate a particular problem.

ANOVA works best when the following conditions apply:

- Are you planning to compare the means of 3 or more populations?
- Are the populations normally distributed?
- Are the samples independent of one another?
- Does each population have the same variance?

ANOVA then identifies if one or more of the groups are different from the rest. You may think that the above conditions are pretty restrictive, but in reality they are quite common. ANOVA is a very important statistical test, and it is used a great deal. ANOVA is used a lot with DataPower and other in-house tools in semiconductor manufacturing, so if you work in a fab, this is a good technique to learn. The key variable is the F statistic. It is the amount of overlap between the control group and the observed group. A large F value indicates a small overlap, since F is the measure of between-groups variance divided by the measure of within-groups variance.



$$F = \frac{\textit{Measure between groups variance}}{\textit{Measure within group variance}}$$

As an example, let's look at an ANOVA single factor analysis. In this analysis we have 14 groups of product we wish to examine. We use an alpha value of 0.05, which corresponds to a 95% confidence level in our F-distribution. This analysis yields the results shown here in this table. Notice that our F statistic,

or F-ratio, is approximately 168. This value is greater than F-crit, which for 13 degrees of freedom (the sum of the between groups degrees of freedom) and an alpha value of 0.05, is approximately 1.72. This implies that the null hypothesis is false, or in this case, the yields are statistically different, which would further imply that our groups are fundamentally different product. Furthermore, since the P-value is 0, that further confirms that our groups are different from one another.

Anova: Single Factor						
SUMMARY						
Groups	*Count*	*Sum*	*Average*	*Variance*		
Column 1	164	175.36	1.06926829	1.86975038		
Column 2	264	277.59	1.05147727	1.90197614		
Column 3	286	308.04	1.07706294	1.70988047		
Column 4	20	8.8	0.44	0.56967368		
Column 5	145	177.88	1.22675862	2.45825956		
Column 6	239	373.35	1.56213389	1.72412946		
Column 7	319	450.16	1.41115987	5.2682084		
Column 8	254	1815.56	7.14787402	6.56075594		
Column 9	143	263.18	1.84041958	11.3861012		
Column 10	109	190.49	1.74761468	8.92170166		
Column 11	154	161.11	1.04616883	1.34883425		
Column 12	160	207.63	1.2976875	1.61860405		
Column 13	39	51.72	1.32615385	0.56167166		
Column 14	93	108.11	1.16247312	1.59311012		
ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	7940.42511	13	610.801931	168.394261	0	1.72427333
Within Groups	8614.63197	2375	3.62721346			
Total	16555.0571	2388				

An extension of the ANOVA method is to use the process to examine an experimental design with blocking. Blocks might represent different batches of wafers, or a product run through different factories, or material run over different periods of time in the same factory. In a blocked design the idea is to quantify the effect of the different treatments, or methods, and the blocking scheme. In a randomized block design, the setup will eliminate variations between the batches. One can then test if the methods are effective by checking to see if the means are equal. One can also look at the residuals, or what remains after the grand average, methods and block effects are taken into account. Put another way, one can use residuals to identify relationships between the means and the variances.

	Method and Resulting Yield (%)				
	A	B	C	D	Block Average
Batch 1	92.3	94.3	98.2	96.4	95.3
Batch 2	94.1	87.4	96.5	87.8	91.5
Batch 3	89.7	93.2	94.9	90.2	92.0
Batch 4	91.2	96.5	93.3	90.4	92.9
Batch 5	86.7	91.9	94.5	92.2	91.3
Treatment Average	90.8	92.7	95.5	91.4	92.6

Probably the best way to understand this is to show an example. Let's assume that we have 5 batches of a new chip design that we plan to run through 4 factories, to comply with multi-sourcing requirements for our customer. We'll refer to these factories as Factory A, Factory B, Factory C, and Factory D. We then look at the yield associated with those factories and group them in the table like we show here. We then generate averages associated with the Blocks (or batches in this case) and the Treatments or Methods (the factories in this case). Those averages are also shown here in the above table.

Anova: Single Factor		alpha =0.05				
SUMMARY						
Groups	*Count*	*Sum*	*Average*	*Variance*		
A	5	454	90.8	7.83		
B	5	463.3	92.66	11.493		
C	5	477.4	95.48	3.622		
D	5	457	91.4	10.26		
ANOVA						
Source of Variation	*SS*	*df*	*MS*	*F*	*P-value*	*F crit*
Between Groups	64.8855	3	21.6285	2.60545099	0.08764007	3.23887152
Within Groups	132.82	16	8.30125			
Total	197.7055	19				

We then perform an ANOVA single factor analysis. We use an alpha value of 0.05, which corresponds to a 95% confidence level in our F-distribution. This analysis yields the results shown here on this chart. Notice that our F statistic, or F-ratio, is 2.605. This value is less than F-crit, which for 19 degrees of freedom (the sum of the between groups and the within groups degrees of freedom) and an alpha value of 0.05, is 3.24. This implies that the null hypothesis is true, or in this case, the yields are not statistically different, which would further imply that our four factories are manufacturing essentially identical product. Furthermore, since the P-value is greater than 0.05, that further confirms that our four factories are manufacturing essentially identical product. In next month's Technical Tidbit, we'll discuss two-factor ANOVA.

Ask the Experts

Q: Why is doping in the polysilicon different between the p- and n-channel transistors in many technologies?

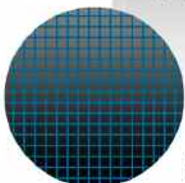
A: The main reason is that by doping the polysilicon opposite to the doping in the channel, the process engineers can produce threshold voltages that are more consistent between the p- and n-channel transistors. If the doping were the same, one transistor would have a much higher threshold voltage than the other.

Learn from the Experts...

...wherever you are.

-Learn at your own pace.
-Eliminate travel expenses.
-Personalize your experience.
-Search a wealth of information.

Visit us at www.semitracks.com for more information.



SEMITRACKS, INC.
Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

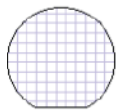
1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



SEMITRACKS INC.
Semiconductor, Microelectronics, Microsystems and Nanotechnology Training

5608 Brockton Court NE
Albuquerque, NM 87111
Tel. (505) 858-0454
Fax (866) 205-0713
e-mail: info@semitracks.com

IRPS

International Reliability Physics Symposium

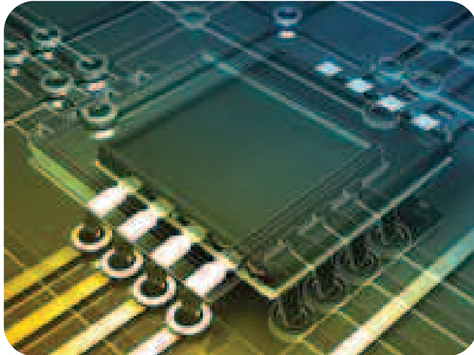
2018 IEEE International Reliability Physics Symposium

March 11-15, 2018
Hyatt Regency San Francisco Airport
1333 Bayshore Highway
Burlingame, CA, USA 94010

Registration is available at www.irps.org

Chris Henderson, Semitracks President

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com anytime before the symposium!



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

~

For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
March 19 – 22, 2018 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany

CMOS, BiCMOS and Bipolar Process Integration
September 10 - 12, 2018 (Mon – Tue)
San Jose, California, USA