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CVD Part II

By Christopher Henderson

Tungsten can be deposited using a CVD reaction; however, it requires several gas species. The most common CVD reaction for tungsten is tungsten hexaflouride plus hydrogen and silane. The hydrogen bonds with the flourine atoms, converting into hydrofluoric acid, which can then be pumped away in gaseous form. Silane, although not part of the main reaction, plays an important role in the overall deposition process. Tungsten hexafluoride requires electrons to dissociate. If there is a layer of tungsten, then the tungsten hexafluoride will obtain electrons from the tungsten causing it to dissociate. On bare silicon, the tungsten hexafluoride will attack and etch the silicon to obtain electrons. However, on an oxide layer, the process will not proceed because there are no available electrons for the tungsten hexafluoride. This phenomenon gives rise to selective tungsten deposition. The addition of silane provides the catalyst to start tungsten deposition on everything. This shuts off the attack on the silicon substrate, creating a blanket deposition. The CVD tungsten process is commonly used for vias. It yields very good step coverage. One can deposit tungsten in vias with diameters down to 0.1µm or better.

The process applications for tungsten include creating interconnect plugs, or filling vias and contact holes, and creating local interconnect layers. Process engineers like tungsten for its ability to completely fills vias and contact holes, its thermal stability, its excellent conformal step coverage, the fact that its CTE closely

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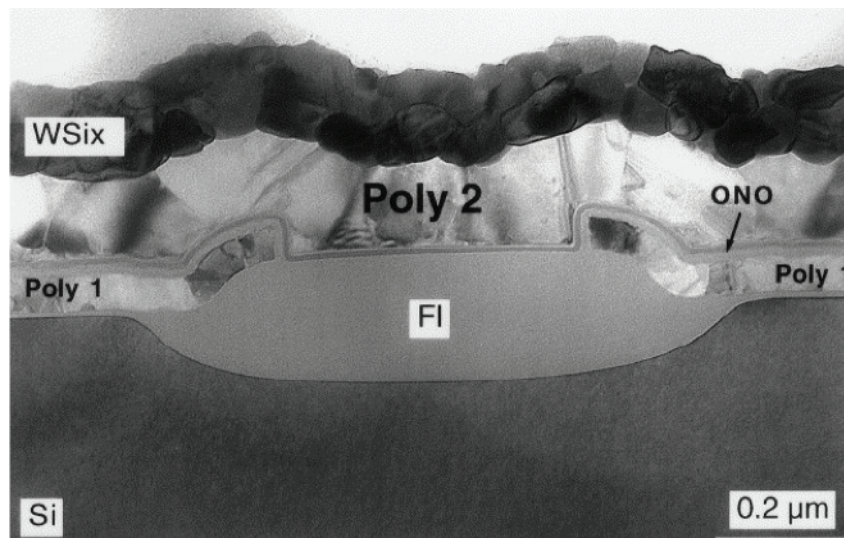
matches silicon, its excellent EM resistance, and its excellent corrosion resistance. However, tungsten does have undesirable qualities like higher resistivity than that of aluminum alloy films, poor adhesion to oxides and nitrides—which precludes deposition in hot-wall reactor or quartz furnace tubes, the fact that it oxidizes above 400°C , and its cost.

Let's look briefly at the deposition conditions. Process engineers deposit tungsten in single-wafer cold-wall LPCVD reactors. The process gas is generally tungsten hexafluoride, but can be tungsten hexachloride. They use temperatures ranging from 300 to 450°C, depending on the process. The gas lines in the CVD system must be heated to prevent condensation. There are three possible deposition reactions: silicon reduction, silane reduction and hydrogen reduction. We show the basic chemistries and temperatures here. A few comments are in order about the reactions. The silicon deduction reaction is self-limiting at thickness around 10 to 15 nanometers. Engineers use the silane reduction reaction to produce nucleation layers for hydrogen reduction. They then use the hydrogen reduction reaction to deposit the bulk of film after silicon or silane reduction reactions.

One can also use selective deposition to create tungsten for local interconnect layers and plugs. This is a selective process where process engineers deposit only on exposed silicon. There are two methods for doing this: selective and blanket tungsten deposition. Selective deposition is a two-step process with silicon and hydrogen reduction, or silane and hydrogen reduction, followed by tungsten deposition. This is not commonly performed. The more common approach is blanket deposition, which is also a two-step process. In addition to tungsten silicide, this is more commonly used for plug formation. These deposition processes require a very clean oxide-free surface.

Let's move on and discuss refractory metal silicide and nitrides. Process engineers use these materials in a supporting role in sub-micron metalization schemes, to act as barrier layers and adhesion layers. In fact, these materials can serve as both barrier and adhesion materials at the same time. They can be deposited by CVD or PVD. Some examples of common applications include aluminum-silicon contacts to create diffusion barriers and to prevent junction spiking; tungsten plugs, to create diffusion barriers and to protect the silicon from damage from the tungsten hexafluoride gases during tungsten deposition and to form adhesion layers between the tungsten and underlying films; and copper interconnect diffusion barriers, to prevent copper diffusion into the silicon dioxide and form adhesion layers between the copper and underlying film.



Process engineers use chemical vapor deposition to deposit refractory metals such as titanium, cobalt, platinum, and tungsten. These silicide layers can form barriers to prevent silicon precipitates and aluminum-silicon junction alloying or reduce the resistance of silicon, and polysilicon connections, like we show on the right. CVD is the preferred method for silicides, such as titanium, cobalt, molybdenum (pronounced mal-lib-denum), nickel and tungsten. CVD is also extensively used for metal sandwich layers such as titanium and titanium nitride, and barrier metals, including titanium tungsten and tungsten.

The main precursor for CVD titanium is titanium tetrachloride plus hydrogen, under the right plasma conditions. However, there is a potential for chlorine contamination in films. Titanium nitride is used as diffusion barrier in aluminum metallization schemes. There are several precursors used for CVD titanium nitride. One precursor system is titanium tetrachloride plus ammonia at 450 to 600ºC. The reaction produces a film with decent step coverage. There is the possibility that chlorine atoms can become incorporated into the titanium nitride layer. Tetrakisdimethylamido titanium is another precursor that is commonly used for CVD titanium nitride. Abbreviated TDMAT it is a titanium with four nitrogen groups bonded to it. Each nitrogen group also contains two methyl groups. A related molecule with a similar ethyl molecule, TDEAT is also used commonly. Both TDMAT and TDEAT can decompose thermally. CVD reactions with both precursors cause substantial amounts of carbon in the titanium nitride film. TDMAT and TDEAT both yield very good step coverage. The reactions are performed at temperatures between 250 and 400ºC. TDMAT and TDEAT can be used in conjunction with ammonia to reduce carbon incorporation. However, the step coverage becomes worse.

Chemical vapor deposition of tantalum is relatively new. Tantalum nitride serves as a liner to stop copper diffusion. Tantalum has a similar chemistry to titanium, but it is five-fold coordinated rather than four-fold. The precursor work is still in development at this time. There has been some work using methyl and ethyl amido complexes. These are some of the more promising chemicals for this effort. Others are experimenting with depositing tantalum oxide, and exposing the metal oxide film to a thermally or plasma enhanced nitrating gas, preferably comprising nitrogen, oxygen, and ammonia. Since the uses for tantalum nitride involve very thin layers, this processing is covered more with Atomic Layer Deposition.

Let's now discuss chemical deposition of other metals. Aluminum and copper are the two most common metals used for interconnects. Researchers have experimented with aluminum CVD processes, but in general have not been able to develop reliable processes. Several possible precursors such as DMAH (dimethyl aluminum hydride), and DMAA (dimethyl amine alane) have been investigated. This class of compounds is generally liquid at room temperatures, and extremely pyrophoric. It is possible to do selective deposition for "better" via fill. Because of problems associated with these materials CVD aluminum is not likely to be used anytime soon, if ever. Researchers have also worked with CVD copper processes. They have investigated various metalorganic precursors, such as CupraSelect, developed by Schumacher. It is commonly written as (HFAC)Cu(TMVS), where HFAC is hexafluoroacetylacetonate, and TMVS is trimethylvinylsilane. These molecules have long, complex structures. While several CVD processes give good step coverage and deposition rates, they are overshadowed by electroless plating. Electroless plating provides better deposition characteristics, and is used widely in the industry today.

Chemical vapor deposition of low-k dielectrics is even less developed. Most researchers are developing spin-on materials that are deposited in liquid form. There are two potential areas where

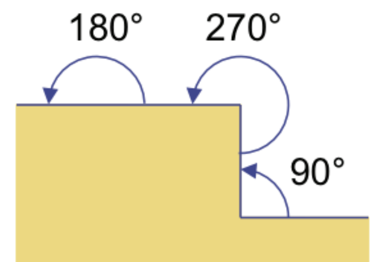
chemical vapor deposition of low-k dielectrics may take off. One involves the deposition of paralyne. Paralyne is an organic polymer. It can be evaporated and transported over the wafer where it will condense back into a polymer film. It is very straightforward to perform. Researchers at Texas Instruments have worked on this process. Researchers have also worked on CVD of carbon films. Carbon films can be deposited from methane or fluorocarbons. Both Sharp Semiconductor and Applied Materials have worked on these films.

Let's move on and discuss step coverage. This is an important issue for both physical and chemically vapor deposited films. We defined step coverage using this equation.

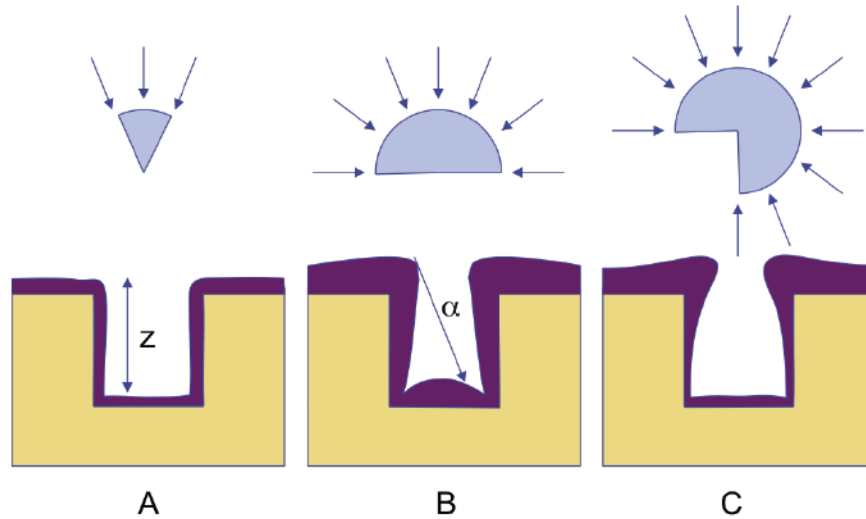
$$Step\ coverage\ (\%) = (t_s / t_n) \times 100\%$$

For conformal coverage, there is equal film thickness over all the topography—or in other words—the vertical and horizontal surfaces have equal film thickness. *If we examine conformal coverage in a mass-transport limited system, we find that film thickness at a given point is a function of the reactant flux, which is in turn a function of pressure and adatom migration. If the adsorbed reactants can migrate easily across the surface, they will be found with equal probability on any part of the substrate, which results in conformal step coverage. The adatom mobility is a function of the adatom species and energy, so higher substrate temperatures and ion bombardment will enhance adatom surface migration. *In general, the step coverage is a function of many factors, including film species, reactor design and deposition conditions.

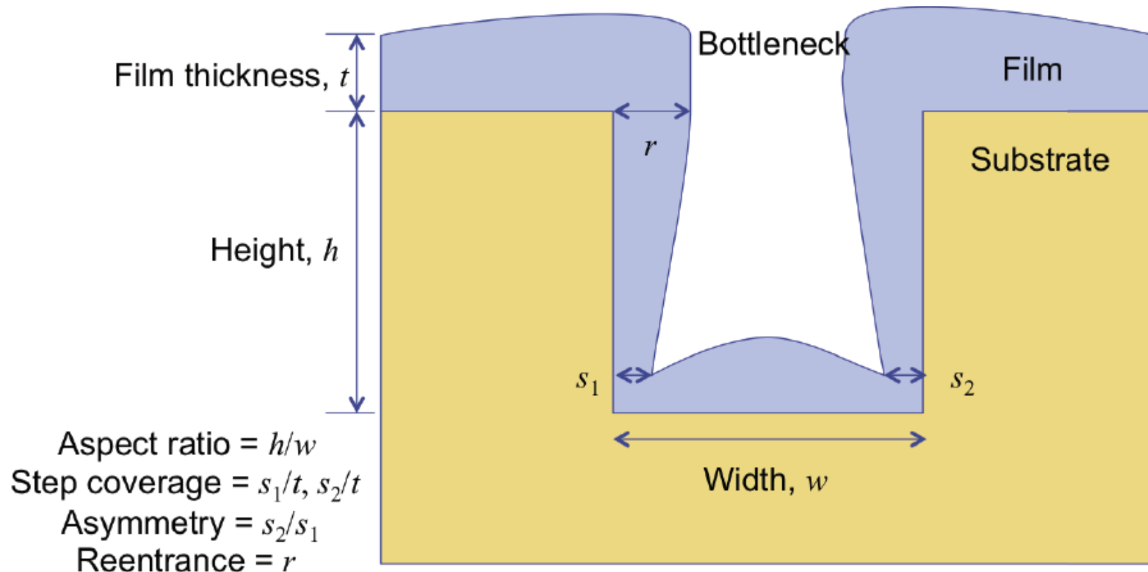
The coverage is affected by the arrival angle of particles. The arrival angle theta is the angle of incidence of the arriving species. We will discuss three examples to illustrate this point. If we look at CVD deposition of silicon dioxide from silane, we know that the sticking coefficient of silane is high and the surface migration is low. We also know that with atmospheric pressure CVD, the mean-free path is quite low. These frequent collisions will create random arrival angles, so the flux is directly proportional to the range of arrival angles. Those angles will depend on the topography of the chip, so top corners will produce overhang, and bottom corners will produce bottom corners. The figure at the bottom right shows the concept of arrival angle and its effect on step coverage.



In the second example, let's look at the deposition of silicon dioxide from silane using low pressure CVD. With this technique the mean-free path is long, so the atoms follow straight-line trajectories, which can lead to shadowing. This can produce re-entrant profiles near the bottom of steps. In the third example let's look at plasma enhanced CVD of silicon dioxide from TEOS. Here, the mean-free path is long, but the adatom migration rate is also high. This creates a more conformal layer, which can be useful in certain circumstances. So the main factors that affect step coverage are the reactant arrival angles, which are a function of chamber pressure, and the adatom migration rate, which is a function of substrate temperature and ion bombardment.



This slide shows schematic diagrams with different types of step coverage. Figure A shows conformal coverage resulting from rapid surface migration. Figure B shows non-conformal coverage for a long mean-free path and no surface migration. Figure C shows non-conformal coverage for a short mean-free path and no surface migration. Notice the overhang that forms at the top corners.

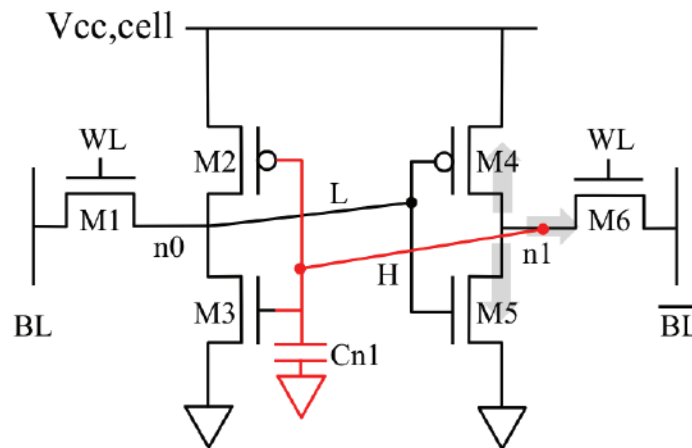


Sometimes, engineers will measure these step coverage features to monitor a process. This diagram shows the deposition of a film into a hole having a high aspect ratio. A bottleneck may develop due to the buildup of an overhang on the top corners. We define the film thickness, width and height of the hole. We also define the aspect ratio, step coverage, asymmetry, and reentrance of the film using the variables on the left.

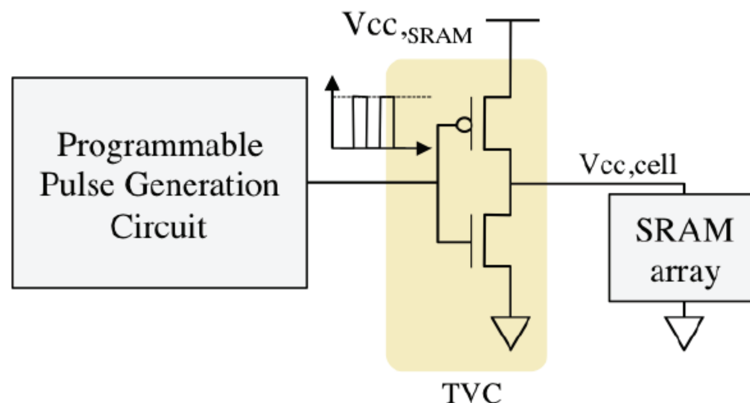
Technical Tidbit

Transient Voltage Collapse

Supply-voltage scaling or reduction has been a key approach to achieve low-power consumption in advanced SOCs and microprocessors. We typically denote the supply voltage as either V_{DD} or V_{CC}. However, voltage-scaling in the SRAM block is challenging because the read, write, and hold stability of the SRAM are influenced by increased voltage variations at lowered V_{DD}. Several years ago, design engineers introduced the transient voltage collapse (TVC) technique for modern SRAM architectures to achieve low-voltage operation and higher density SRAM cells.



Reducing the SRAM cell supply voltage (V_{CC},cell) during write operations has been proposed to reduce competition between transistors M4 and M6 (or M2 and M1) in 6-transistor SRAM structures (see Figure 1—upper left). In order to achieve consistent writing conditions, M2 and M4 should be weaker than M1 and M6, respectively. Lowering V_{CC},cell voltage below the threshold voltage of M2 and M4 makes drive of these transistors very weak. Consequently, the write-stability becomes less sensitive to the process variation and/or V_{CC} variation at low V_{CC} voltages. Therefore, when one connects the TVC circuit directly to V_{CC},cell, it briefly collapses the V_{CC},cell voltage to near 0 V during the write operation. This idea is widely adapted in modern Systems on a Chip (SOCs), graphics processor units (GPUs), and microprocessors, which are currently available on the market. Figure 2 (lower right) shows a circuit diagram of the TVC circuit which generates a transient V_{CC},cell droop with varying durations through a programmable pulse generator.



Ask the Experts

Q: I have performed an autoclave test with the parameters: 120°C, at 85% relative humidity for 168 hours. I want to know the acceleration factor related to normal conditions like 25°C and 55% relative humidity. Which formula do I use to calculate the acceleration factor I have simulated with this test?

A: The main equation to use for your work, given that you are accelerating both temperature and pressure, would be the Peck Model.

$$AF = \left(\frac{RH_{Stress}}{RH_{Use}}\right)^{a} e^{E_A/k\left(1/T_{Use} - 1/T_{Stress}\right)}$$

$$AF = \left(\frac{V_{Stress}}{V_{Use}}\right)^{b}\left(\frac{RH_{Stress}}{RH_{Use}}\right)^{a} e^{E_A/k\left(1/T_{Use} - 1/T_{Stress}\right)}$$

However, we need to know several other parameters in order for you to make a calculation. First, we need to know what failure mechanism or mechanisms you are interested in modeling. Is it bond pad corrosion? Is it leakage between pins on the outside of the package? Internal leakage? Once we know the mechanism, then we can figure out what we need to use for an activation energy (EA) and a humidity exponent (a). Second, are you also accelerating something where voltage is involved?

IRPS

International Reliability Physics Symposium

2016 IEEE International Reliability Physics Symposium

April 17-21, 2016
Pasadena Convention Center
Pasadena, CA, USA

Registration is available at www.irps.org

Chris Henderson, IRPS General Chair

Chris would be happy to meet with you and discuss any training needs you have. Contact him at henderson@semitracks.com during the symposium!

Spotlight: Process Integration Short Course

Our CMOS, BiCMOS and Bipolar Process Integration Course is scheduled for March 21 and 22 in Albuquerque, New Mexico. We don't offer this course publicly very often, so now is your opportunity to attend it. For further information, please visit the website (Click here)

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS and BiCMOS Process Integration*** is a five-day course that offers detailed instruction on the physics behind the operation of a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and interconnect performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into four segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why CMOS (Complimentary Metal Oxide Semiconductor) devices dominate the industry today
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.

3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.
5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, strained silicon, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

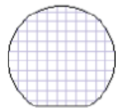
COURSE OUTLINE

1. Introduction
2. Conventional CMOS
   a. Key Components and Parameters
   b. Process Overview and Integration Issues
   c. Scaling and Limitations
3. Mobility Enhancement Techniques
   a. Strained Silicon
   b. Crystal Orientation
4. Gate Stacks, High-k Dielectrics
   a. Gate Conductor Materials and Properties
   b. High-k Materials and Properties
   c. Gate Stack Integration
5. Options for Source-Drain, Extensions
   a. Elevated Source/Drain
   b. Co-Implantation of Inactive Species
   c. Schottky-Barrier Source-Drain
6. Three-Dimensional Structures
   a. FinFETs, Multi-Gates
7. Interconnects
   a. Aluminum Interconnects, Issues
   b. Copper Interconnects, Issues
   c. Low-k Dielectrics

8. Conventional BiCMOS
    a. Bipolar Transistor Fundamentals
    b. BiCMOS Process Overview
    c. Scaling and Limitations
9. Bipolar Enhancement Techniques
    a. SiGe
    b. SiGe:C
10. CMOS/BiCMOS Reliability Considerations
    a. Electrostatic Discharge
    b. Electromigration and Stress Migration
    c. Soft Errors, Plasma Damage
    d. Dielectric Reliability
    e. Bias Temperature Instabilities
    f. Hot Carrier Reliability
    g. Burn-In
11. Yield Considerations
    a. Yield Detractors
    b. Models
    c. Monitors

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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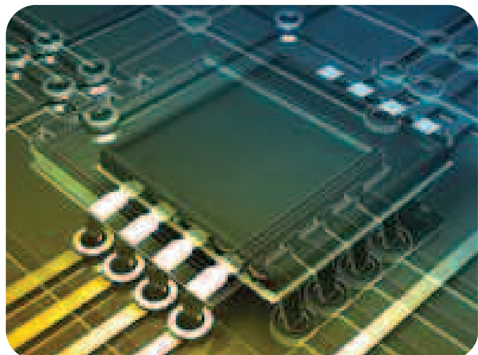

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Semiconductor Reliability
January 6 – 8, 2016 (Wed – Fri)
San Jose, California, USA

Failure and Yield Analysis
January 18 – 21, 2016 (Mon – Thur)
San Jose, California, USA

CMOS, BICMOS and Bipolar Process Integration
March 21 – 22, 2016 (Mon – Tue)
Albuquerque, New Mexico, USA

Wafer Fab Processing
March 29 – April 1, 2016 (Tue – Fri)
San Jose, California, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany