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Thermal Processing—Part V, Equipment and Processing

By Christopher Henderson

Let's move on and discuss rapid thermal processing, or RTP, hardware. Engineers normally perform RTP one wafer at a time, so RTP hardware is designed to process one wafer at a time. The system rotates the wafer while in the system to minimize the effects of heating non-uniformities and gas flow non-uniformities. RTP hardware operates either at atmospheric pressure or reduced pressure, and is compatible with both dry and chlorine oxidations. Wet oxidations can be performed using in situ steam generation, where one introduces hydrogen and oxygen gas onto a hot wafer surface where they react and form steam. Obviously, this is a safety issue, and must be performed carefully with the appropriate mitigation protocols.

Rapid Thermal Processing employs either cold wall or hall wall technology. Cold wall technology is the traditional method. Here, an array of tungsten or halogen lamps heats the wafer through radiation. This process brings the wafer up to the required temperature within a few seconds. However, the wafer is not in thermal equilibrium with the chamber itself or the lamp, so this can lead to non-uniformities in the anneal process. Hot wall technology is the newer method. Here, heating elements like silicon carbide radiate blackbody heat to the wafer through convection and conduction. This method leads to a more uniform temperature profile, which means a more uniform anneal process across the wafer.

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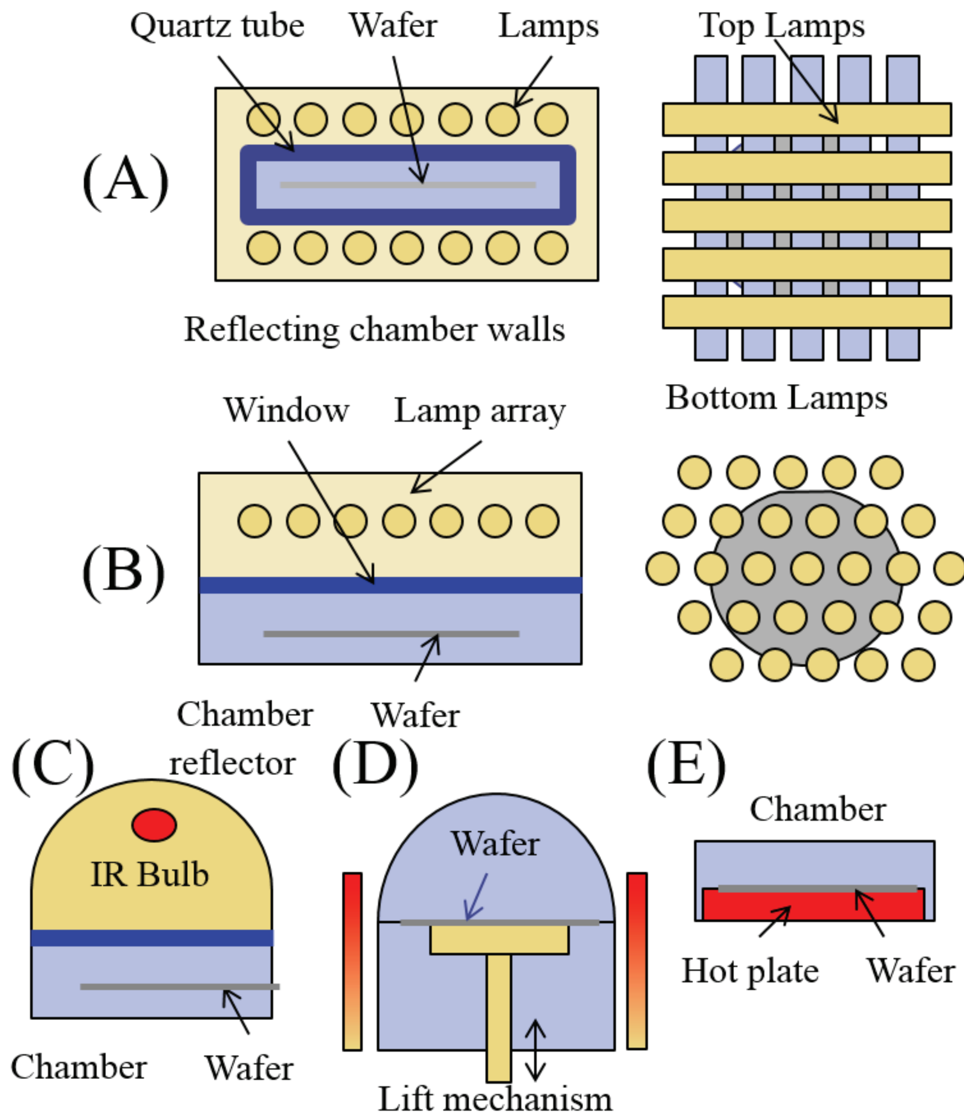
The manufacturers of rapid thermal processing equipment have created various designs and configurations for use in the semiconductor industry. These drawings show the more common configurations. They range from quartz tube and lamps, like we show in figures A and B, to chambers with IR bulbs, rods, and hot plates, like we show in figures C, D, and E respectively. Rapid thermal annealing is fast becoming the first choice for thermal processing steps. Engineers use rapid thermal annealing for post-implant damage annealing and dopant activation, where the heat drives the dopant atoms to the lattice sites to become electrically active. They form metal silicides for contacts with the technique. Materials like titanium, cobalt, and nickel silicide lend themselves well to rapid thermal processing. Process engineers also perform rapid thermal oxidation to create thin oxide and oxynitride layers for transistor gates, capacitors, pad oxides, side wall spacers, and shallow trench isolation liners.



Rapid thermal processing has many advantages over atmospheric oxidation furnaces. First, RTP can heat and cool the wafer very quickly. For example, one can achieve a 250 degree centigrade per second temperature ramp-up and a 90 degree per second ramp-down, which minimizes dopant redistribution and transient-enhanced diffusion effects. It also provides engineers with lower and better control of the thermal budget and better process control. Second, because of the potential short cycles, RTP allows one to grow oxides at higher temperatures. This leads to higher quality films with less trapped charge and less leakage. It also leads to higher carrier mobility due to a smoother interface at the silicon-dielectric interface. Third, rapid thermal processing, being a single wafer tool, lends itself well to clustering with other tools. For example, one can integrate pre-clean, rapid thermal oxidation gate formation and gate polysilicon deposition into the same cluster tool. Fourth, RTP provides excellent process flexibility. Engineers can run at atmospheric or reduced pressure, and they can utilize a wide range of process gases for steps like low-k dielectric deposition. Fifth, since RTP can be performed on a wafer-by-wafer basis within a cluster tool, RTP can therefore be an ultra-clean process. The main challenge is temperature measurement and control, including the ramp-up, soak, and ramp-down steps.

Applied Materials Vantage RTP system

These images show examples of rapid thermal processing hardware. The image on the left shows a rapid thermal processing system from the exterior. The image on the right shows the RTP chamber, with a wafer in the system.

One of the challenges with Rapid Thermal Processing is temperature measurement. Normally, one measures high temperatures of objects using optical techniques. Basic radiation physics includes a concept called a blackbody. A blackbody is a theoretical object that absorbs all the radiation it receives. It then emits a characteristic temperature-dependent spectrum of radiation. For example, the sun is almost an ideal blackbody. It absorbs almost all of the incoming radiation. Since the surface of the sun is approximately 5500 degrees centigrade, it emits a spectrum of radiation that peaks in the visible range, creating that bright white light we see. That radiation spectrum also includes ultraviolet and infrared light as well. We feel the infrared light as warmth on our skin on a clear summer day. The second concept is emissivity. This is the ratio of energy radiated to the energy by a material to the energy radiated by a blackbody at the same temperature. While the sun is almost a perfect blackbody, having an emissivity near 1, an object like a mirror—a polished silver surface—has an emissivity near zero. In other words, it has a high reflectivity. Power and temperature are related by the Stefan-Boltzmann radiation law, shown here, where W is the total power, sigma is the Stefan-Boltzmann constant, and T is the temperature of the object.

$$W = \sigma T^4$$

The most common optical measurement tool for RTP is the optical pyrometer. It is a non-contact tool that determines the temperature by measuring the wafer's emissivity. It is the main technique used in cold wall RTP hardware.

This is an example of an optical pyrometer. The challenge with optical pyrometry is the difference from wafer-to-wafer, lot-to-lot, and technology-to-technology. Since we're measuring emissivity, the emissivity is a function of the backside films and the reflectivity. This means the coatings and the backside preparation play a big role in the accuracy of the readings. As such, many hot wall reactors use both thermal couples and optical pyrometers.

Let's move on to briefly discuss the ancillary tools for thermal processing. There are two common tools for measuring oxide thickness: the reflectometer and the spectroscopic ellipsometer. The

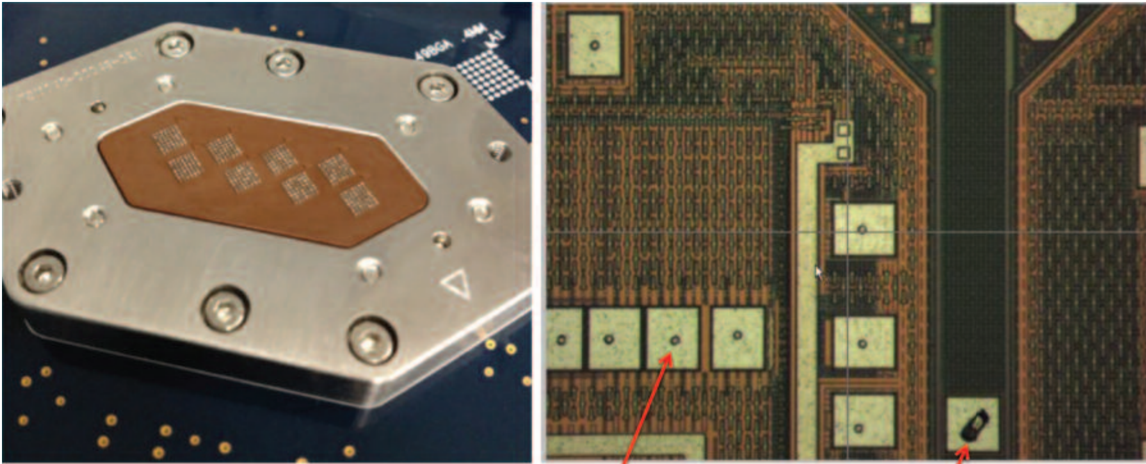
reflectometer uses optical interference. It determines the interference between the light reflected at the air-silicon dioxide interface and the light reflected at the silicon dioxide-silicon interface. This technique only works on oxides thicker than 10 nanometers. The spectroscopic ellipsometer uses a laser to look at changes in polarization that occur when the light reflects off of the silicon or silicon dioxide surface. The polarization change depends on the spectrum, so the spectrum can provide more accurate data. This technique works on dielectrics down to 5 angstroms, and can be applied to a wider range of materials than just silicon dioxide, making it a good choice for low-K and high-K dielectrics. Finally, the transmission electron microscope can be used for offline verification of very thin oxides. Since it requires destructive sample preparation, it must be performed outside of the normal process flow.

The industry uses still other tools to assess oxide film quality. Process engineers make these measurements both inline and off-line. For dielectric strength, process engineers measure time to breakdown, charge to breakdown, and other MOS measurements. For mobile ion charge, engineers use capacitance-voltage plotting. They do this with and without bias and at different temperatures. They measure the shift in the flatband voltage of an MOS transistor under stressed conditions and compare it to an unstressed sample to look for differences. For fixed and trapped charges, again process engineers use the capacitance voltage plot and other MOS transistor measurements. Finally, for particulate contamination, they use wafer inspection systems to look at both patterned and unpatterned wafers.

With all thermal processing, temperature control is the most critical factor. Process engineers must include examination of ramp rates, monitor for temperature overshoot, account for stabilization times, and other variables. As feature sizes become smaller and smaller, this is a more important activity.

Technical Tidbit

Vertical Probe Cards



Vertical Probe Mark Cantilevered Probe Mark

An increasingly common type of probe card is the vertical probe card. The image on the left shows an octal (8) site vertical probe card from Form Factor. The probes pass through two offset plates, which create a bend in the probes. A reduction in the amount of bend in the probes lowers the probes and generates the pressure on the pad required to make positive contact. This approach or technology is sometimes known as buckling beams. We show examples of the probe marks on the pads in the image on the right. The probe mark left by the vertical probe is typically smaller than that left by a cantilevered probe. This type of probing will generate fewer particles, and can facilitate probing an array of pads, since the probes do not take up as much lateral area as cantilevered probe tips.

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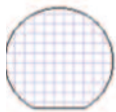

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Ask the Experts

Q: Why do engineers use more than one algorithm to identify outliers?

A: The reason stems mainly from the type of distribution related to the parameter used for outlier identification. For example, if we use diode breakdown voltage as an identification parameter, the distribution of breakdown voltages is typically a normal distribution. That means that algorithms like the 3-Sigma algorithm will work well. On the other hand, if we use a parameter like IDDQ, the distribution for IDDQ is typically right-skewed (a tail of data that extends to higher currents moreso than to lower currents). In this case, an algorithm like Tukey or CPKn will tend to do a better job. Many engineers actually prefer the CPKn algorithm when the tails are significant.

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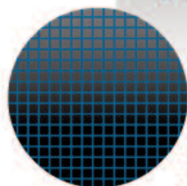

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Spotlight: EOS, ESD, and How to Differentiate

OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. Although EOS and ESD damage can at times look quite similar to each other, the source each and the solution can be quite different. Therefore, it is important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a two-day course that offers detailed instruction on EOS, ESD and how to distinguish between them. This course is designed for every manager, engineer, and technician concerned with EOS, ESD, analyzing field returns, determining impact, and developing mitigation techniques.

Participants learn to develop the skills to determine what constitutes a good ESD design, how to recognize devices that can reduce ESD susceptibility, and how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism.** Participants learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.
2. **Overview of the ESD Failure Mechanism.** Participants learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.
3. **ESD Circuit Design Issues.** Participants learn how designers develop circuits to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.
4. **How to Differentiate.** Participants learn how to tell the difference between EOS and ESD. They learn how to simulate damage and interpret pulse widths, amplitudes and polarity.
5. **Resolving EOS/ESD on the Manufacturing Floor.** Participants see a number of common problems and their origins.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. Participants will understand the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. The seminar will identify the major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. Participants will be able to identify basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.
5. Participants will be able to distinguish between EOS and ESD when performing a failure analysis.
6. Participants will be able to estimate a pulse width, pulse amplitude, and determine the polarity of an EOS or ESD event.
7. Participants will see examples of common problems that result in EOS and ESD in the manufacturing environment.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, written text material, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The course notes offer dozens of pages of additional reference material the participants can use back at their daily activities.

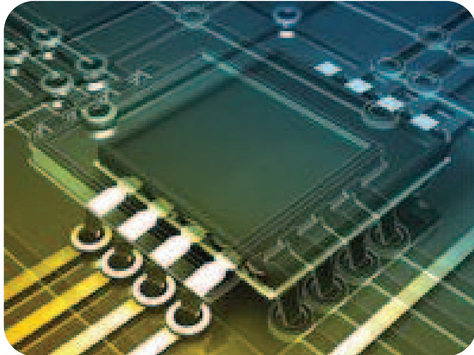
COURSE OUTLINE

Day 1

1. Introduction
   a. Terms and Definitions
   b. ESD Fundamentals
   c. EOS Fundamentals
2. Electrical Overstress Device Physics
   a. Sources of EOS
   b. EOS Models
   c. Electrothermal Physics
3. Electrostatic Discharge Device Physics
   a. ESD Models
   b. ESD Testing and Qualification
   c. ESD Failure Criteria
   d. Electrothermal Physics
   e. Electrostatic Discharge Failure Models
   f. Semiconductor Devices and ESD Models
   g. Latchup
4. EOS Issues in Manufacturing
   a. Charging Associated with Equipment
      i. Testers
      ii. Automated Handling Equipment
      iii. Soldering Irons
   b. Charge Board Events
   c. Cable Discharge Events
   d. Ground Loops/Faulty Wiring
   e. Voltage Differentials due to High Current
   f. Event Detection

Day 2

5. ESD Protection Methods
   a. Semiconductor Process Methods
   b. MOSFET Design
   c. Diode Design
   d. Off-Chip Drivers
   e. Receiver Networks
   f. Power Clamps
6. Differentiating Between EOS and ESD
   a. EOS Manifestation
   b. ESD Manifestation
   c. Circuit considerations
      i. Chip level
      ii. System level
   d. Simulating ESD
   e. Simulating EOS
7. EOS/ESD Design and Modeling Tools
   a. Electrothermal Circuit Design
   b. Electrothermal Device Design
   c. ESD CAD Design



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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San Jose, California, USA

EOS, ESD and How to Differentiate
January 28 – 29, 2015 (Wed – Thur)
San Jose, California, USA