SEMITRACKS, INC.

ISSUE 158
AUGUST
2022

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Analog Building Blocks

By Christopher Henderson

This month concludes our series of Feature Articles with a discussion of operational amplifier circuits. We can now combine the concepts we discussed previous Feature Articles to create even more versatile amplifiers.

Figure 1 illustrates a Basic Operational Amplifier. The light shaded area is the differential amplifier portion of the circuit. The medium shaded area is the common source stage, and finally, the dark shaded area is the output buffer.

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WHAT'S INSIDE?

Want to take control of your learning? See Page 6

UPCOMING WEBINARS:

Wafer Fab Processing

IC Packaging Design and Modeling Course

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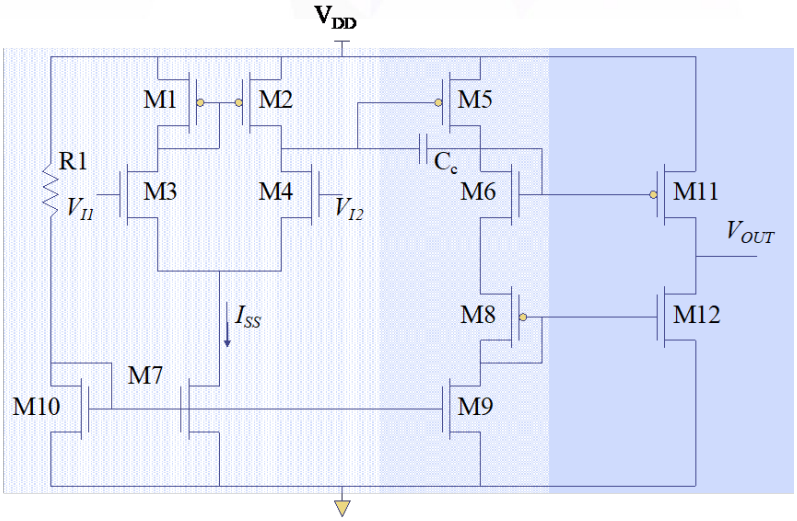

Figure 1- Basic Operational Amplifier

One common method to help protect the operational amplifier from thermal runaway is to insert a short circuit protection scheme, as shown in Figure 2. The addition of M13 and M14, as well as the two resistors in between M11 and M12 at the output, eliminates the possibility of thermal runaway on M11 or M12. The values of R2 and R3 are typically around 1kΩ.

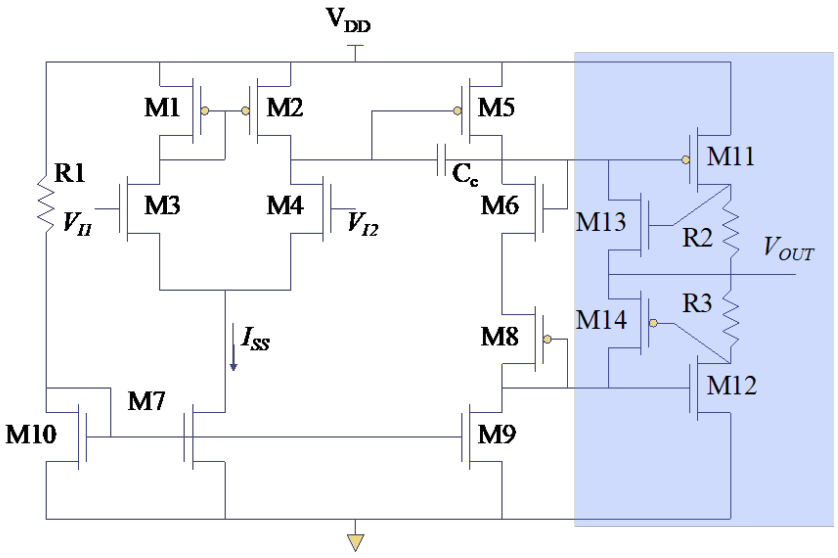

Figure 2- Short circuit output protection

An important topic that we will briefly cover is the concept of feedback in amplifiers. All analog designers should be aware of feedback, how it occurs, and how to mitigate its effects. Amplifiers not only amplify signals, but they also shift the phase of those signals. It is this phase shift that can lead to problems. If the phase shift exceeds 180°, then the shifted signal can be amplified if there is a feedback loop. A feedback loop is constructed, or can occur when the output signal is, in some manner, connected back to the input. Furthermore, if the phase shift exceeds 180° when the gain of the amplifier exceeds one, then the circuit can be prone to oscillations. In order to avoid such problems, analog designers must analyze their circuits for this possibility. The circuit analysis techniques involve the use of Bode plots (discussed below), as well as Nyquist diagrams (discussed later). If the amplifier is susceptible to oscillations, then the circuit should be modified to avoid the problem. This is normally referred to as compensation.

Figure 3 shows a Bode plot for the Basic Operational Amplifier that was shown in Figure 1. Note that the gain of the amplifier begins to roll off above about 300 kHz. By the time the frequency has reached 30 MHz, the gain is down to 0 dB, or unity. Notice that we introduce a phase shift in the amplification when the frequency increases. By the time we reach 10 MHz, the amplifier phase is -180°. At 10 MHz, the amplifier gain is still positive. A positive gain at a -180° phase shift means that this particular amplifier is unstable at frequencies above 15 MHz. In other words, it will go into oscillation at 15 MHz or higher.

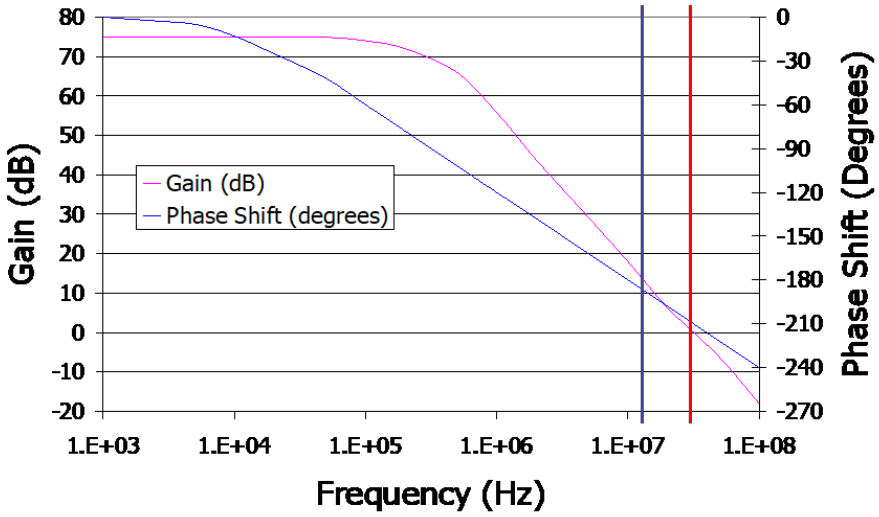

Figure 3- Bode plot for standard operational amplifier

The drawing in Figure 4 is a Nyquist plot for our amplifier. The Nyquist plot allows us to represent the phase shift that occurs in an amplifier as a function of frequency. It allows us to reduce the Bode plot to a single graph. The Nyquist plot is made on a polar coordinate system. The important point illustrated by this Nyquist plot is the instability of the amplifier. If the Nyquist plot encircles the point (-1,0) then the amplifier is unstable. In this graph T_0 would be 75 dB, representing the gain of the amplifier.

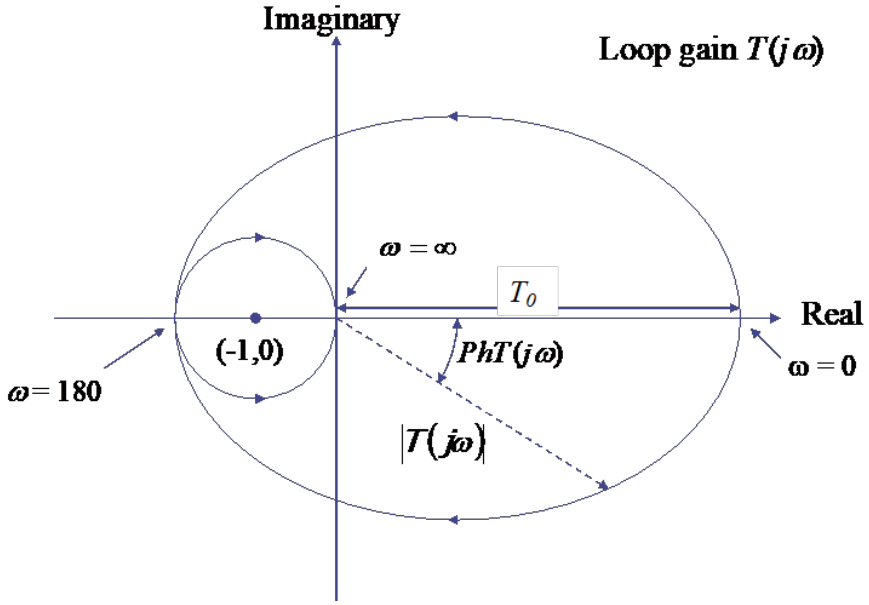

Figure 4- Illustration of Nyquist plot for amplifier

In order to compensate for feedback, R_c and C_c are inserted in the common source circuitry (shaded area), as shown in Figure 5. Typically, a circuit designer will add in circuit elements to reduce the amount of phase shift on an operational amplifier to allow for more of a phase margin. This accounts for propagation delay that might occur due to a large load capacitance. A typical amount of margin is 45°. For some high-performance applications, a designer may allocate less margin.

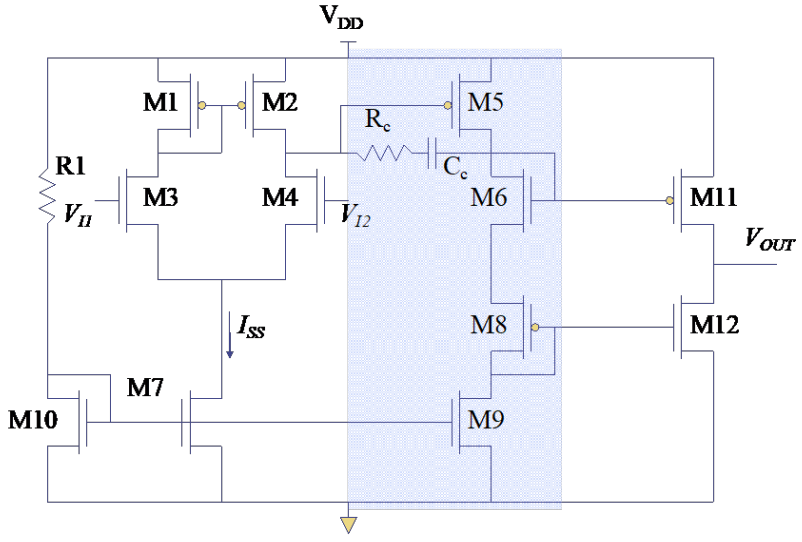

Figure 5- Compensation circuitry

In addition to feedback, there are a number of additional amplifier parameters that the designer must take into account. These include input offset voltage, output voltage swing, common mode rejection ratio, power dissipation, power supply rejection ratio, and slew rate. Input offset voltage is a measure of how well balanced the amplifier is. It is the voltage associated with the output voltage being zero volts. The output voltage swing is a measure of how wide a range over which the amplifier can operate. The common mode rejection ratio is a measure of an amplifier's ability to reject—or not amplify—signals that occur on both inputs. Power dissipation is a measure of the amount of power an amplifier consumes. This is important in both static and dynamic operation. Power supply rejection ratio is a measure of an amplifier's ability to reject—or not amplify—noise on the power supply lines to the amplifier. Finally, slew rate measures the ability of an amplifier to respond to fast changes in input signals. This is usually described in terms of volts per microsecond.

Now, we cover some additional analog circuits that are commonly used by circuit designers.

First, we will mention the Operational Transconductance Amplifier (shown in Figure 6). The Operational Transconductance Amplifier—or OTA as it is sometimes called—is basically an op-amp with the output buffer removed. An OTA can only drive a capacitive load. All of the nodes have low impedance, except for the input and output nodes.

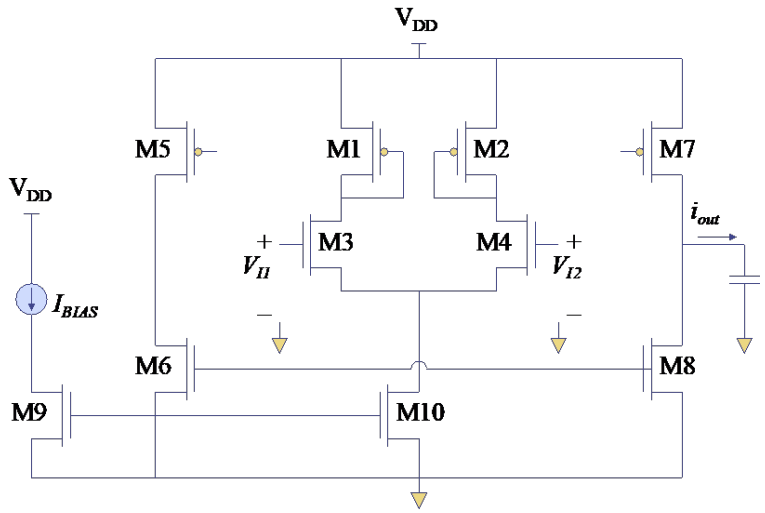

Figure 6- Operational transconductance amplifier

Next, we will mention the Differential Output Operational Amplifiers which are a necessity in many circuit designs. Many mixed signal designs can generate noise. Digital logic in particular can generate a lot of noise. The Differential Output Operational Amplifiers, or differential op amps, can reject noise on the input lines if the input lines run closely together. If the lines are close together, the same amount of noise is generated on each line. A differential op amp can also do a good job of rejecting power supply noise. The circuit shown in Figure 7 is an example of a fully differential folded cascode OTA. The key to the differential op amp is the common mode feedback circuit, or CMFB (discussed in more detail below).

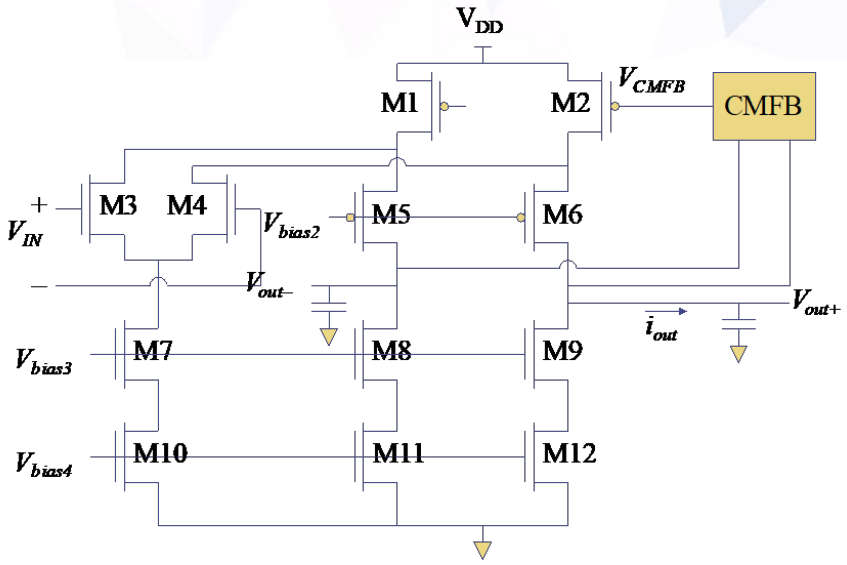

Figure 7- Differential output operational amplifier

The common mode feedback circuit (shown in more detail in Figure 8) senses the voltages on the plus and minus outputs and feeds the reference voltage, which is the average of the plus and minus output voltages, back into the amplifier. For example, let's assume that VDD is 5 volts and VSS is 0 volts. The common mode feedback voltage should be 2.5 volts. The common mode feedback circuit rejects the difference mode signals on its inputs and amplifies the common mode signal. Therefore, it amplifies the difference between the average of the outputs and the common mode voltage.

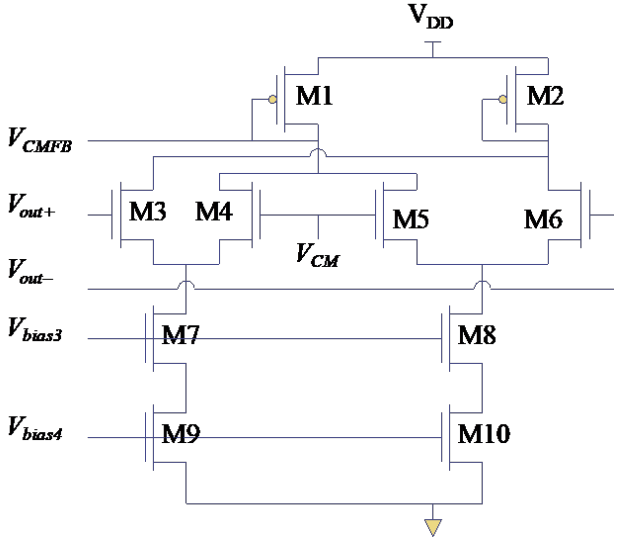

Figure 8- Common mode feedback circuit

This concludes our series of articles on Analog Building Blocks. To learn more about circuit design and other topics, please visit our website at www.semitracks.com. Our Online Training system provides a variety of materials to help you continue your education in Semiconductor Technology.

Technical Tidbit: Pulsed Nucleation Layers

This month's Technical Tidbit covers Pulsed Nucleation Layers. Pulsed Nucleation is used in the formation of contacts for Integrated Circuits.

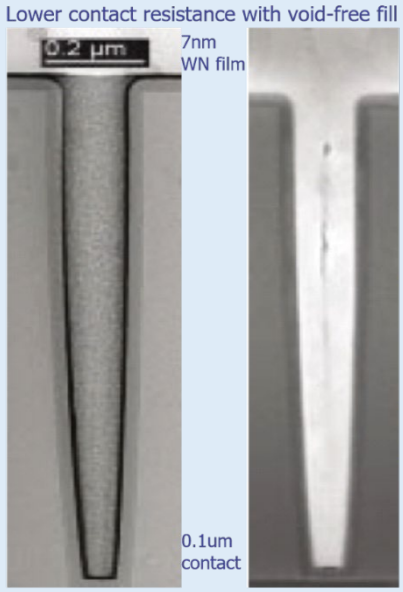

Figure 1- TEM images

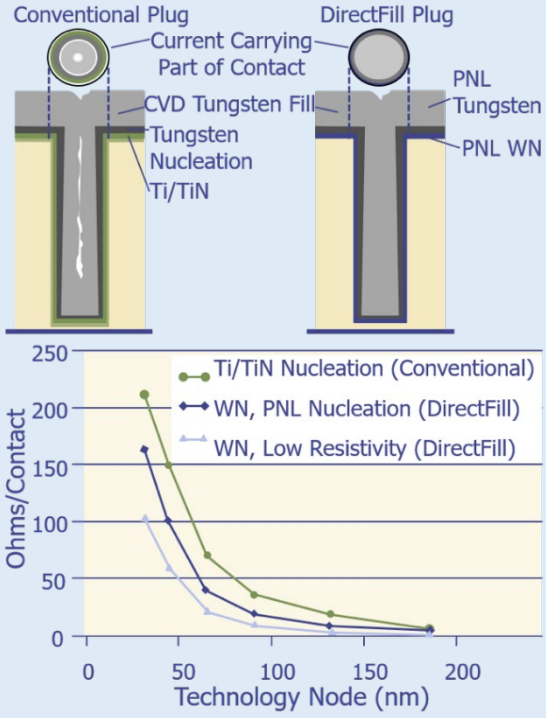

Figure 2- data associated with PNL performance

Tungsten is a commonly used material for making those contacts. Tungsten and tungsten-nitride films can be conformally deposited, even in high-aspect ratio vias and contacts. This leads to better fill characteristics and lower resistances like we show in the Transmission Electron Microscope (TEM) images in Figure 1, and the diagrams in Figure 2. However, there are still concerns about contacts and vias. As we scale feature sizes down, there is more barrier layer, more grain boundary scattering, and more voiding, which leads to higher resistance. The aspect ratio of the vias or contacts also plays an important role in the development of voids. Voids are more likely to form the higher the aspect ratio is. Variations in critical dimensions would impact void formation as well. One method for reducing these problems and lowering the resistance is a technique called Pulsed Nucleation Layer, or PNL, deposition. This creates a lower resistance connection, like we see in the graph at the bottom of Figure 2.

The main use of PNL is the forming of a tungsten nucleation layer using a sequential deposition process. The tungsten nucleation layer is created by reacting pulses of a tungsten-containing precursor, like tungsten hexafluoride, and a reducing gas, like hydrogen, in a process chamber to deposit tungsten on the substrate. Thereafter, the reaction by-products generated from the tungsten deposition are removed from the process chamber. After the reaction by-products are removed from the process chamber, a flow of the reducing gas is provided to the process chamber to react with residual tungsten-containing precursor remaining therein. Such a deposition process forms tungsten nucleation layers having good step coverage. The sequential deposition process of reacting pulses of the tungsten-containing precursor and a reducing gas, removing reaction by-products, and then providing a flow of the reducing gas to the process chamber may be repeated until a desired thickness for the tungsten nucleation layer is formed.

Ask The Experts

Q: I have a question about the history of the IC testing process. Was testing done in the past using hand test only without a test system?

A: Early on, some companies did hand testing with voltmeters and oscilloscopes. By the 1970s however, companies were making their own basic test systems to capture the information. A major reason why companies built their own testers is that none were available to purchase. One company that did this was Texas Instruments (TI). TI built a tester, known as the VLCT (Very Low Cost Tester), to test components. They continue to use this tester, since these testers are fully depreciated (paid for), allowing the company to keep the cost of test lower.

Course Spotlight: IC Packaging Design

We will be hosting this course in an upcoming webinar. For more information, see page 10 for dates and times. We hope to see you there!

COURSE OBJECTIVES

With focused guidance from your instructor, you will gain insight into the following:

1. An in-depth understanding of semiconductor packaging design and its technical issues.

2. Understanding the basic concepts behind thermal and mechanical simulations of packages.

3. Identifying the key issues related to the continued growth of the semiconductor industry. This includes the need for high power dissipation, and designs that can mitigate the increasing fragility of the die because of low-k dielectrics.

4. You'll see a wide variety of sample modeling problems to solve in class, to gain a hands-on knowledge of the fundamentals of packaging modeling.

5. Identifying basic and advanced principles for mechanical stress and thermal diffusion.

6. Understanding how package reliability, power consumption and device performance relate to each other.

7. Learning to make decisions about packaging construction and strategies for evaluating new packaging designs and technologies.

8. You will also be introduced to wafer level simulations; an increasingly necessary skill with the advent of low-k dielectrics.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

OVERVIEW

Semiconductor and integrated circuit technology continues to develop at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The industry is also pushing to use semiconductor devices in an increasing array of applications. To accomplish this, the industry is also driving prices down. This has created a number of challenges related to the packaging of these components.

IC Packaging Design and Modeling is a three day course that offers thorough instruction on the design and modeling of semiconductor packages. We place special emphasis on package interactions with the die. This course is essential for every manager, engineer, and technician who works in semiconductor packaging, using semiconductor components in high performance applications or nonstandard packaging configurations, or supplying packaging tools to the industry.

By focusing on the fundamentals of packaging design and modeling, you'll learn why advances in the industry are occurring along certain lines and not others. Our instructors clearly explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline. You'll learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Packaging Design Overview.** Learn the fundamentals of packaging design, and why modeling has become critical to semiconductor packaging for today's designs.

2. **Mechanical Simulations.** Learn the fundamentals of displacement, strain, stress, and energy. You'll be able to leverage St. Venant's Principle and apply fracture mechanics to a problem.

3. **Thermal Simulations**. Learn heat transfer modeling, and steady-state and transient thermal modeling. The instructor also explains industry standard and compact thermal models.

4. **Modeling Semiconductor Packages.** Learn about the software used for modeling a variety of aspects of semiconductor packaging. You'll also see a number of examples using current modeling tools used by Package Design experts.

COURSE OUTLINE

1. Package Design Principles
    a) Background
    b) ITRS Roadmap Issues
    c) JEDEC Standards for Packaging
    d) Semiconductor Package Designs: What is a Good Packaging Design?
    e) Modeling Software
2. Assembly and Packaging Processes
    a) Assembly and Packaging Processes
    b) Selecting Package Materials
    c) Advanced Packaging
    d) Stacked Die & Stacked Packages
    e) Through Silicon Via (TSV) Interconnects
3. Stress Simulations
    a) Solid Mechanics Concepts
        i. Basics of Displacement, Strain, Stress and Energy
        ii. Leveraging St. Venant's Principle
        iii. Applying Fracture Mechanics
    b) Manufacturability
        i. Thermomechanical Modeling Metrics
        ii. To Model or Not to Model
        iii. Assembly Process Simulations
4. Thermal Simulations
    a) Heat Transfer Principles
    b) JEDEC Thermal Test and Simulations
    c) SteadyState and Transient Thermal Modeling
    d) Application Specific Thermal Simulations
    e) Using Compact Thermal Models
7. Reliability and Coupled Mechanics
    a) Thermomechanical Reliability
        i. Solder Joint Reliability (SJR)
        ii. Single Chip & Multiple Chip Package SJR
        iii. Solder Joint Shape Predictions
    b) Coupled Mechanics
        i. Moisture Diffusion
        ii. Plastic Package "Popcorn" Cracking
8. WaferLevel Simulations
    a) Venturing into New Territory (Submodeling)
    b) ChipPackage Interactions
        i. Interfacial Fracture Mechanics
        ii. Bridging IC Interconnect and Package Gaps
    c) Microelectromechanical Systems (MEMS)
        i. Device Operations
        ii. MEMS Packaging
9. Drop Tests Simulations
    a) Drop Test & Structural Dynamics
    b) Solder Selection & Performance
        i. Leaded Solders
        ii. LeadFree Solders
        iii. Surface Finishes, Solder Pastes, & Metallization
    c) Package Design Effects
        i. Stand-Off Heights
        ii. Ball Array Pattern
        iii. Single Chip & Multiple Chip Packages

Upcoming Webinars:

Wafer Fab Processing WEBINAR
4 Sessions of 4 Hours each
US: October 3 - October 6, 2022 (Mon - Thurs), 8:00AM - 12:00Noon PDT
Visit: https://www.semitracks.com/courses/processing/wafer-fab-processing.php

IC Packaging Design and Modeling WEBINAR
4 Sessions of 4 Hours each
US: October 10 - October 13, 2022 (Mon - Thurs), 8:00AM - 12:00Noon PDT
Visit: https://www.semitracks.com/courses/packaging/ic-packaging-design-and-modeling.php

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!