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InfoTracks

Semitracks Monthly Newsletter

Basic Failure Mechanisms

By Christopher Henderson

This month we conclude our series of Feature Articles on Failure Mechanisms. In last month's Feature Article we discussed Package-Related Failure Mechanisms. This month we will discuss Use Condition Failure Mechanisms.

Use Condition Failure Mechanisms

Use Condition Failure Mechanisms include radiation effects, electrical overstress (EOS), electrostatic discharge (ESD), latchup, and snapback. These mechanisms, especially EOS and ESD, are quite frequently observed in the field. In fact, probably 50% or more of the typical field return failures fall into the categories of EOS and ESD.

Radiation Effects

Radiation effects can be caused by energetic particles from space, or energetic particles resulting from the decay of naturally occurring elements like radon or radium. Energetic particles can result in a phenomenon known as single event upset or SEU. SEU broadly affects memory ICs and ICs with memory (which is quite common today). A particle known as an alpha particle (a helium nucleus stripped of its electrons) can generate significant charge as it travels through a transistor junction. This can interrupt the operation of the IC. The effect is usually not permanent, but in many instances, the power must be cycled to the IC or the IC must be reset to resume normal

In this Issue:

functionality. Radiation effects tend to be worse in space and at high altitudes, but it is becoming more of a problem at ground level as IC geometries shrink and memory usage increases. Alpha particles cannot penetrate very far, so alpha particles must be generated close to the IC surface in order for a failure to occur. More energetic cosmic particles can penetrate through thicker materials, generating alpha particles as a secondary reaction. Designers protect against SEU through parallel design, redundancy in memories, shielding, and specialized processing involving silicon on insulator (SOI).

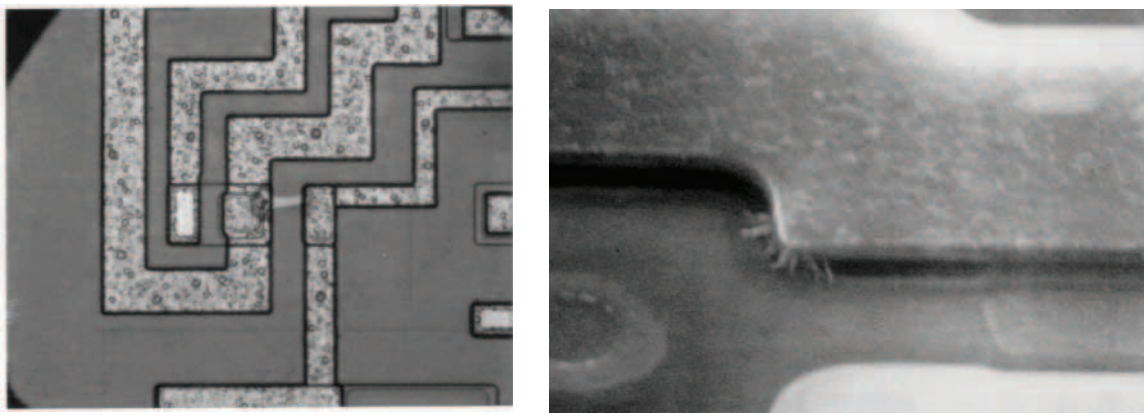
Electrical Overstress (EOS)

Electrical overstress can come from a wide variety of sources, but many are human-caused. Electrical overstress usually creates permanent damage to the IC. Although one must take into account EOS as a failure mechanism, it is hard to determine the reliability impact from these events. Usually, designers will concentrate on creating ICs that are robust to a certain level. If further robustness is necessary, then circuitry at the system level can be used to control potential events.

Electrostatic Discharge (ESD)

ESD is a fast pulse that creates limited damage on the IC. ESD is modeled through three basic circuits: the human body model, the machine model, and the charged device model. The human body model simulates a person's finger zapping the IC, the machine model simulates a charged machine zapping the IC, and the charged device model simulates a charged device discharging into a grounded surface.

One of the most important activities the FA engineer can do when an IC has an EOS or ESD failure is to provide some feedback to the customer as to the voltage levels, current levels, and pulse duration that might have caused the damage. This can be done through experimentation (zapping ICs) and simulation. Usually, a conversation with the customer is necessary to better understand the system level circuitry to provide them with useful data. Figure 1 (a) shows an example of Electrical Overstress and Figure 1 (b) shows an example of Electrostatic Discharge.



(a) (b)

Figure 1 (a) Base to collector short caused by electrical overstress on a bipolar IC and (b) electrostatic discharge causing polysilicon fingers to short between the gate and source of a transistor.

Latchup

Latchup is a phenomenon that occurs in CMOS ICs. Basically, a parasitic bipolar transistor pair is inadvertently turned on, causing a high current in the IC. This interrupts normal operation. Latchup can result in damage to the IC if the current is high enough to melt metal interconnect or bondwires, but this is relatively rare. Latchup is usually mitigated through design and layout techniques, and can be completely eliminated by using SOI.

Snapback

Snapback is a phenomenon that occurs in an NMOS transistor. A voltage pulse that occurs when a n-channel transistor is in saturation can initiate snapback. Like latchup, snapback leads to high current that interrupts the normal operation of the circuit. Once the current is removed, the IC returns to normal operation. Snapback can also infrequently result in damage to metal lines or bondwires.

Both latchup and snapback initiation and hold voltages can be experimentally determined. This can be accomplished using an ESD test system.

This concludes our discussion of basic failure mechanisms.

Technical Tidbit

Field Failure Rate Concepts

This month's Technical Tidbit will cover some basic ideas regarding field failure rates.

It is a waste of time and energy to track annual failure rates (AFR) and then argue about small changes in monthly AFR charts. AFR, or annual returns divided by the installed base of components, is an average and provides little actionable information that is too late and imprecise. It is a waste of expertise, ability, and initiative not to use the actionable information from the available data.

In the semiconductor industry, some customers may ask for age-specific reliability predictions, because their customers (the system manufacturers) asked. They want to know the probability of being dead on arrival, the probability of failure in the first month, first three months, six months, a year, etc. Age-specific reliability predictions provide actionable information because age-specific reliability doesn't change much. Designs change, but manufacturing, packaging, shipping, installation, the environment, and customers don't. Until there is field experience with new products, age-specific reliability predictions can help plan warranty, service, spares production, burn-in, and assist the designers.

It's not necessary to track products and parts by serial number to estimate age-specific reliability. Tracking parts by serial number requires about 1000 times as much data storage capacity and probably generates more than a thousand times as many errors, compared to shipments and returns data. Generally accepted accounting principles require ships and returns data, which is sufficient for estimating age-specific reliability. That means that your company should have sufficient data. Shipments and returns are population data, so reliability estimates from the population have no sample uncertainty.

		No. Returned from Customer																																																
Datecode	No. Shipped to Customer	Jan-10	Feb-10	Mar-10	Apr-10	May-10	Jun-10	Jul-10	Aug-10	Sep-10	Oct-10	Nov-10	Dec-10	Jan-11	Feb-11	Mar-11	Apr-11	May-11	Jun-11	Jul-11	Aug-11	Sep-11	Oct-11	Nov-11	Dec-11	Jan-12	Feb-12	Mar-12	Apr-12	May-12	Jun-12	Jul-12	Aug-12	Sep-12	Oct-12	Nov-12	Dec-12	Jan-13	Feb-13	Mar-13	Apr-13	May-13	Jun-13	Jul-13	Aug-13	Sep-13	Oct-13	Nov-13	Dec-13	Total
Jan-10	403481	0	0	1	1	1	0	1	2	1	0	4	0	0	2	4	3	0	1	2	0	2	2	2	2	1	4	0	0	7	1	1	0	0	2	0	2	1	4	5	7	1	1	4	1	4	2	0	2	81
Feb-10	404616	0	0	0	1	2	2	1	1	0	1	1	1	0	2	1	0	2	1	3	1	3	0	2	0	2	0	2	2	0	4	3	4	3	4	0	3	4	2	5	2	3	4	3	3	1	3	3	3	88
Mar-10	496938	0	0	0	0	1	1	1	2	0	2	0	0	3	5	1	5	0	2	2	4	1	3	3	0	2	1	2	3	3	3	3	3	6	2	2	1	3	2	2	4	3	1	0	5	3	2	2	4	98
Apr-10	400060	0	0	0	0	0	0	0	0	4	2	3	0	2	0	1	0	0	1	1	1	1	1	0	3	3	1	1	1	2	1	1	1	2	1	3	1	2	3	3	2	1	4	0	1	5	4	2	2	67
May-10	400130	0	0	0	0	0	0	0	1	0	1	1	2	0	2	1	0	4	0	1	2	2	0	2	0	0	1	1	2	0	3	1	3	0	2	1	1	2	1	0	4	1	2	3	2	1	4	1	6	61
Jun-10	499727	0	0	0	0	0	0	0	0	1	0	0	1	1	2	0	0	0	1	0	2	2	2	0	1	1	3	0	1	0	1	2	2	1	1	2	4	3	3	1	0	2	3	2	3	0	1	5	1	55
Jul-10	400696	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0	2	0	2	0	1	0	0	0	2	3	2	0	1	2	0	1	0	2	0	0	0	4	0	1	1	2	0	0	2	2	1	3	37
Aug-10	399967	0	0	0	0	0	0	0	0	0	2	0	0	0	1	2	3	0	1	1	0	1	0	0	4	0	1	0	0	1	3	2	0	1	0	0	2	2	0	1	0	0	1	3	1	1	0	1	0	35
Sep-10	501468	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	3	1	1	0	2	1	0	2	0	3	2	1	0	1	2	1	0	2	2	1	1	1	0	2	0	1	1	1	2	2	5	45
Oct-10	396390	0	0	0	0	0	0	0	0	0	0	1	0	2	1	0	0	0	0	2	0	1	1	0	0	3	0	2	1	0	0	0	1	0	3	0	2	3	0	0	0	2	2	2	2	0	1	4	1	37
Nov-10	405644	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	1	1	0	0	2	0	2	0	1	0	1	1	1	0	1	0	2	1	2	3	1	0	2	1	1	2	0	2	0	1	2	34
Dec-10	498003	0	0	0	0	0	0	0	0	0	0	0	0	1	0	2	0	0	2	1	1	0	0	1	1	3	0	0	2	1	1	1	6	0	1	0	0	0	1	1	3	2	1	2	0	1	2	1	0	38
Jan-11	401757	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	2	0	0	1	0	0	1	4	0	0	0	0	1	0	1	0	0	0	2	1	0	3	2	0	2	0	1	1	24
Feb-11	398842	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	2	0	0	0	1	1	1	0	1	0	2	0	2	0	0	0	1	0	0	0	1	1	0	1	0	1	3	0	0	2	22
Mar-11	500013	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	2	1	1	0	0	0	1	0	3	0	1	0	0	2	2	0	1	3	2	0	0	0	1	1	0	3	0	0	1	0	27
Apr-11	397780	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	2	1	0	3	0	1	0	1	0	0	0	1	3	0	1	1	0	0	1	0	0	1	3	0	1	0	0	3	23
May-11	397976	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	2	1	0	0	0	0	2	0	0	1	1	3	2	0	0	0	0	0	1	0	0	1	0	0	2	0	0	19
Jun-11	497701	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	3	1	0	0	1	0	0	1	0	0	0	0	2	0	0	1	0	0	1	0	0	0	0	1	0	0	3	15
Jul-11	396187	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	2	0	0	0	0	1	0	1	5	1	0	0	1	3	0	18
Aug-11	405010	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	2	2	0	1	0	1	2	1	0	0	1	0	0	0	1	0	0	2	0	0	1	1	1	0	1	18
Sep-11	496969	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	2	0	0	0	0	2	0	0	2	2	2	0	1	0	0	1	1	2	0	0	1	1	20
Oct-11	400385	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	3	0	0	2	0	1	1	0	0	0	0	0	1	1	1	1	0	0	2	0	0	14
Nov-11	403357	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0	1	1	2	0	0	0	0	0	1	0	0	1	0	1	0	10
Dec-11	504622	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	2	0	3	0	0	0	6	1	0	0	1	2	19
Total	10407719	0	0	1	2	4	3	3	6	6	8	11	7	10	17	13	15	10	16	22	14	22	19	16	22	24	19	22	26	22	24	22	31	25	29	18	28	31	23	28	30	24	36	37	27	30	29	31	42	905

FITS	14.4924487
MTBF	69,001,452

Table 1. An Example of Field Failure Statistics.

Table 1 is an example of how to utilize field data statistics by examining devices as a function of datecode and return date. This table shows monthly data on field returns for a high volume product. The FIT rate is quite good, on the order of 14 FITS, and the Mean Time Between Failures (MTBF) is approximately 69 million hours. While the FIT rate and MTBF are both quite good, we may want to delve into the data in more detail to see if there are any underlying trends or issues.

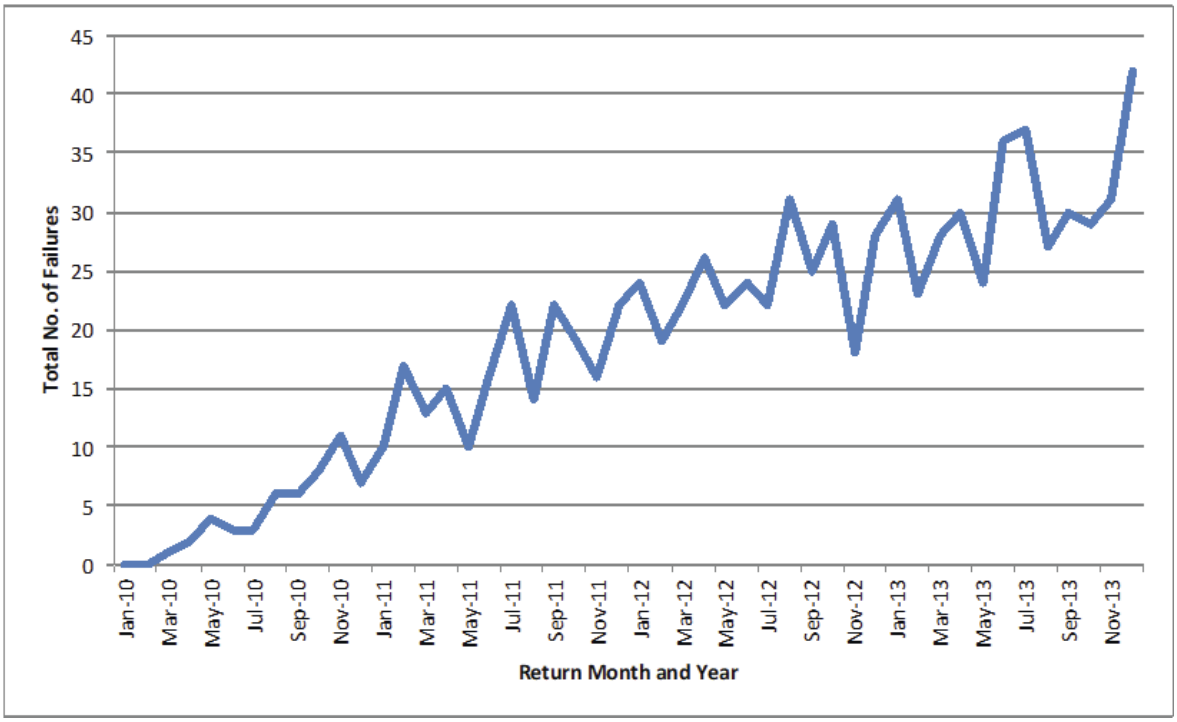


Figure 1. Total Number of Failures as a Function of Time.

Figure 1 shows the field reliability estimated from the ships and returns data in Table 1. Notice that the field returns increase over time as more product makes its way into the field.

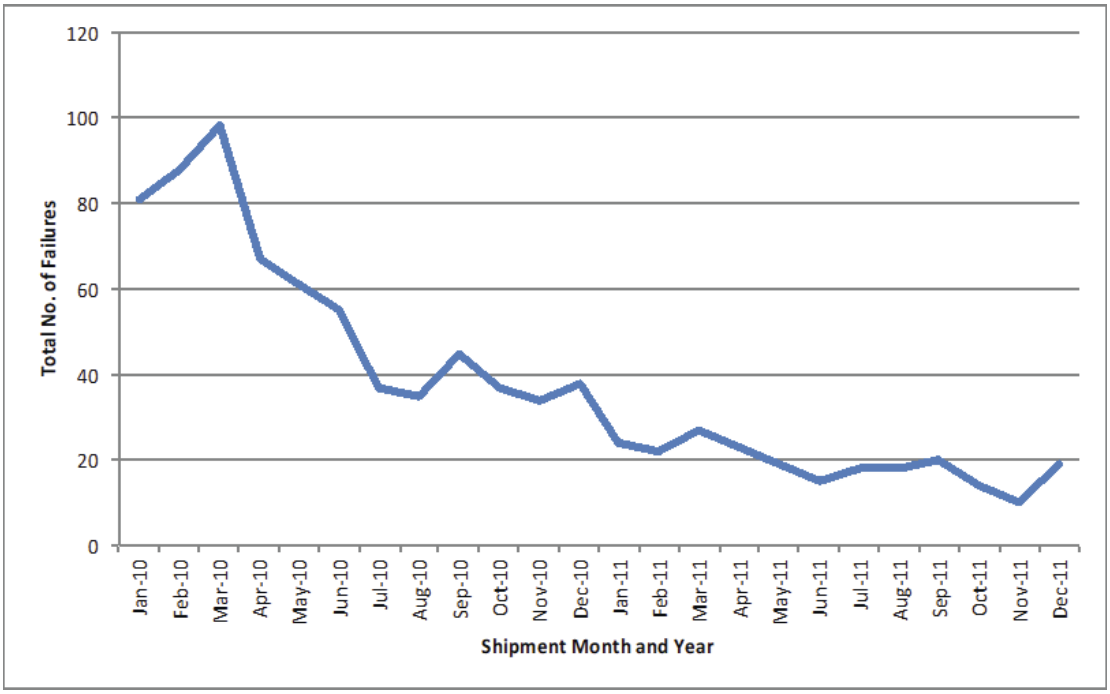


Figure 2. Total Number of Failures as a Function of Ship Date.

Notice, however, that the number of field failures drops for newer datecodes, as shown in Figure 2. This is partially due to the fact that older products have had more time to potentially fail. However, that doesn't completely explain the drop, since the drop is not linear. The non-linear drop indicates that the products improved shortly after being introduced, helping to further reduce the failure rate.

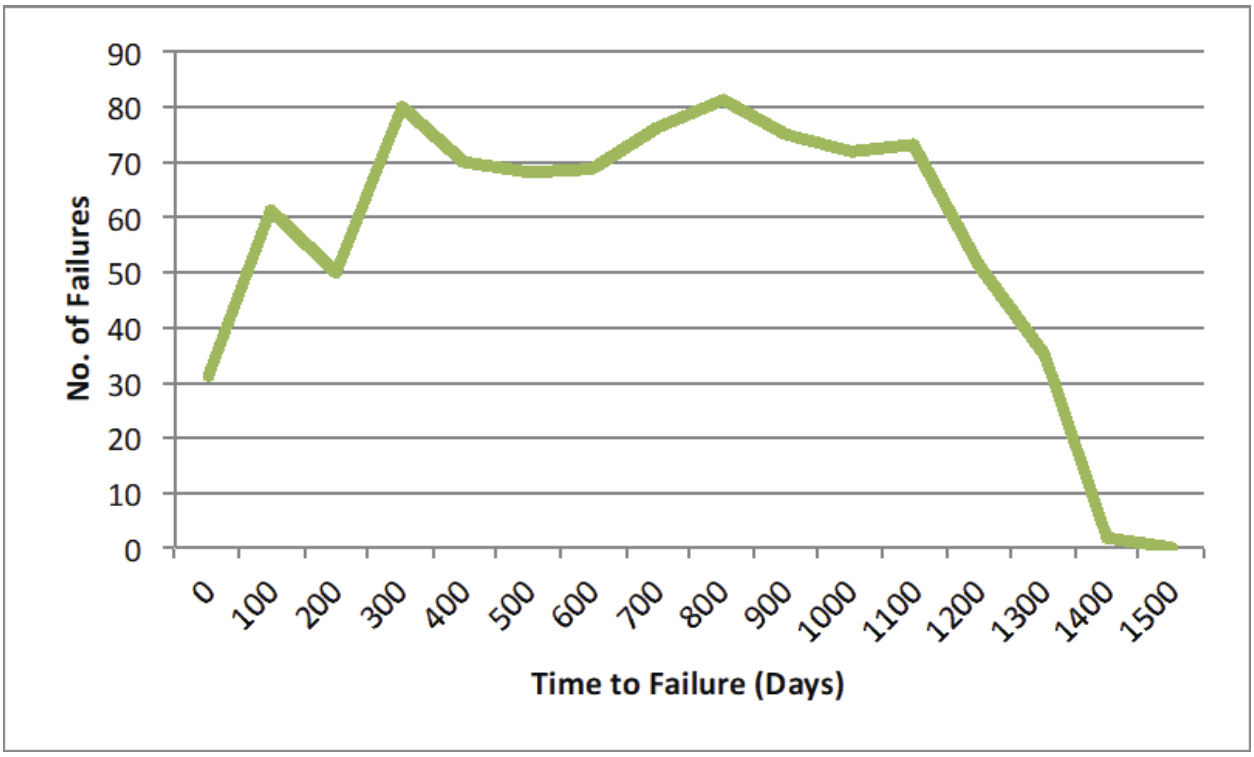


Figure 3. Number of Failures as a Function of the Time to Failure.

The graph in Figure 3 shows the field returns by age of the component. Notice that the field returns initially increase, but then saturate at longer use timeframes. The tail-off in failure rates at the higher numbers is an artifact of insufficient data due to few components being in the field that long.

One can use the information in this article to better predict the reliability of the product, and provide feedback to manufacturing and reliability engineering as to the real reliability levels.

Ask the Experts

Q: I understand that one of the disadvantages of sawing packaged components to singulate them is the cost, but I also understand that sawing packaged components can allow for higher throughput. These concepts seem to contradict each other. Can you help explain this?

A: There is a subtlety here to understand. There are two types of sawing processes one can use to singulate packaged ICs: a tape-mounted process and a vacuum jig-mounted process. Using tape is costly, since you would need a piece of tape for each leadframe strip you singulated. Using a vacuum jig would be lower cost, since no tape is involved. In general, though, sawing gives you higher throughput than punching because you can effectively saw apart a leadframe faster than you can punch the units from the leadframe.

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Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills
   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless

f. Thermal Interface Materials (TIMs) and Lids
g. Fine Pitch Warpage Reduction
h. Stacked Die and Stacked Packages
i. Material Selection for Board Level Temperature Cycling and Drop Reliability

4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

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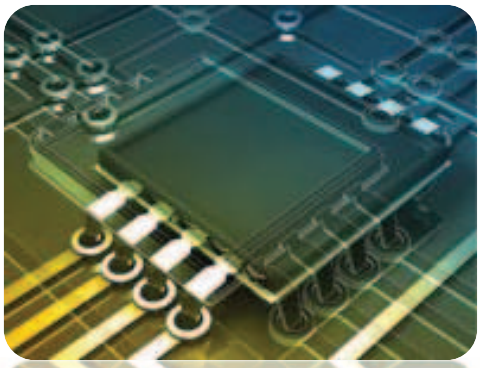

Upcoming Webinars

(Click on each item for details)

Semiconductor Reliability / Product Qualification

4 sessions of 4 hours each
Europe: August 30 – September 2, 2021
(Mon – Thur), 1:00 P.M. – 5:00 P.M. CET

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