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Semitracks Monthly Newsletter

Photonics Device Fundamentals

By Christopher Henderson

In this month's feature article, we will begin a series on photonics device fundamentals. This will be the first in a series of four articles. We begin this month with a discussion of Light Emitting Diodes (LEDs), Laser Diodes, and Resonant Cavities.

There are three basic building blocks to optical electronic systems: energy converters, manipulators and passive components. Energy converters include emitters and detectors. Manipulators include modulators, amplifiers and switches. Passives include waveguides, splitters and combiners, couplers, filters, and wavelength converters.

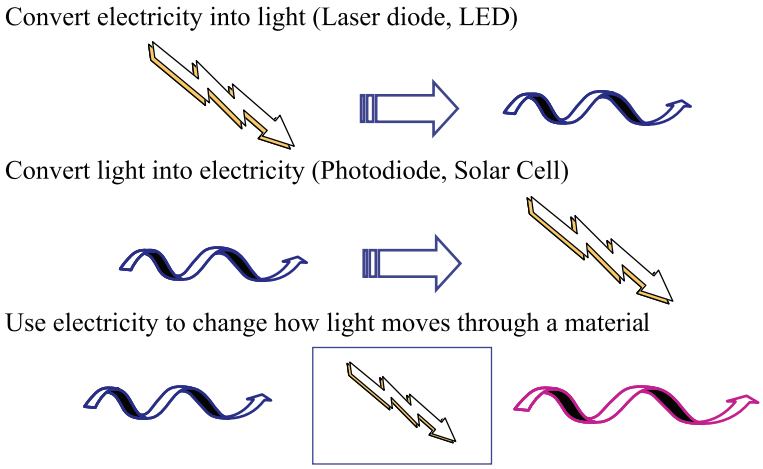

Figure 1. Illustration of active optoelectronics.

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In an active optoelectronics system, we may need to convert electricity into light, as illustrated in the upper part of Figure 1. We can use a laser diode or a light emitting diode for this process. We may also need to convert light into electricity. We can use a photodiode or a solar cell to do that. We may need to use electricity to change how light moves through a material, as illustrated in the lower part of Figure 1.

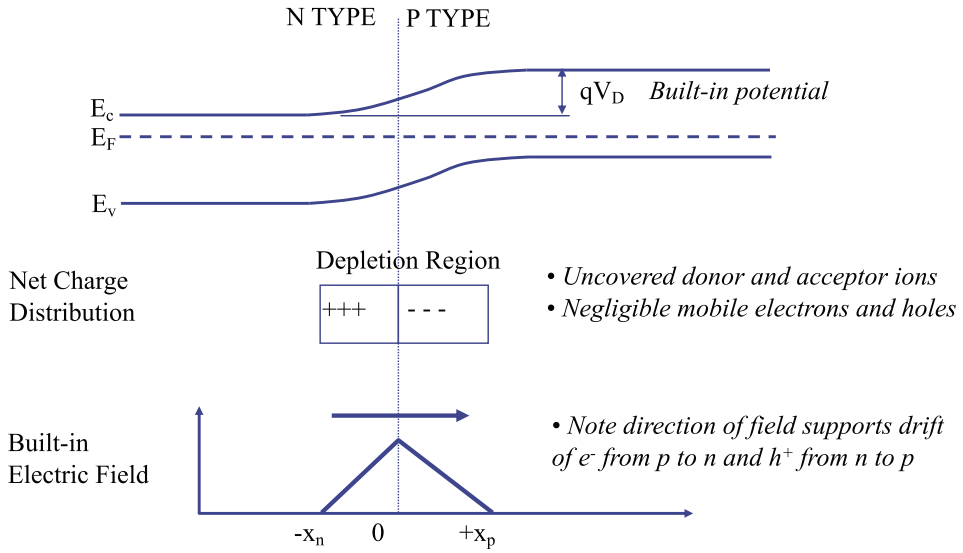


Figure 2. Illustration of energy band diagram for pn junction.

Let's begin by discussing the pn junction with no external bias. We show the energy band diagram for the pn junction here in Figure 2. The difference in the conduction band height from the n-type to the p-type material represents the built-in potential of the junction. At the interface between the n- and p-type semiconductor there will be a depletion region, where there is fixed positive and negative charge in the dopant atoms, and negligible free carriers. The separation of the fixed positive and negative charge leads to a built in electric field. The direction of the electric field vector will be from left to right in this configuration, supporting the drift of electrons to the left, and the drift of holes to the right.

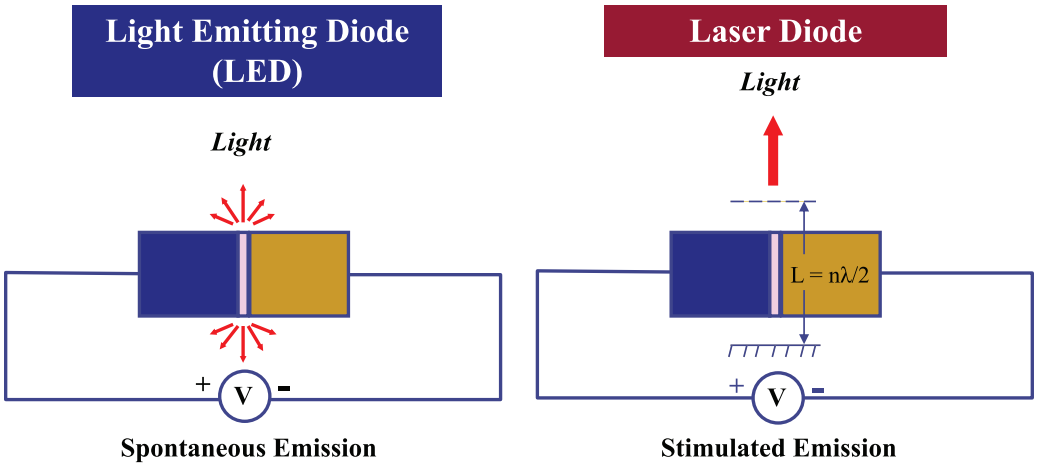


Figure 3. Illustration of LEDs and laser diodes.

In a light emitting pn junction diode, as seen on the left of Figure 3, one can place a bias across the junction and create spontaneous emission, as the carriers recombine. In a laser diode, as seen on the right of Figure 3, one can place a bias across the junction, and when the carriers recombine, this transfers energy into the crystal structure, creating light. This is known as stimulated emission.

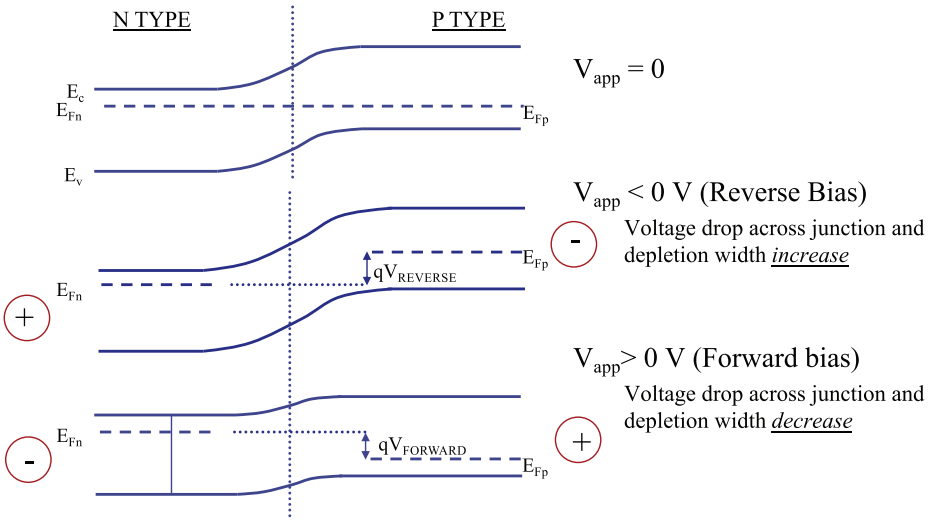
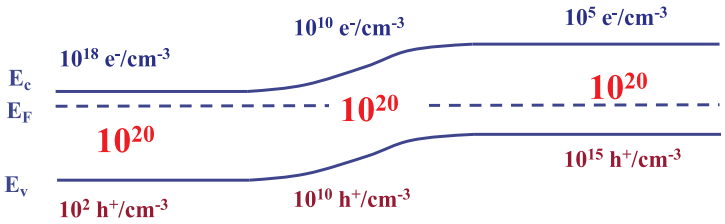


Figure 4. Biasing LEDs and laser diodes.

Let's now look at the three biasing conditions in Figure 4. First, we show the zero-bias condition. In this condition, the Fermi Level is flat across both the p- and n-type material. In the reverse bias condition, both the voltage drop across the junction and the depletion width increase. In the forward bias condition, both the voltage drop across the junction and the depletion width decrease.

At zero bias, the Electron/Hole Product across a pn junction is small



Forward bias exponentially increases the Electron/Hole Product in the junction

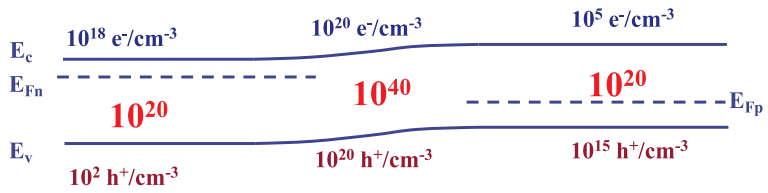


Figure 5. Biasing LEDs and laser diodes (cont.).

As shown in Figure 5, when we have zero bias across the LED or laser diode structure, the electron-hole concentration across the pn junction is quite small, on the order of 10^{20} carriers per cm^3. However, during forward bias, the carrier concentration increases exponentially across the junction, to the order of 10^{40} carriers per cm^3.

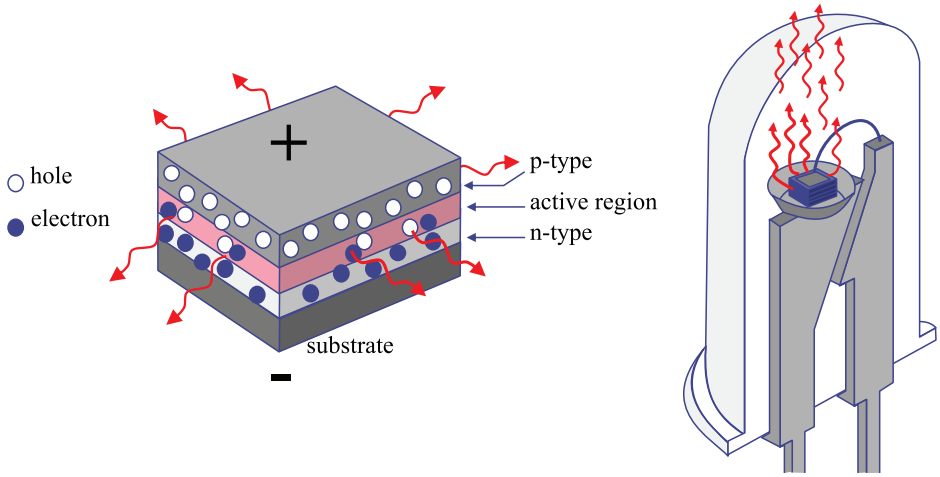


Figure 6. LEDs: spontaneous emission.

As shown on the left in Figure 6, when an LED is forward biased, the p-type semiconductor injects holes into the n-type region, and the n-type semiconductor injects electrons into the p-type region. The carriers will recombine on both sides of the junction and emit light in all directions. Therefore, in a packaged LED, engineers add in external reflectors that are required to direct the light in the appropriate direction, like we show here on the right of Figure 6.

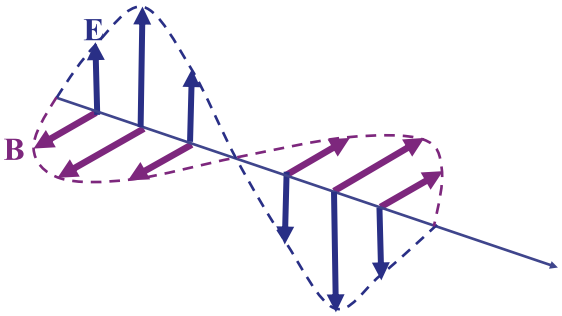


Figure 7. Lasers: stimulated emission is an electromagnetic wave.

In a laser diode, the physical properties associated with their operation are somewhat different. Recall that light is an electromagnetic wave with both electrical and magnetic properties (as illustrated in Figure 7). The electric field of the photons exerts a force on the electrons in the conduction band. The force is in sync with the light wave, and it stimulates the recombination of an electron-hole pair.

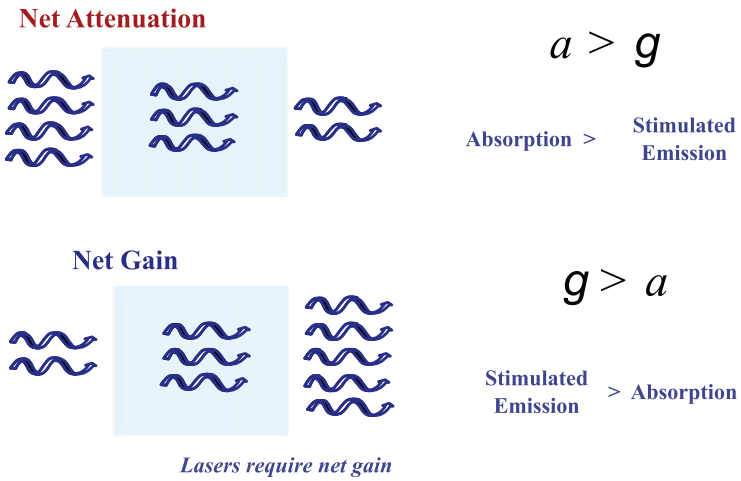


Figure 8. llustration of net absorption or net gain.

The concepts of attenuation and gain are important in relation to the operation of a laser diode. As shown in the upper portion of Figure 8, net attenuation occurs when the absorption is greater than the stimulated emission. Net gain occurs when the stimulated emission exceeds the absorption, as illustrated in the lower portion of Figure 8.

The emission wavelength in laser diodes is dependent on two properties. The laser wavelength is determined by the mirror spacing and the effective index of refraction. It is also dependent on the bandgap of the active region of the laser.

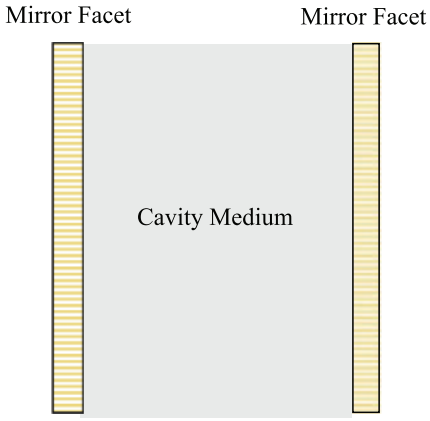


Figure 9. Illustration of Fabry-Perot optical resonator .

One method for controlling the wavelength is to create a structure known as a Fabry-Perot optical resonator. As illustrated in Figure 9, these structures consist of a cavity made from a particular semiconductor material with mirror facets on both sides of the cavity. The structure creates resonant optical modes by light reflecting from the end mirrors.

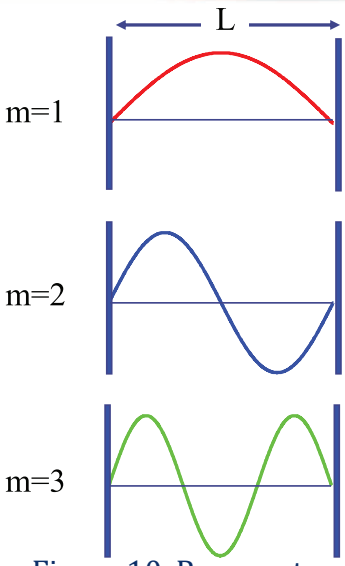


Figure 10. Resonant cavities.

A resonant cavity creates a quantum mechanical condition where the amplitude of the light wave must be zero at each end of the cavity so it only allows wavelengths that satisfy the conditions where λ, the wavelength, is equal to two times the length of the cavity divided by m, where m is an integer greater than or equal to one. This can create wave patterns like we show in Figure 10.

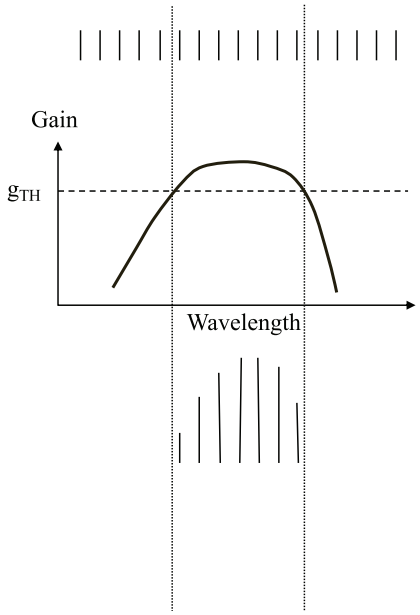


Figure 11. Illustration of cavity mode spectrum.

We can use resonant cavities to create a cavity mode spectrum. A large number of discrete wavelengths satisfy the constructive interference requirement within the cavity. However, only over a limited range of wavelengths will the gain be sufficient for creating laser action. Therefore, as shown in Figure 11, the cavity mode spectrum will only consist of the wavelengths that satisfy both statements above.

Next month, we will continue with part two in the series.

Technical Tidbit

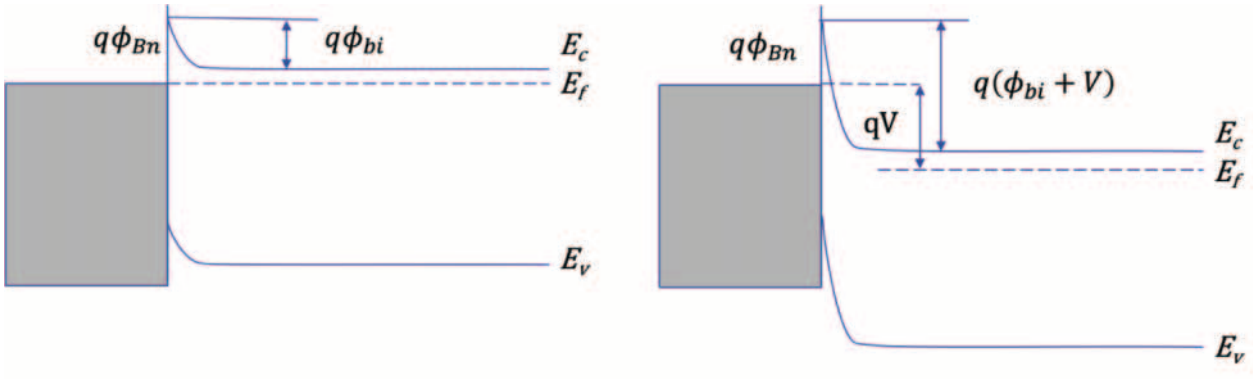
Silicide Schottky Barriers

In this technical tidbit, we will discuss Schottky barriers associated with silicides and how to measure the barrier height.

Silicides tend to be used as a contact material between metal and the silicon substrate, or polysilicon gates. After metal is deposited on Si, an annealing step is applied to form a silicide-Si contact. The term "metal-silicon contact" includes silicide-Si contacts. Over the years, engineers have used a number of different silicide materials for this purpose.

Silicide	$ErSi_{1.7}$	HfSi	$MoSi_2$	$ZrSi_2$	$TiSi_2$	$CoSi_2$	WSi_2	NiSi	Pd_2Si	PtSi
ϕ_{Bn} (V)	0.28	0.45	0.55	0.55	0.61	0.65	0.67	0.67	0.75	0.87
ϕ_{Bp} (V)			0.55	0.49	0.45	0.45	0.43	0.43	0.35	0.23

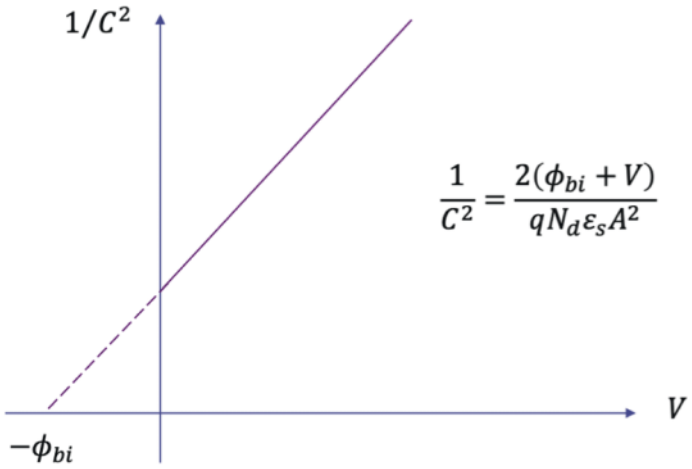
The table shown here covers many of the silicide materials used in the semiconductor industry. From a Schottky barrier perspective, an ideal candidate would be one that exhibits a similar barrier height for both n- and p-type silicon. In practice though, this may not be the main factor, as other factors like resistivity, stability, and ease of processing are usually more important. Even though this table shows measured values, it is important to measure the barrier height experimentally to account for the unique factor associated with the process. In general, silicide-Si interfaces are more stable than metal-silicon interfaces.



$$q\phi_{bi} = q\phi_{Bn} - (E_c - E_f) \qquad = q\phi_{Bn} - kTln\frac{N_c}{N_d}$$

$$W_{dep} = \sqrt{\frac{2\varepsilon_s(\phi_{bi}+V)}{qN_d}} \qquad C = \frac{\varepsilon_s}{W_{dep}}A$$

The most common method for measuring the Schottky barrier height is the Capacitance-Voltage plot, or CV plot. Let's briefly review the device physics. The figure above shows the energy band diagram and basic equations for the Schottky barrier. The Schottky barrier, $q\phi_{bi}$ is the difference between the silicide to silicon workfunction difference ($q\phi_{Bn}$) minus the difference between the Conduction Band (E_C) and the Fermi Level (E_F) of the silicon. This can be re-written in terms of the doping concentration. The width of the depletion region (W_{dep}) is the square root of this formula. Finally, the capacitance is the ratio of the dielectric constant of the silicon over the depletion width times the area. So how do we then plot the CV data to extract the barrier height?



Once ϕ_{bi} is known, ϕ_B can be determined using:

$$q\phi_{bi} = q\phi_{Bn} - (E_c - E_f) = q\phi_{Bn} - kTln\frac{N_c}{N_d}$$

In order to extract the barrier height, we plot the data as shown here, using one over the square of the capacitance as the y-axis and the voltage as the x-axis. The x-intercept is the negative of the barrier height. Once we know $q\phi_{bi}$, we can calculate $q\phi_b$ using the equation shown above.

Ask the Experts

Q: How thick is the Buried Oxide (BOX) typically in Silicon-On-Insulator (SOI)?

A: It varies from process to process, but it can range from 1 – 2 microns in older SOI technologies to as thin as 10nm in state-of-the-art SOI devices with adaptive back-body biasing.

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

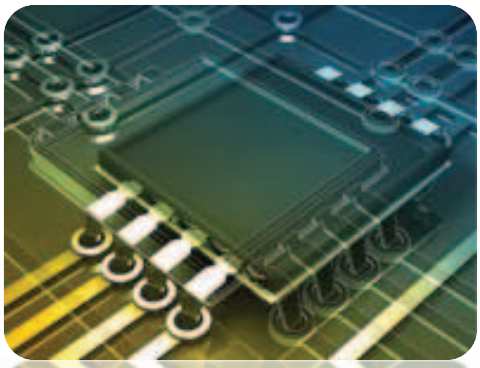
1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
   b. Scaling



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We are always looking for ways to enhance our courses and educational materials.

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We look forward to hearing from you!

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(Click on each item for details)

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April 6 – 9, 2021 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 6 – 9, 2021 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 12 – 15, 2021 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 19 – 20, 2021 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 22, 2021 (Thur)
Munich, Germany