Issue 122 August 2019

# InfoTracks

Semitracks Monthly Newsletter

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## Infrared Thermography Part 2

### By Christopher Henderson

In last month's feature article, we introduced the topic of infrared thermography. We covered blackbody radiation as well as information on emissivity and reflectivity. In this month's article, we'll continue to cover infrared thermal imaging (or infrared thermography) in more detail.

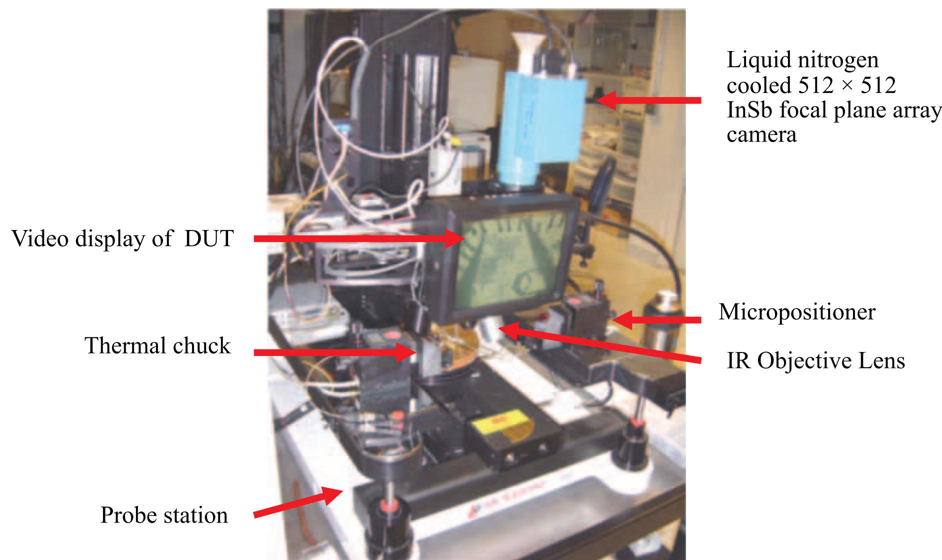


Figure 6. Example of infrared thermal imaging microscope.

This photograph in figure 6 shows an example of an infrared thermal imaging microscope. The system consists of a probe station

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with an IR camera mounted on it. In this case, the camera is a liquid nitrogen-cooled 512 x 512 indium antimonide array camera. The IR image can be seen on the video display. The circuit can be powered through a probe card, or through individual probes. In this system, the stage can be heated if necessary.

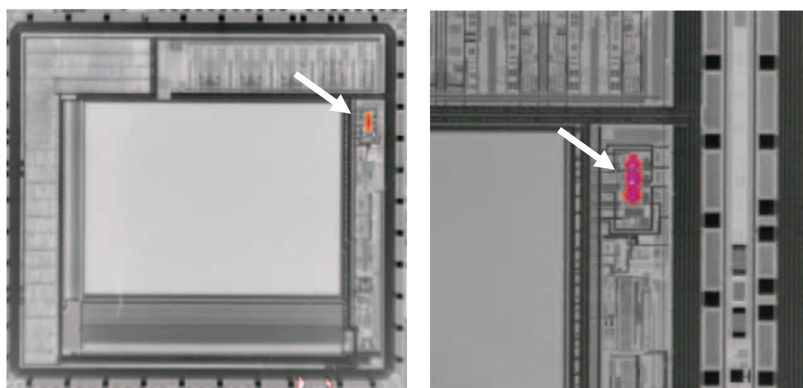


Figure 7. Reflected + emitted IR composite images using 2x objective (left) and 5x objective (right).

Here is an example analysis using infrared thermal imaging. This particular integrated circuit is a CMOS imaging circuit with leakage in a driver circuit. The arrow in the left-hand image indicates the location of the leakage. The images are a composite of reflected infrared light and emitted infrared light. The image on the right-hand side shows a higher magnification image of the leaky circuit.

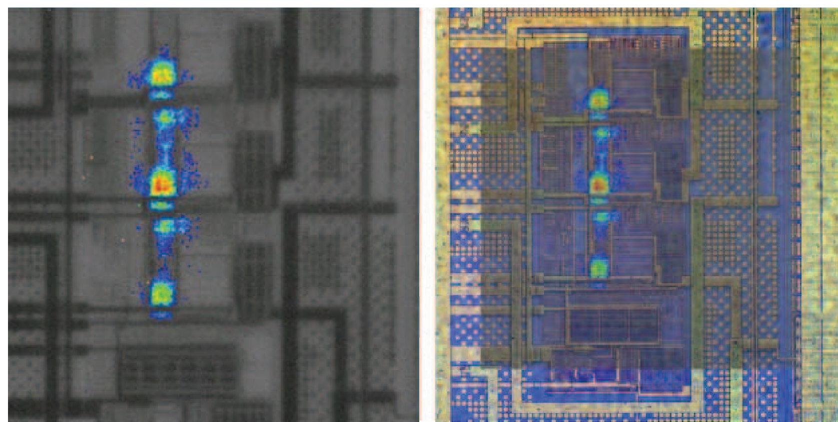


Figure 8. Higher magnification images of infrared thermal emission.

These images in Figure 8 show the infrared thermal emission at a higher magnification. The image on the left shows a composite reflected IR-emitted IR image, and the image on the right shows the emitter IR

image overlaid on an optical image of the area in question. Again, the spatial resolution of the technique is limited to around 5µm, but it does allow one to rapidly and non-destructively locate the area where the leakage is occurring. Further analysis work will be necessary to localize the exact defect spot.

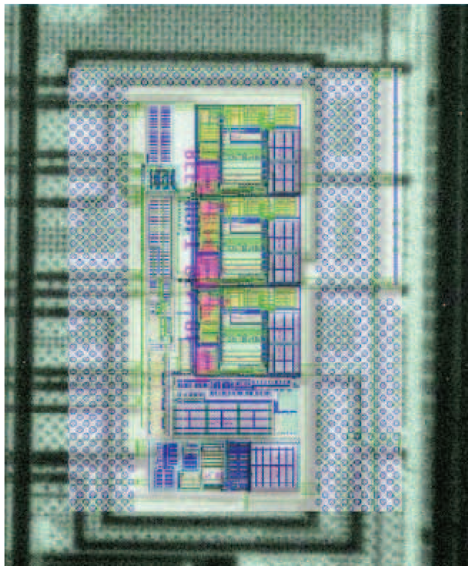


Figure 9. IR image with CAD overlay.

This image in Figure 9 shows the emitted IR overlaid on a computer-aided design database image of the area in question. This particular circuit containing a group of PMOS transistors was found to exhibit a low drain to source breakdown voltage.

Resolution is an important topic in failure analysis, but it is ill-defined. The best definition of resolution, at least one that is quite widely used, is the definition stated by Lord Rayleigh. He stated that "The rule is convenient on account of its simplicity and is sufficiently accurate in view of the necessary uncertainty as to what is meant by resolution." In other words, he didn't have a good method for determining it, so he therefore declared it to be 61% of the wavelength divided by the numerical aperture of the optics system. For infrared thermal imaging, that means that the resolution is approximately 61% of the wavelength, given a numerical aperture of one. Most standard optical systems have a numerical aperture less than one, although newer techniques allow values greater than one.

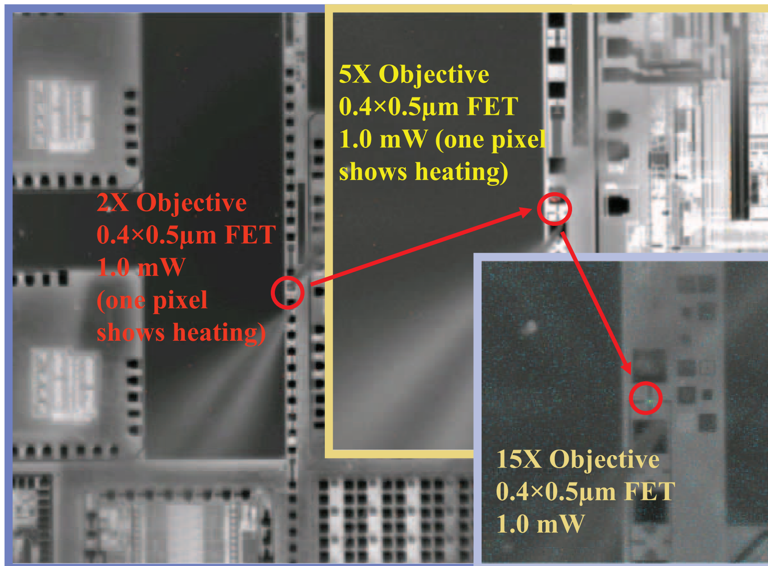



Figure 10. IR sensitivity practical limits.

This image in Figure 10 shows the practical limits to the sensitivity of the system. At 20X and 50X magnification, the heat-generating location is limited to one pixel. At 150X, the heat generating site is beginning to spread out somewhat. The power of the tool is not in its resolution, but rather its ability to image non-destructively. No coatings are required, as is the case with liquid crystals and FMI.

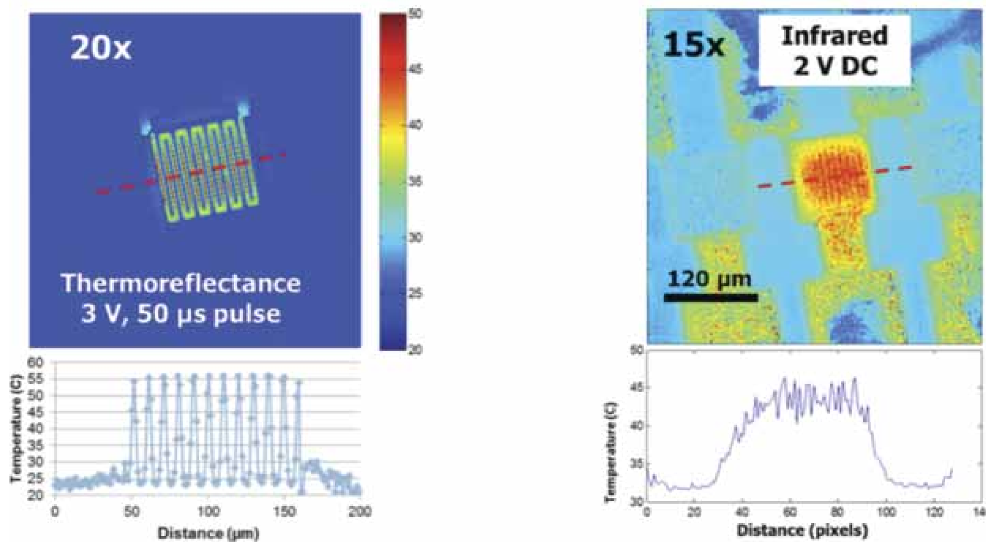



Figure 11. Thermoreflectance Thermal Imaging (TTI).

Thermal imaging is now beginning to benefit from improvements in pulsed imaging using thermoreflectance measurements. These newer systems use hyperspectral detectors to take advantage of data at different frequencies. The image on the left in Figure 11 shows an example of thermoreflectance data on a test structure. The engineer pulses the structure with 3 volts at a 50 µsec pulse rate. One can clearly see the temperature rises of 30°C in the metal lines. In the DC IR thermal image on the right, the heat expands rapidly, reducing the thermal definition in the structure, making it difficult to see the temperature rise in the metal interconnect.

## References

Figure 6

Photograph courtesy Freescale Semiconductor

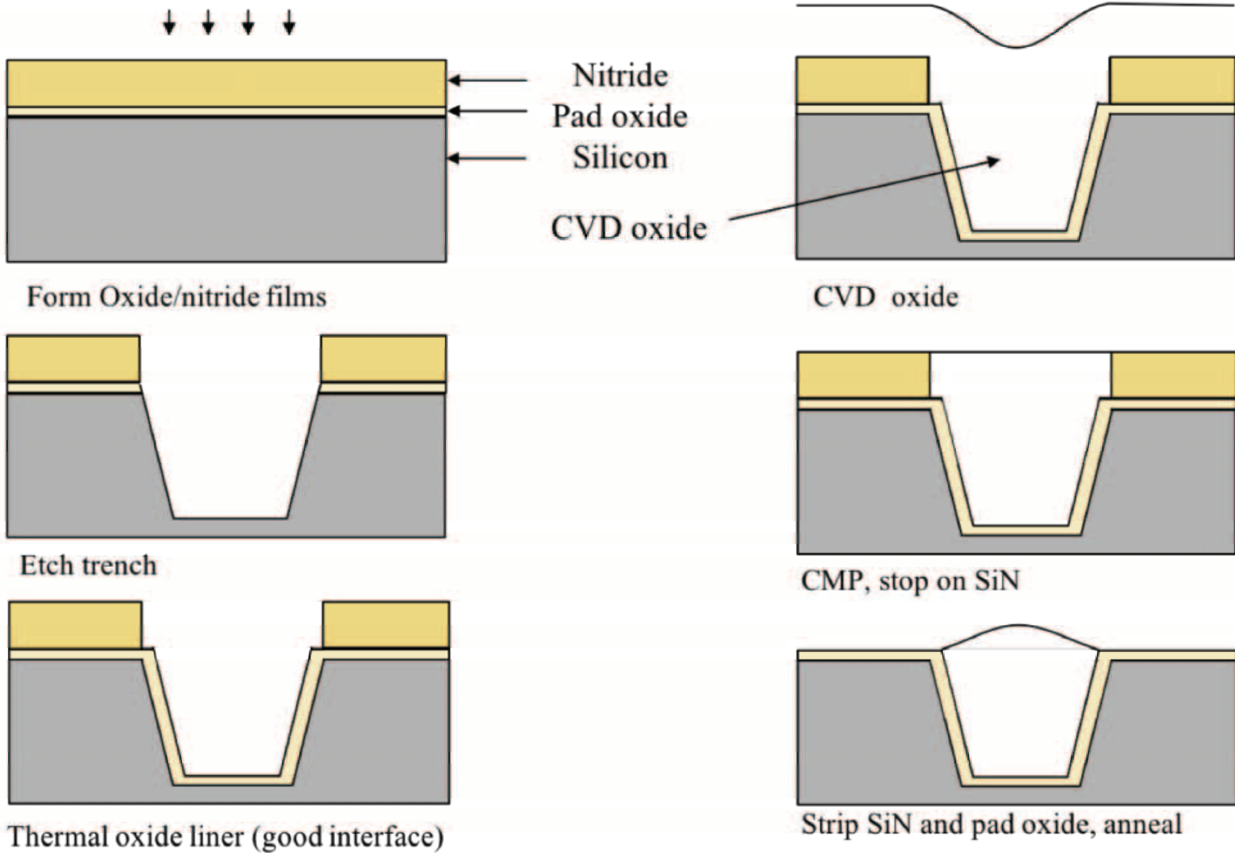
Figures 7 – 10

Images courtesy Freescale Semiconductor

# Technical Tidbit

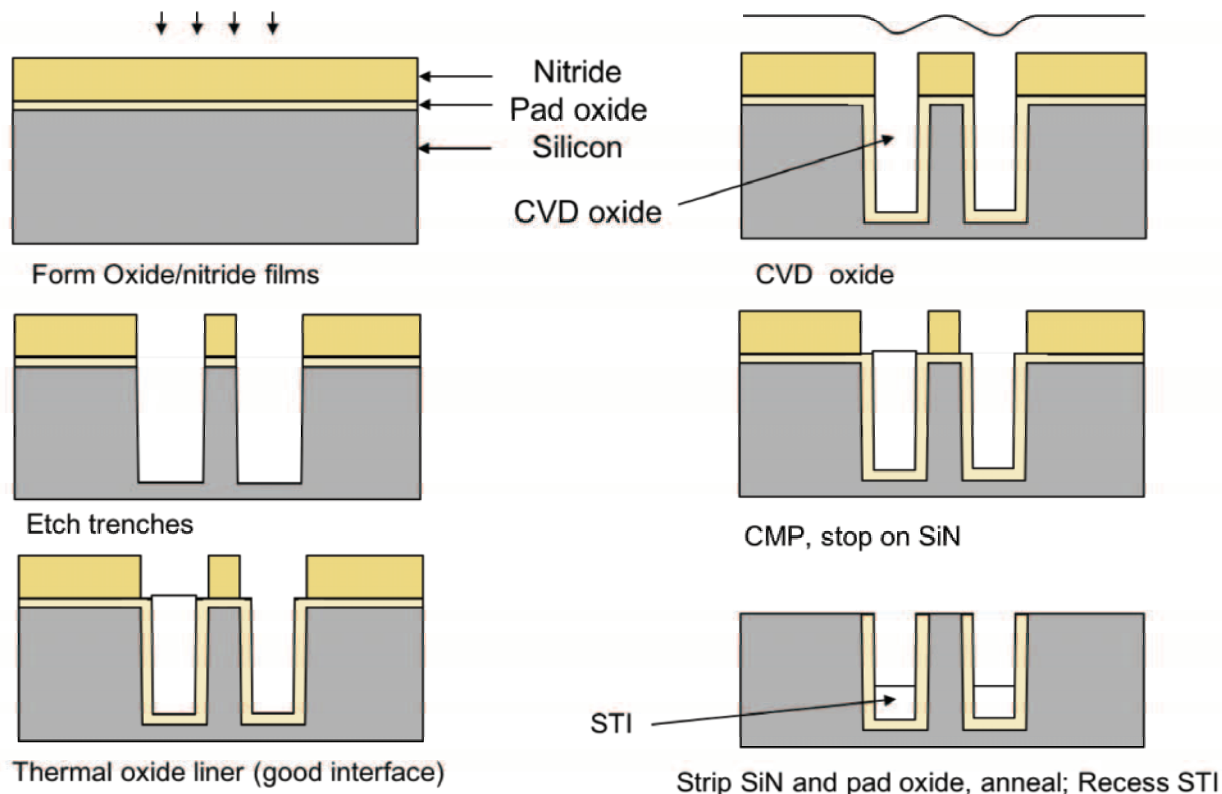
## Shallow Trench Isolation

This month's technical tidbit covers shallow trench isolation.




First let's review the most common isolation process, Shallow Trench Isolation, or STI. The process for shallow trench isolation is similar to a recessed LOCOS process. First, one deposits the pad oxide, followed by the silicon nitride films. The opening for the trench is patterned, and the trench is etched. In the STI process however, the trench is not as deep as the recessed LOCOS process. Next, the trench is lined with a thermal oxide that has good interface qualities. We want to avoid charge trapping and parasitic

transistors in the trench itself. Next, the trench is filled with a deposited oxide. Once the trench is full, one uses chemical mechanical planarization to polish the oxide off the surface of the wafer. The nitride cap can be used as a stopping layer. Finally, the nitride and the pad oxide are stripped from the wafer surface, leaving the filled trench.




The isolation process flow for FinFETs is very similar to the standard shallow trench isolation process. First, one deposits the pad oxide, followed by the silicon nitride films. The openings for the trenches are patterned, and the trenches are etched. Next, the trenches are lined with a thermal oxide that has good interface qualities. We want to avoid charge trapping and parasitic transistors in the trenches themselves. Next, the trenches are filled with a deposited oxide. Once the trenches are full, one uses chemical mechanical planarization to polish the oxide off the surface of the wafer. The nitride cap can be used as a stopping layer. The nitride and the pad oxide are stripped from the wafer surface, leaving the filled trenches. Finally, we etch away a portion of the STI, leaving the elevated fin structures. Some process variation issues for the isolation steps include control of fin height, width, slope, and fin roughness. The CMP process might also create issues related to fracturing of the fins, contamination, or non-uniform fin heights.

## Ask the Experts

**Q: What does UTG/LTG stand for?**

**A:** UTG stands for Upper Test Guardband, and LTG stands for Lower Test Guardband. These values are typically established during the characterization of first silicon. Test or Validation engineers might look at a parameter over a supply voltage range, or a temperature range, examine the distribution of the values, and then use the results to establish the Upper and Lower Test Guardbands that would be used during Production Testing.

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# **Spotlight:** Wafer Fab Processing

## OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

## COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

## INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

## COURSE OUTLINE

**Day 1**

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

**Day 2**

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

**Day 3**

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

**Day 4**

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

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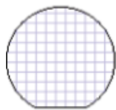

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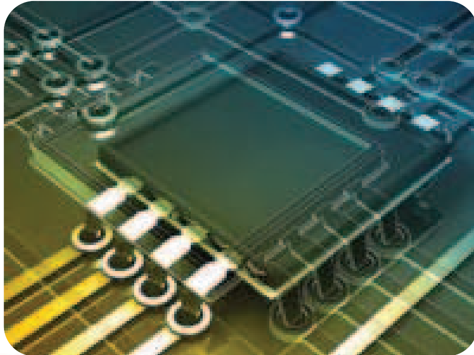

# Feedback

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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# Upcoming Courses

**(Click on each item for details)**

## Introduction to Processing
**March 2 – 3, 2020 (Mon – Tue)**
**Portland, Oregon, USA**

## Failure and Yield Analysis
**March 2 – 5, 2020 (Mon – Thur)**
**Portland, Oregon, USA**

## Advanced CMOS/FinFET Fabrication
**March 4, 2020 (Wed)**
**Portland, Oregon, USA**

## IC Packaging Technology
**March 5 – 6, 2020 (Thur – Fri)**
**Munich, Germany**

## Semiconductor Reliability / Product Qualification
**March 9 – 12, 2020 (Mon – Thur)**
**Portland, Oregon, USA**

## Wafer Fab Processing
**April 14 – 17, 2020 (Tue – Fri)**
**Munich, Germany**

## Semiconductor Reliability / Product Qualification
**April 14 – 17, 2020 (Tue – Fri)**
**Munich, Germany**

## Failure and Yield Analysis
**April 20 – 23, 2020 (Mon – Thur)**
**Munich, Germany**

## IC Packaging Technology
**April 27 – 28, 2020 (Mon – Tue)**
**Munich, Germany**

## Advanced CMOS/FinFET Fabrication
**April 30, 2020 (Thur)**
**Munich, Germany**