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Oxidation Part 3

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In the final installment of our series, we will discuss the subject of oxidation. Last month, we discussed oxidation systems. This month, we'll discuss the properties of the silicon/silicon dioxide interface and oxide traps.

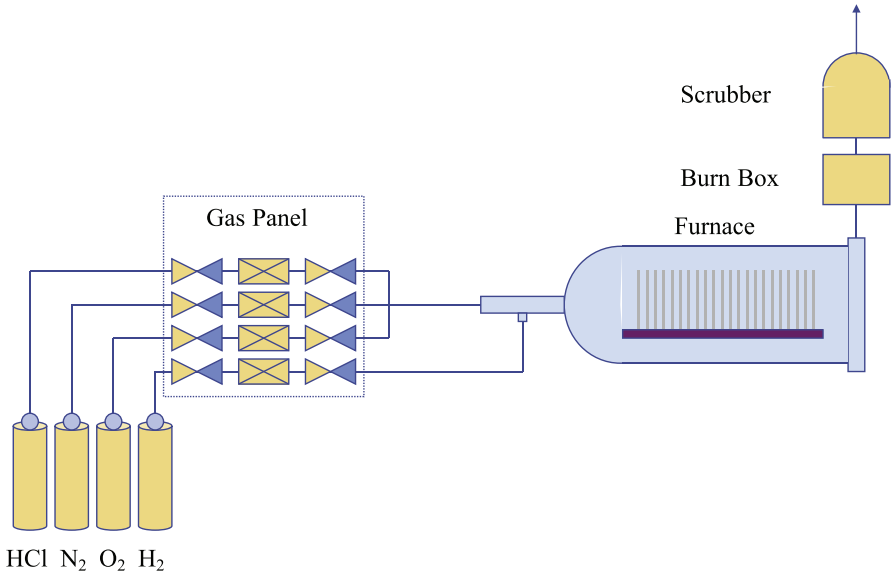

Figure 20. Basic schematic: oxidation.

This diagram shows the basic schematic for an oxidation system. Various gases are routed through a gas panel into the oxidation

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furnace. This allows one to use dry oxygen, hydrochloric acid, and hydrogen in the oxidation environment. One can also use nitrogen to purge the system. The exhaust from the furnace goes through a burn box. The burn box operates at temperatures high enough to oxidize the remaining gases so that they do not present a hazard. The scrubber then removes any toxic chemicals from the environment.

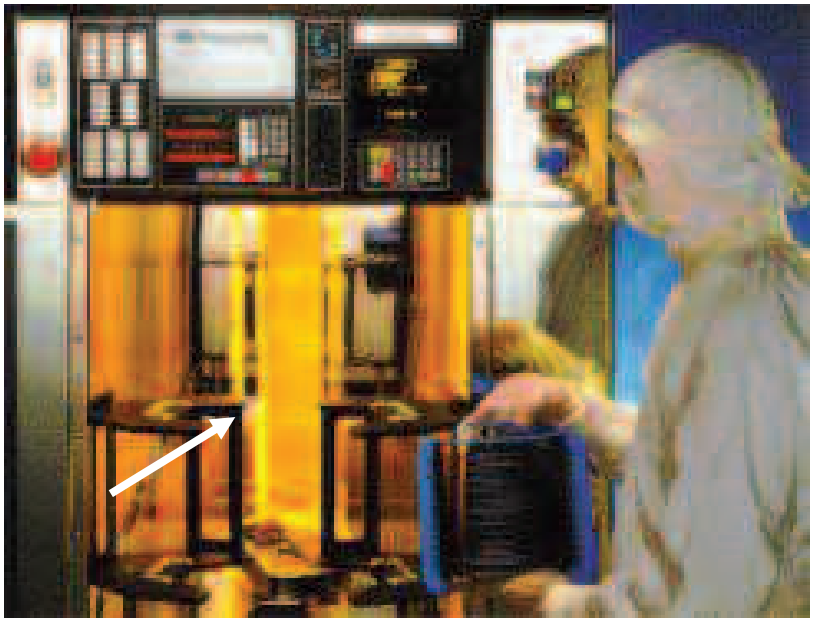


Figure 21. Oxidation furnace.

This picture shows a process technician with a boat of wafers in front of an oxidation furnace. This particular system is a vertical furnace. The furnace tube is indicated by the arrow. The yellowish glow indicates that the system is probably at the oxidation temperature.

Here is the typical process sequence. First, the wafers are cleaned to start with a pristine surface. Next, the cleaned wafers are loaded into a quartz boat. The oxidation furnace is set to idle and purged with dry nitrogen. Dry nitrogen is used to prevent oxidation during idle furnace and the temperature ramp processes. The idle temperature is approximately 850°C. Next, the wafers are pushed into the furnace. The temperature is ramped up at a rate of 10°C per minute to the oxidation temperature and stabilized. Once the temperature has stabilized, the nitrogen gas is replaced with oxygen, steam, or an oxygen/ hydrochloric acid mixture. The oxidation process runs for the specified period of time. Once it is complete, the furnace is purged with nitrogen to quench the oxidation process. The furnace is cooled to room temperature, and the wafer boats are pulled out of the furnace.

There are four types of charge that can affect the behavior of a transistor or parasitic device. They are mobile ion charge, oxide trapped charge, fixed oxide charge, and interface trapped charge. Mobile ion charge—usually a positive ion like sodium or potassium in parts per million concentrations—can cause measurable instabilities in transistors. Oxide trapped charge occurs when silicon-oxygen bonds are broken due to ionizing radiation, plasma etching, or ion implantation. These bonds can normally be repaired by annealing. Fixed oxide charge manifests itself as a sheet of positive charge located within 2 nm of Si/SiO_2 interface. It is attributable to incompletely oxidized silicon atoms that have a net positive

charge. The charge always remains positive. Interface trapped charge is also due to incompletely oxidized silicon. The incompletely oxidized silicon produces a dangling bond. It tends to be very close to the interface. The charge may be positive or negative and may change during device operation.

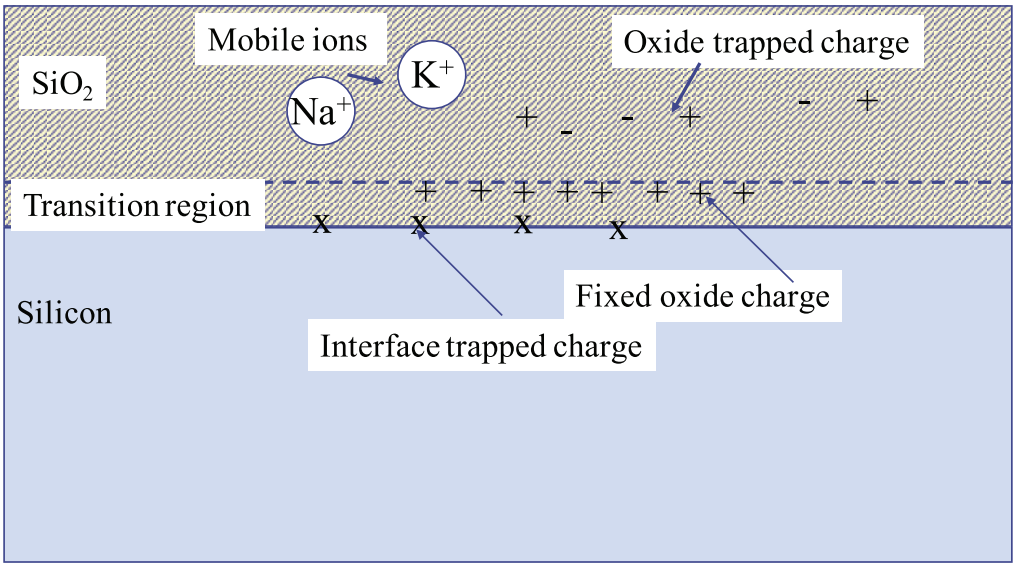


Figure 22. Charges Associated with SiO_2/Si.

This diagram shows the four different types of charge that can occur in the silicon dioxide and at the silicon/silicon dioxide interface. Mobile ions such as sodium and potassium can be found scattered throughout the silicon dioxide layer. In the presence of an electric field however, they can be attracted to the interface. Oxide trapped charge is found randomly throughout the oxide. If there is an excess of either positive or negative fixed charge, it can affect device operation. Fixed oxide charge tends to occur in the transition region between the silicon and the silicon dioxide. Finally, interface trapped charge occurs right at the silicon/silicon dioxide interface.

We are quickly approaching a critical decision point with regard to the use of silicon dioxide as a gate dielectric. With each new technology node, the feature sizes are scaled smaller. This includes physical features such as gate oxide thickness, channel length junction depth, etc. In order to scale these features, the voltage must be scaled as well. However, we are approaching the limit of gate oxide scaling. The tunneling leakage currents are becoming too large for gate oxide thicknesses below 20Å. In addition, the dopants in the polysilicon gate can easily penetrate through the thin gate oxide into the channel below.

There are a variety of techniques used to grow very thin oxides. Some of these techniques involve the classical oxidation process, while others involve depositing an oxide rather than growing it. For thin oxides, one requires shorter times and/or lower temperatures in an oxidation furnace. Another popular method for growing thin oxides is rapid thermal oxidation. This process uses short times and low pressures to achieve a high quality thin oxide. Rapid thermal chemical vapor deposition is a method for depositing an oxide. This is performed at low temperatures with a short cycle time and/or low pressure. Remote plasma enhanced CVD is another deposited oxide. It uses a remote microwave plasma source to introduce precursor radicals such as nitrogen. This process occurs at very low temperatures, at least compared to normal thermal oxidation processes.

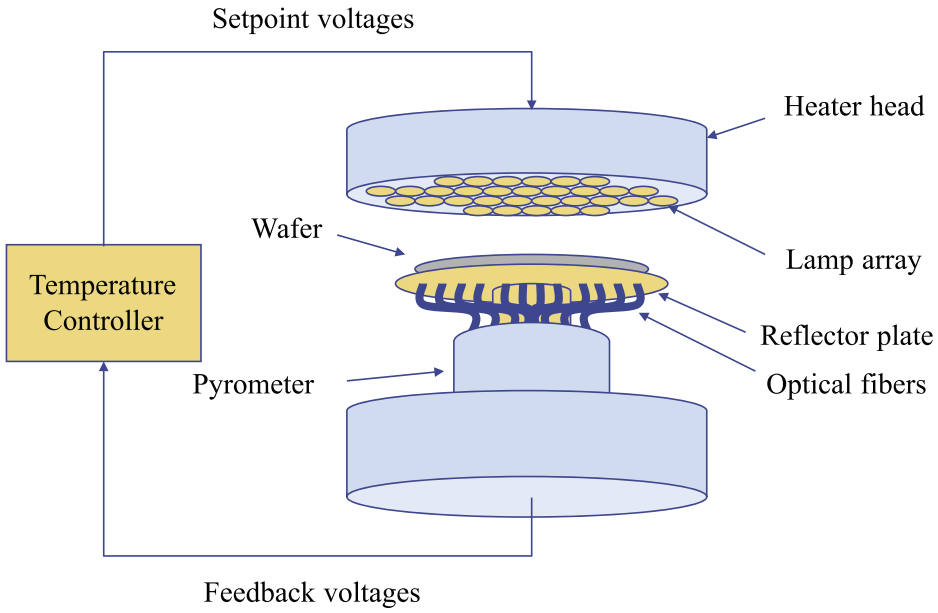


Figure 23. Rapid thermal processing.

Rapid thermal processing is a different approach to the oxidation process. A single wafer is placed under an array of heat lamps. These heat lamps act like an oven, rapidly heating the surface of the wafer. An optical pyrometer is used to determine the temperature of the wafer. The voltage levels from the pyrometer are sent to the temperature controller, which can then adjust the intensity of the heat from the lamps. This configuration allows more rapid heating and cooling of the wafer.

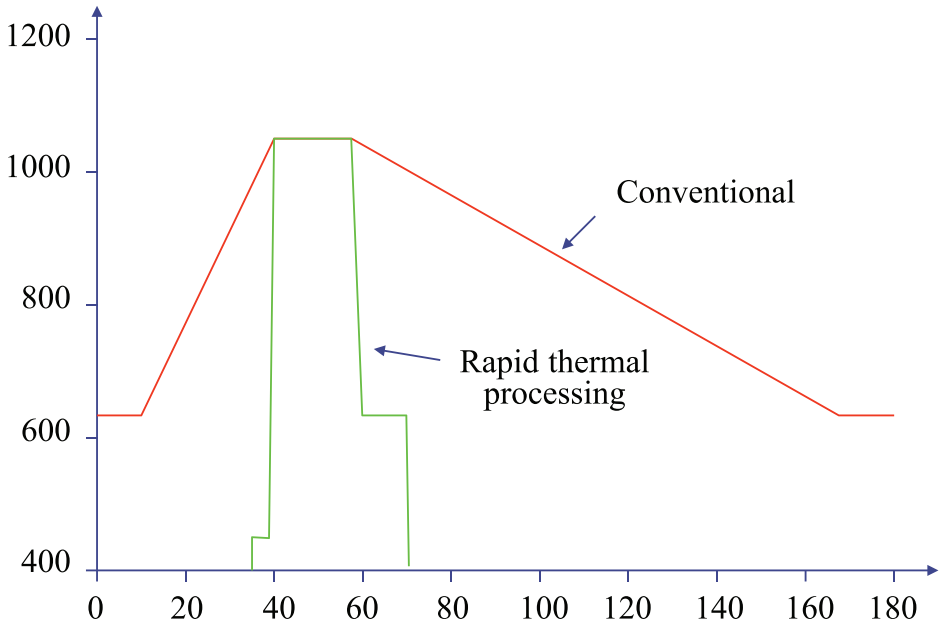


Figure 24. Temperature ramping.

This graph shows the temperature ramp profiles for both a conventional oxidation furnace and a rapid thermal processing system. The conventional ramp is shown in red, and the rapid thermal processing ramp is shown is green. Notice that the rapid thermal processing system starts from a much lower temperature, and quickly ramps up to the oxidation temperature. The main disadvantage of the rapid thermal processing approach is that these systems are designed to handle a single wafer at a time. A conventional wafer oxidation furnace can handle up to 20 wafers in parallel.

Figure 25. RTP production system.

This image shows a rapid thermal processing production system. Notice that the system has two chambers that can operate in parallel. This helps to alleviate the bottleneck associated with this process.

The practical limits for silicon dioxide as a gate dielectric is around 15–20Å. Below this level, leakage currents and dopant penetrations increase the transistor leakage to the point where no further gains can be made in performance. As we approach this limit, researchers are actively investigating other dielectric materials. High dielectric constant materials can potentially extend scaling to thinner equivalent oxide thicknesses. Researchers have investigated three groups of materials: nitrides, oxynitrides, and high dielectric constant materials such as aluminum oxide, zirconium oxide, hafnium oxide, and yttrium oxide. At this point, hafnium oxide is the main candidate that is replacing silicon dioxide at the 45nm node and below. The high-K dielectrics require atomic layer deposition techniques, since they are quite thin and cannot be natively grown on the silicon surface.

In summary, oxidation is a critical process that has enabled the scaling of transistors to the nanometer scale. Bruce Deal and Andrew Grove developed a model that successfully describes the oxidation process; in fact, the model—although almost 40 years old—is still widely used today. Scaling of the silicon dioxide layers for the gate dielectric is becoming a major challenge. At the 45nm node, silicon dioxide is inadequate as a gate dielectric because of leakage. Hafnium oxide, and to a lesser extent, hafnium silicate are the main replacement materials for silicon dioxide.

Technical Tidbit

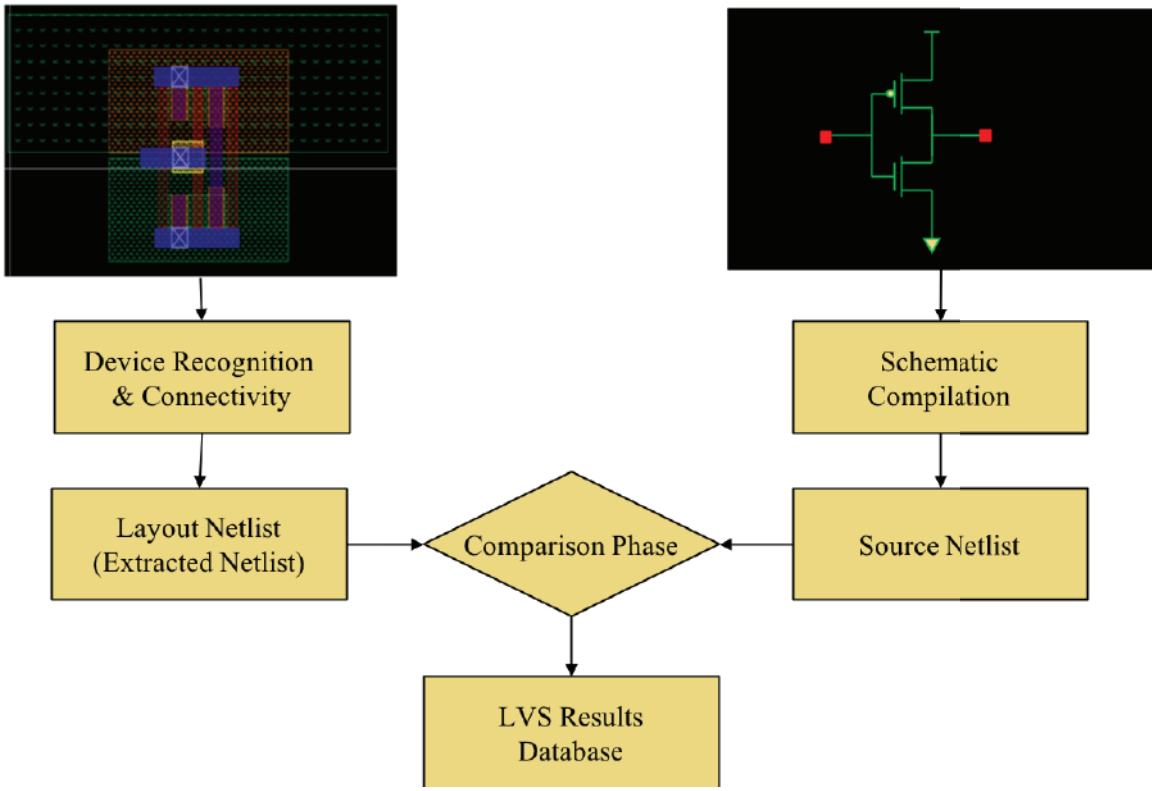
Layout vs. Schematic

In this month's technical tidbit, we'll discuss Layout versus Schematic.

Layout versus schematic (LVS) is a method of verifying that the layout of the design is functionally equivalent to the schematic of the design. A verification EDA tool performs LVS by taking a set of instructional code input, commonly known as LVS rule deck, in the following two steps: extraction and comparison. The LVS rule deck guides the verification tool by providing the instructions and identifying files which are needed for LVS. Design inputs needed for running LVS are as follows:

- Graphical database system (GDS) layout database of the design
- Schematic netlist of the design
- Cell definition file including Intellectual property files and standard cells
- Pad reference file

A LVS rule deck is a set of code, which is written in Standard Verification Rule Format (SVRF) or TCL Verification Format (TVF), which guides the verification tool to extract the devices and connectivity of the integrated circuit. The LVS rule deck contains the layer definitions for the identification of layers used in the layout file and matches description of a layer to the location of the layer in the GDS file. This helps in the recognition of the electrically connected regions in the layout, namely the nets. Nets are recognized from the layout shapes through analysis between layout shapes in layers. LVS rule deck also contains device structure definitions.



The LVS flow is as follows. The verification tool takes the GDS file as input and breaks it down into basic design devices like transistors, diodes, capacitors, resistors etc. These devices are identified in the GDS file by recognition of the layers and shapes that make up the circuit or by the cell definition of the devices/circuits provided in the cell definition file of the intellectual property blocks or in the LVS rule deck itself. It also extracts the connectivity information between these devices from the GDS file. The next step in connectivity extraction is to verify the uniqueness of nets. Each electrical net is given a unique node number for identification during the extraction process. Net names can also be named based upon the presence of layout text objects or text statements in the control file. This device information along with their connectivity is written into a layout netlist file, generally called layout extracted netlist. This process is known as extraction.

In the comparison phase, the verification tool compares the electrical circuits from the schematic netlist and the layout extracted netlist. The netlist comparison process also uses the LVS rule deck. After the successful comparison between layout and source netlist, a one-to-one correspondence between the elements (instances, nets, ports, instance pins) of source netlist and layout netlist is established. The intention of the layout designer is to implement the functionality provided in the schematic into a geometrical representation of layout. Therefore, in order for the verification process to complete without error, both layout and source netlist must match. If the two netlists differ, discrepancies are reported in the form of a LVS result database which can be used to debug LVS issues. The result database would contain the list of incorrect elements and the reason of mismatch like incorrect nets, incorrect ports, and incorrect instances.

Ask the Experts

Q: What is the proper solder fillet height?

A: There is not a single answer, as this depends on the process and the application. For instance, the US Military prohibits the die mounting material from extending onto the top surface or extending vertically above the top surface of the die. Many companies use the same criteria for silver epoxy die attach compounds. However, for many commercial products there are other die attach procedures. For example, die attach films and B-stage would have no fillet, so a fillet height would not apply.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

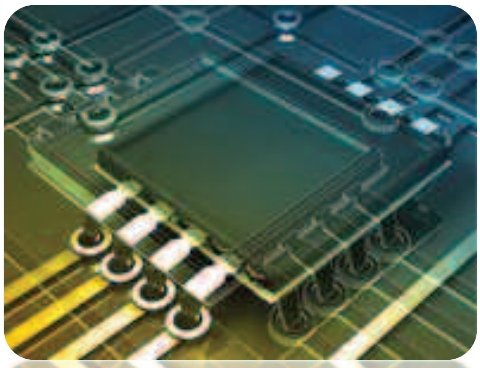
One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

CMOS, BiCMOS and Bipolar Process Integration
September 10 – 12, 2018 (Mon – Wed)
San Jose, California, USA

Wafer Fab Processing
September 17 – 20, 2018 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
October 29 – November 1, 2018 (Mon – Thur)
Singapore

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel