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Lead Free Solders—General Issues Part 2

By Christopher Henderson

The point of failure is a result of the properties of the lead-free solder. Therefore, the stiffness of a lead-free solder reduces transient bend performance.

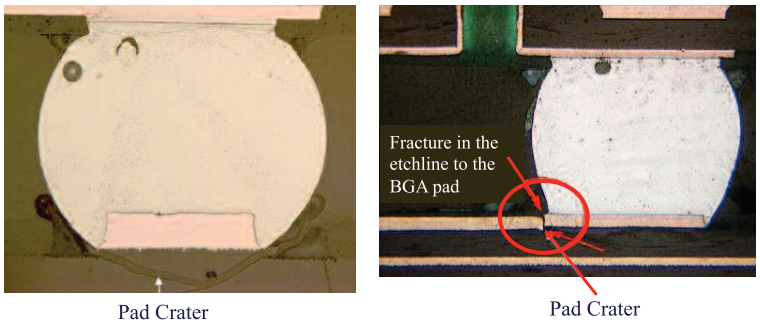


Figure 8. Optical cross-section images showing PCB pad cratering.

The lead-free transition has lowered the printed circuit board materials margin by transferring more solder joint stress into the board and thermally degrading the laminate material. The images in Figure 8 show examples of damage created by this higher stress. Board laminate cracking starting from the edge of the copper pads at pad-laminate interface and propagating under copper pads is referred to as pad craters. Pad craters are primarily caused by mechanical stress or overload condition which may be induced by impact loads and are typically observed near the package corners. The image on the left shows an example of pad cratering. In this case, a portion of

In this Issue:

the substrate has pulled away as evidenced by the gap shown here (indicated by red circle). The image on the right shows a fractured trace on the printed circuit board. In this case the solder joint held, but the stress translated into an adjacent trace which sheared apart. Sometimes these fractures in the printed circuit board occur because the laminate materials thermally degrade from the solder reflow operation.

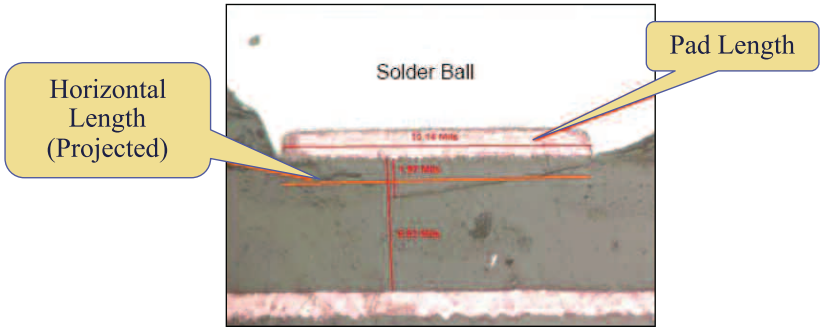
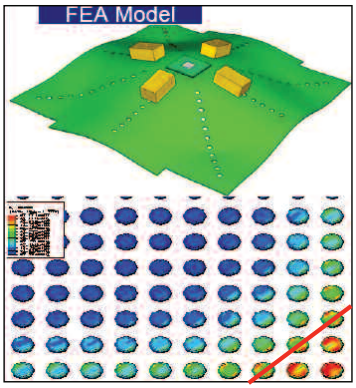


Figure 9. Optical cross-section images showing pad crater characterization.

A major challenge with pad cratering is characterization of the crack (Figure 9). The reason this failure mode needs attention is because these cracks may propagate under copper pads and cause a trace crack at the location where the trace meets that particular pad, or they could provide an opportunity for an electrically conducting path or short within the PCB, among others. Traditional methods involve cross-sectioning the region where the crack has occurred to estimate its horizontal and vertical lengths. This process is both time-consuming and destructive.

A pad crater is defined as the separation of the copper pad from the resin/weave composite or the composite immediately adjacent to the copper pad. These are also known as laminate cracks or pad lifting.



Shock Level	Solder	Crack (%) Row				
		Non CTF		CTF		
		1	2	3	4	5
1	Sn/Pb	50	0	0	0	0
	LF	100	20	0	0	0
2	Sn/Pb	50	50	0	0	0
	LF	100	100	40	0	0
3	Sn/Pb	100	75	0	0	0
	LF	100	100	100	100	100

Figure 10. Shock test performance comparison between Sn/Pb vs. Pb free.

Figure 10 shows a finite element analysis model for an IC package. There are critical-to-function (CTF) pins beginning at row three measured on the diagonal. Notice that near the corner of the device a number of the solder joints exhibit very high stress levels as evidenced by the yellow and red colors. The table on the right shows that a number of the pins in diagonal rows 1 and 2 have a very high percentage of cracks. The number of cracks increases with the shock level test. Also notice that the lead-free solders all exhibit higher percentages. Of particular concern are the cracks on pins in rows 4 and 5. While it may be possible

to place redundant power and ground pins out toward the corners, eventually one must place critical to function pins. The stresses involved with lead-free solders limit the flexibility associated with this practice and reduce the overall shock tolerance of the system.

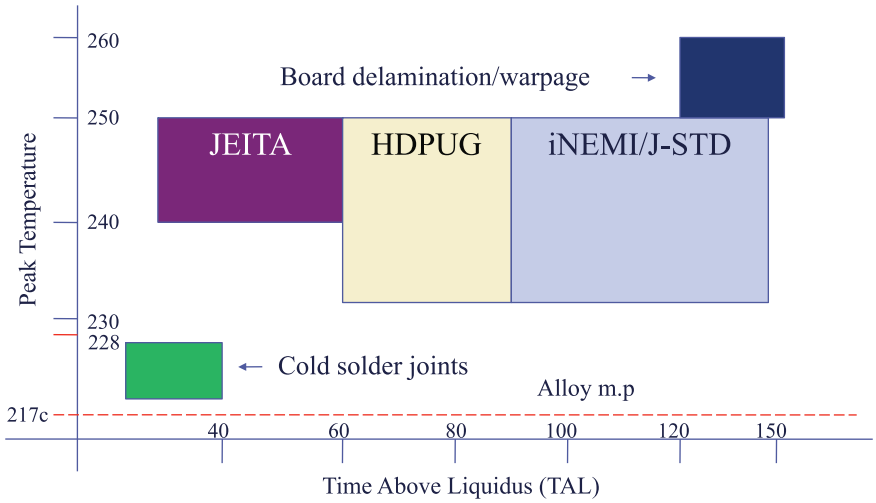


Figure 11. Lead free reflow process window.

The chart in Figure 11 shows the process window associated with lead-free solders. The liquidus temperature of SAC-405 is 217ºC, but to create a reliable solder joint, the temperature must be higher. The three major standards, the Japan Electronics and Information Technology Industries Association (JEITA), the High Density Packaging Users Group (HDPUG), and the International Electronics Manufacturing Initiative (iNEMI) specify a peak temperature of 250ºC. The JEITA standard also specifies a higher minimum peak temperature of 240ºC. The JEITA standard specifies the least amount of time above liquidus temperature, while the HDPUG and iNEMI standards specify longer periods of time. One can see that board delamination and warpage begins at 250ºC and 120 seconds, which is just outside the iNEMI standard. On the other end, lower reflow temperatures and short times can lead to cold solder joints.

The solder fatigue performance is determined by a number of different factors. The first and probably most important factor is the coefficient of thermal expansion mismatch between the component and the board. This factor determines the total amount of strain that will be induced in the system given a particular solder reflow temperature. The second factor is the load on the solder joint. Each solder joint has to carry a particular load in terms of weight and initial stress. Other factors that are important include the pad size on both the component and the board, the pad size ratio, the package and die size, the package rigidity and thickness, and the ball array pattern board thickness and rigidity. Another important factor is the component type. And finally, as we have been discussing, the metallurgy or solder system is important.

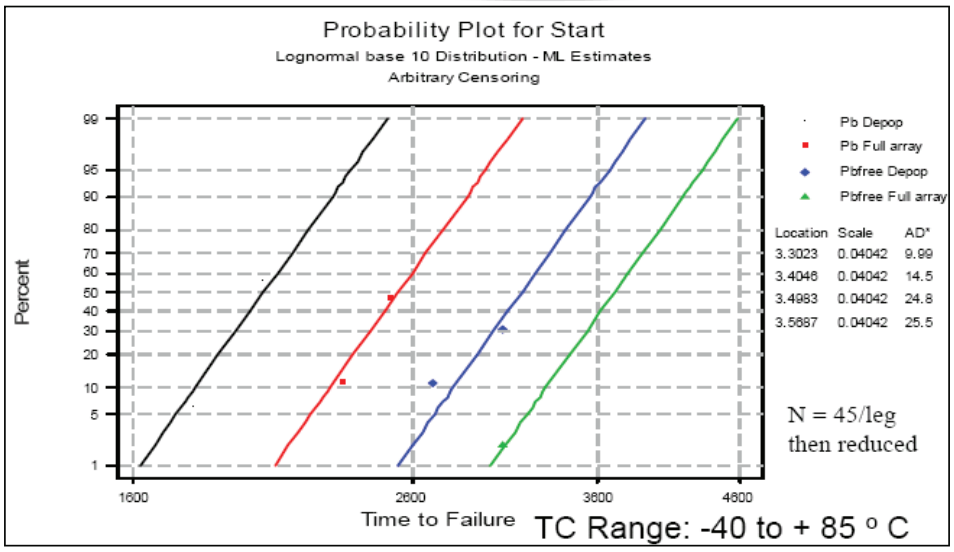


Figure 12. Cumulative Probability Plot showing Time-to-Failure for different solder alloys.

The data on this graph in Figure 12 show results of lead-free vs. leaded solder on 1mm flip chip ball grid array packages using both full arrays and depopulated arrays of solder bumps. The chips did not use heat sinks, and the printed circuit boards used an immersion silver process. The samples were temperature cycled from minus 40 to plus 85ºC. Notice that the lead-free solder samples exhibit better time-to-failure performance than the leaded samples by greater than 40 percent. Notice also that the full array ball performance exceeds the depopulated array performance. This occurs due to the fact that the full array spreads the stress more uniformly between the balls and limits excessive stress on individual balls.

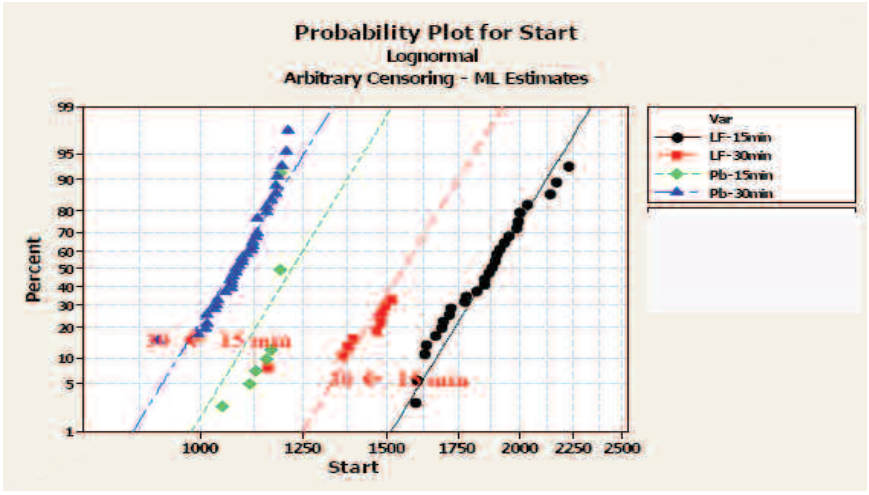


Figure 13. Effect of dwell time on temp cycle performance.

A shorter dwell time helps to improve performance as well. In the graph in Figure 13 notice that the time-to-failure for samples subjected to a 30-minute dwell time failed more quickly than the 15-minute dwell time samples. Again, the lead-free samples fared better than the leaded samples.

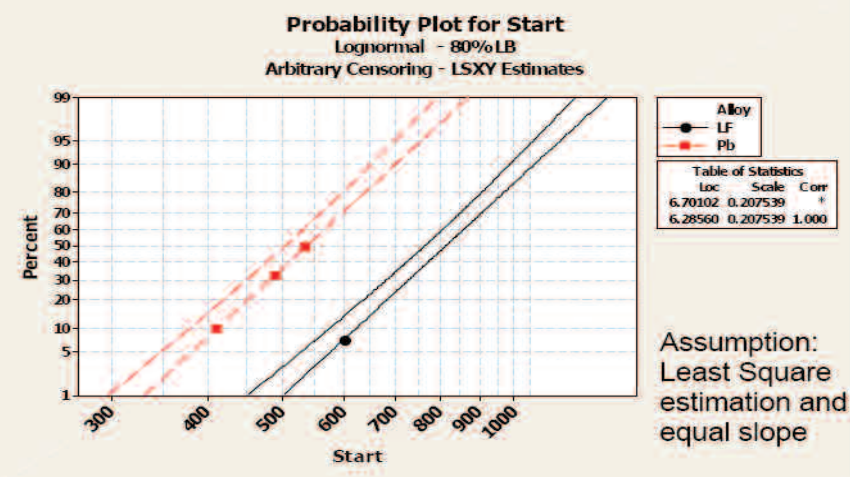


Figure 14. Temp cycle results for PbSn and lead-free solder.

The graph in Figure 14 shows temperature cycling results for both lead-free and leaded solder components on sample boards. In this case, the cycle time was quite long—on the order of 8 hours. The lead-free samples survived approximately 60 percent longer than the leaded samples.

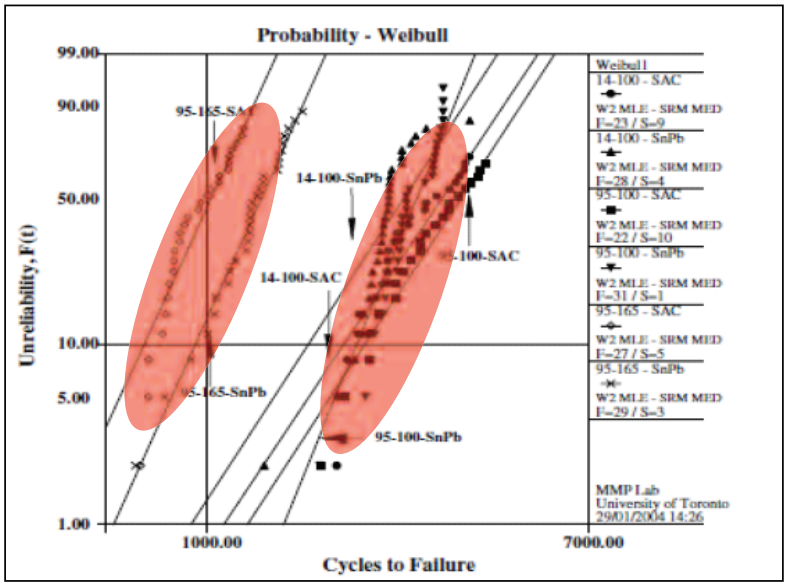


Figure 15. Effect of temperature on solder fatigue.

The graph in Figure 15 shows the effect of different temperatures on solder fatigue. Notice that the when the upper temperature limit in the cycle is limited to 100 degrees, the lead-free and leaded solders behave similarly. However, when the upper temperature is 165 degrees, the lead-free solder performs worse. Poor performance at higher temperatures is not necessarily a problem; it depends on the application. For example, a data center is not subject to the temperature extremes modeled here. On the other hand, an automotive application might require withstanding high temperatures such as these. Currently, there is no common methodology for reliability assessment. Variables such as temperature, dwell time, and ramp rates need to be standardized to allow accurate comparisons.

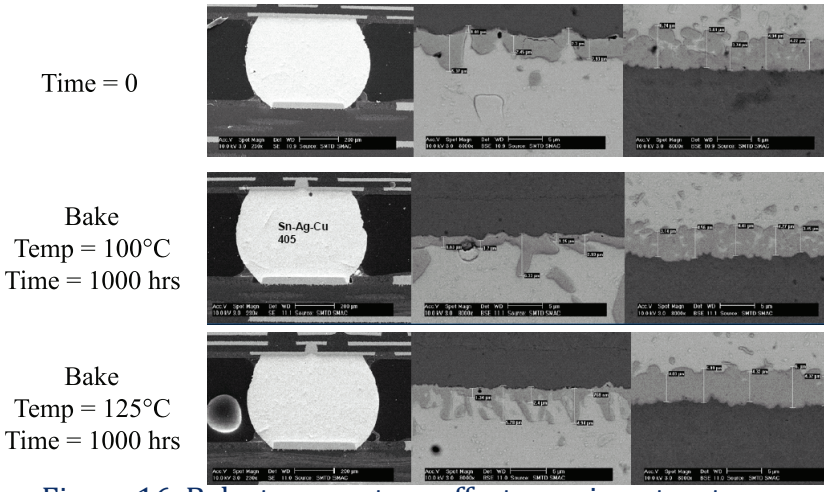


Figure 16. Bake temperature effect on microstructure.

Let's now look at the change in microstructure that can possibly occur with aging. In general, higher temperatures allow diffusion processes to move material within the solder alloy. Does this indeed occur in lead-free alloys under use conditions? The answer is no for most use conditions. These images in Figure 16 show cross-sections of SAC-405 solder balls at zero time, and after 1,000 hours of bake time at 100 and 125ºC. In each of the images there is no evidence of intermetallic growth or voiding. This indicates that silver-tin-copper lead-free solders behave well under elevated operating temperatures.

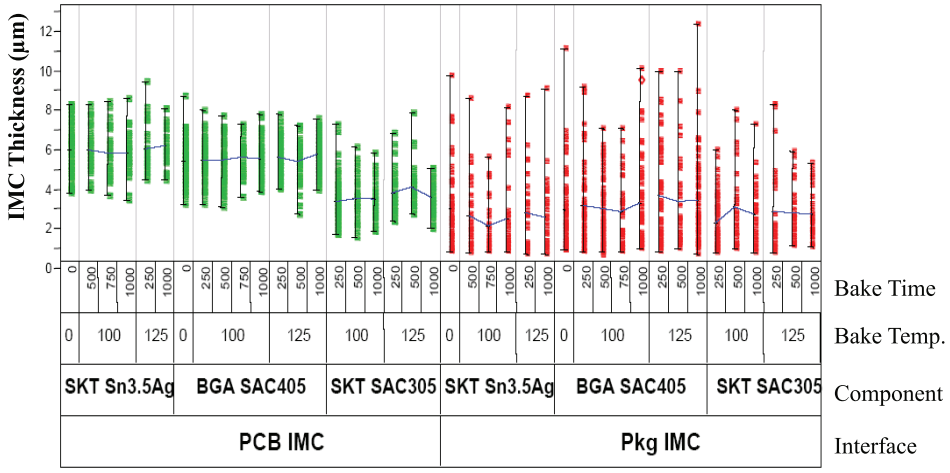


Figure 17. Bake temperature effect on IMC thickness.

Figure 17 shows additional data related to intermetallic growth and baking. In this chart, we evaluate intermetallic growth at the package pad and printed circuit board pads for three lead-free solders at different times under two different temperature stresses. Notice that there is not significant change between the initial conditions and the after-bake conditions.

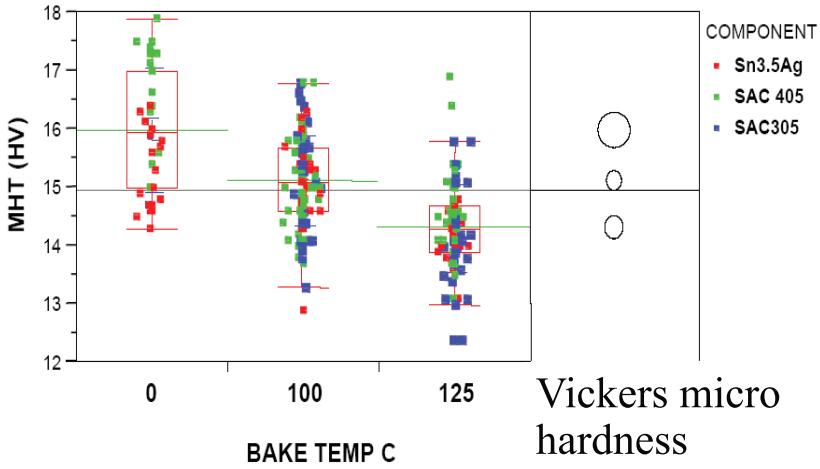


Figure 18. Bake temperature effect on solder properties.

Exposure to high temperatures can alter the properties of the solder. One important property that changes is hardness. The graph in Figure 18 shows the effect of bake temperature on the Vickers micro hardness scale. Notice that for the three lead-free solders shown in the graph, the micro hardness decreases as the bake temperature increases.

Technical Tidbit

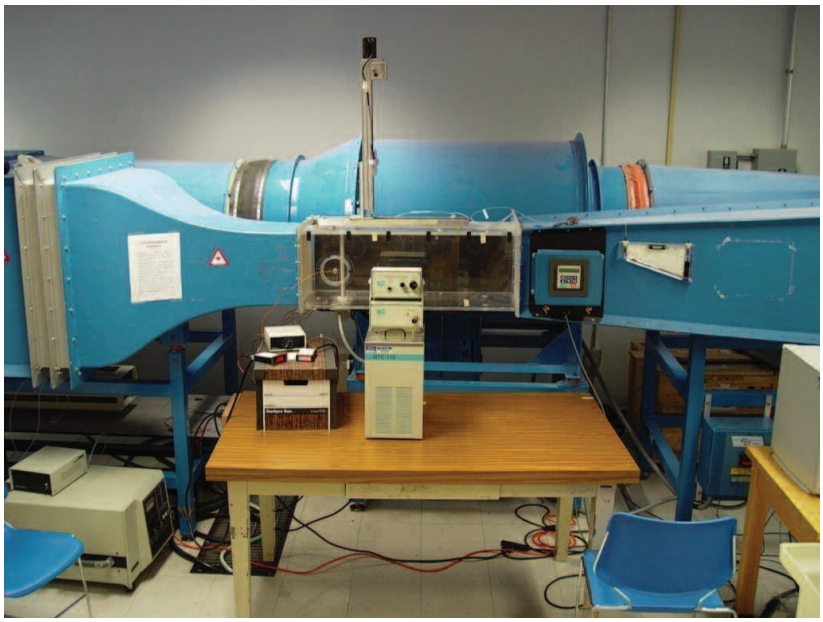
Thermal Resistance Measurements

In this technical tidbit, we will introduce the topic of θ_{JA}, or thermal resistance, junction-to-ambient. This is an important parameter for components that operate at moderate to high power levels.

Engineers report θ_{JA} with two parameters, depending on the board type they use. These parameters are R_{JA} for still air and R_{JMA} for a moving air environment. These values help bound the thermal performance of the package in the customer's application.

Let's address θ_{JA} in a still air environment. R_{JA} measures the thermal performance of the package on a low conductivity test board, like a 1S configuration, in a natural convection environment. 1S refers to a board with one signal layer and no copper planes for cooling. That is, an environment with no cooling or fans. We design the best board per JEDEC 51-3 and 51-5. R_{JA} helps the engineer to estimate the thermal performance of the package when it's mounted in two distinct configurations. The first configuration is a board with no internal thermal planes, like the 1S board. The second configuration is when we use a multi-layer board that is tightly populated with similar components.

Next, let's discuss θ_{JMA}, or θ_{JA} in a moving air environment. In this configuration, we assume a higher power dissipation level that will require a board with two signal layers and two internal planes to help dissipate the increased power. Engineers design the high conductivity 2S2P boards using the JEDEC 51-5 and 51-7 standards. 2S2P boards refer to boards with two signal layers and 2 internal copper planes for cooling. R_{JMA} provides the thermal performance when there are no nearby components that are dissipating significant amounts of heat on a multi-layer board. We just assume one very hot component, for example, an LED package.



This is a typical setup for the moving air environment. It is in essence a wind tunnel, where we can pass a varying degree of airflow past the board to help cool it.

Ask the Experts

Q: I have often observed that for a mosfet in saturation, Vdsat is lower than Vgs-Vth. Upon reading some answers over the web , experts have said that this is due to velocity saturation. I want to understand in more detail how velocity saturation defines Vdsat of a transistor which is simply the min Vds required for the transistor to be in saturation region?

A: Yes, velocity saturation is the most important factor to consider. The main thing to understand is the fact that the electric field across the transistor is highest in the off-state, and lowest in the on-state. So as the transistor goes from the off-state, through saturation, to the on-state, the electric field will be the highest right as the device enters saturation. Therefore, velocity saturation will be at its peak just as the transistor enters saturation, and will have the largest impact on the value of Vdsat and promoting the standard.

Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

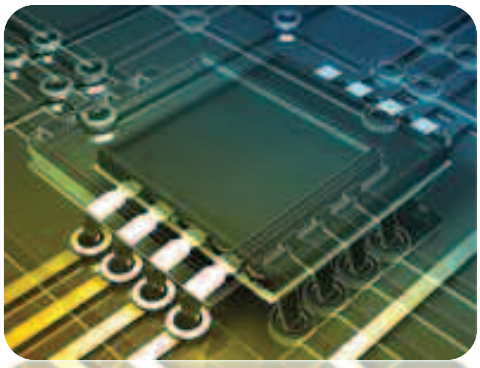
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

ISTFA/2017

International Symposium for Testing and Failure Analysis

November 5-9, 2017
Pasadena Convention Center
Pasadena, CA, USA

Registration is available at
https://register.rcsreg.com/r2/istfa2017/ga/top.html



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Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
September 11 – 14, 2017 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
September 18 – 21, 2017 (Mon – Thur)
Portland, Oregon, USA

IC Packaging Design and Modeling
September 25 – 26, 2017 (Mon – Tue)
Dallas, Texas, USA

IC Packaging Technology
September 27 – 28, 2017 (Wed – Thur)
Dallas, Texas, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany