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CMP – Applications and Issues Part 3

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This is the third and final part in a series on Chemical Mechanical Polishing (CMP) applications and issues.

An important aspect of CMP is end point detection. We typically want to thin a layer or flatten a layer to an exact value. The first case would involve global planarization. The goal would be to polish a film to a particular flatness or stop at a desired remaining film thickness. This is typically the case with dielectric layers. An in-situ optical metrology measurement like ellipsometry is not practical since one cannot consistently locate the same spot of the rotating wafer and there is interference from the underlying films. For these situations, engineers will use a timed polish, which is a form of end point detection. The system calculates the time and feeds forward the time based on pre- and post-polish thickness measurements. By taking data from multiple wafers, one can begin to determine trends and project final thickness values.

The second case would be for local planarization. For example, plug formation falls into this category. The goal here is to remove all of the film except for the material in the recessed regions, like a multilayer metal film. An example might be copper with a tantalum nitride barrier layer. There are four common in-situ real-time monitoring techniques. The first is laser interferometry. Here we mount a laser and detector on a table. We beam the laser through a clear window in the polishing pad onto the wafer and measure and ana-

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lyze the reflected light. We show a typical reflectance curve for the copper-tantalum nitride film below.

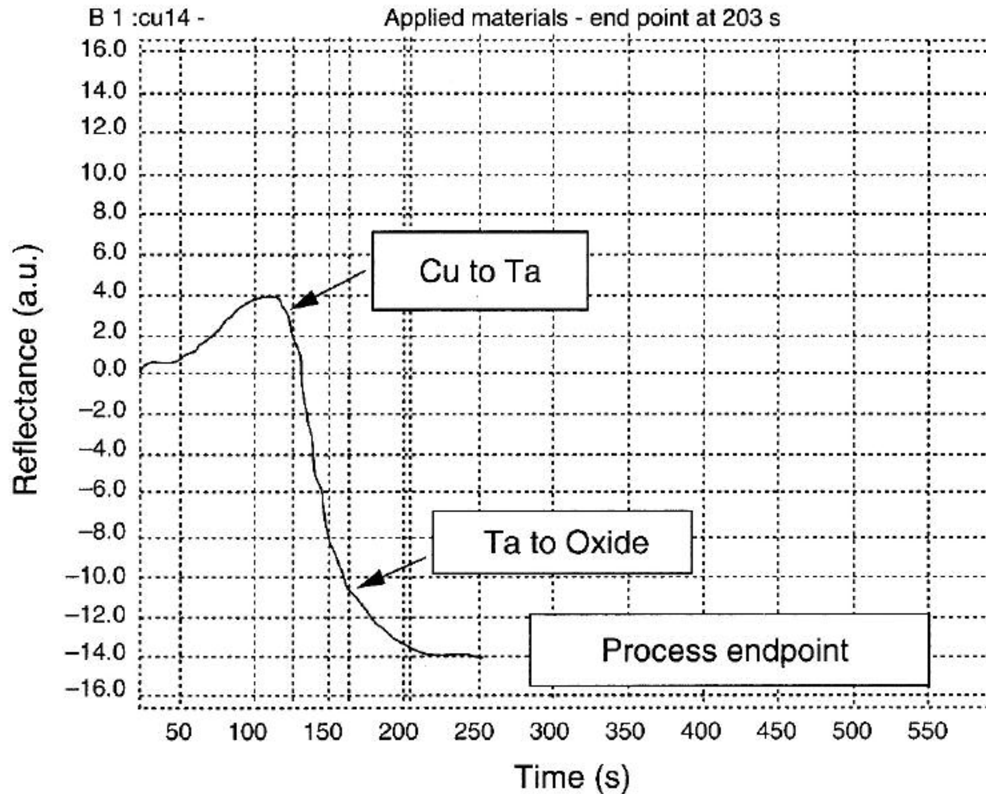


Figure 1. Typical reflectance curve for polishing Cu/Ta/oxide film (from Doering and Nishi).

The next technique is spectrometer reflectivity. Here, engineers measure and analyze reflected light from multiple wavelengths, which can provide a more accurate assessment. The third technique is optical interferometry. In this approach engineers illuminate the wafer backside with infrared light and analyze the light reflected from the frontside. The final technique involves monitoring the motor current. Engineers will sometimes use this method when polishing a film down to a stop layer. An example might be polishing a low-k dielectric layer to an etch stop, like SiCOH. The Hall probe detects changes in the friction as one layer ends and the other begins.

There are several factors related to topography on the circuit that can cause problems. One is local plug dishing. This occurs when via materials are softer than the surrounding oxide. The overlying metal layer may not make good contact to the recessed vias, resulting in poor electrical connection. Aggressive chemical mechanical polishing slurries can also produce a phenomenon known as key-holing. Key-holing occurs when the center of the via opens. Large areas of oxide with little in the way of metallization or vias can lead to a condition known as oxide erosion or dishing. The soft oxide layers polish away more rapidly than regions covered with metal. Particulate in the pads or in the slurry can scratch the surface, leaving marks. These scratches can interfere with subsequent processing.

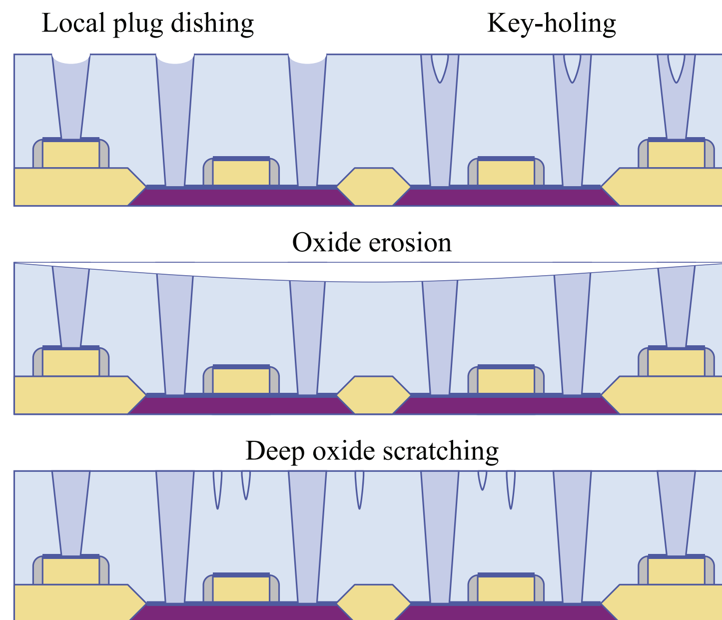


Figure 2. Process factors related to patterns on an IC.

Process control is a tough requirement for CMP. Here are some other issues that affect CMP. The degree of planarity is a common issue. With CMP the removal rates may show significant variability. For example, larger or densely packed features will polish more slowly than sparely populated features. This necessitates multiple measurements. Engineers will use surface profilometry or AFM to do this work. Another common issue is film thickness. This can be measured with ellipsometer or reflectometer. Defectivity is also a prominent concern. This includes foreign material like slurry residues and particles, and voids like microscratches, dishing, and coring. One can map and quantify these defects with a laser particle scanner. However, effective monitoring is challenging due to grain noise from polycrystalline metal films under the oxide, pattern noise from metals under oxide, and film thickness variations.

In Figure 3 we show some examples of the various defects that accompany CMP operations. These include dishing, rip-out, unfilled and filled microscratches, residual slurry material, surface particles, tungsten plug coring, residual tungsten, and recessed plugs. There are certainly others, but these are among the more common.

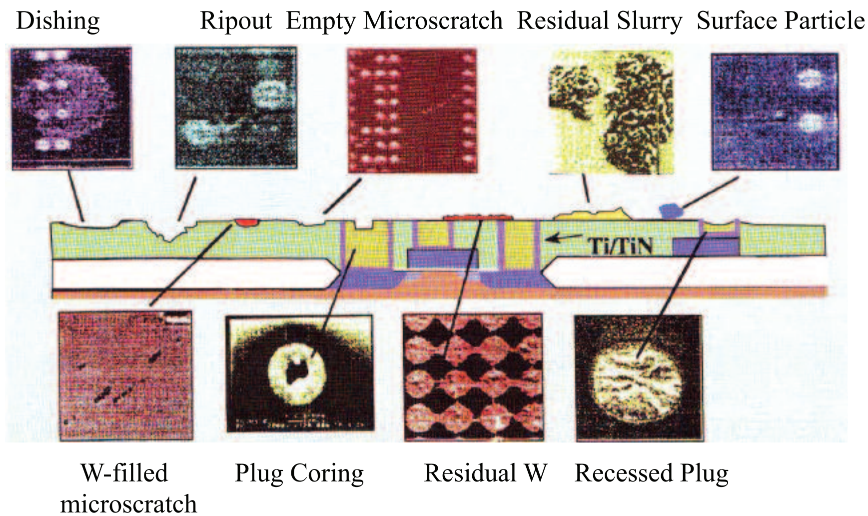


Figure 3. Examples of defects that arise during the tungsten-CMP process (courtesy KLA-Tencor).

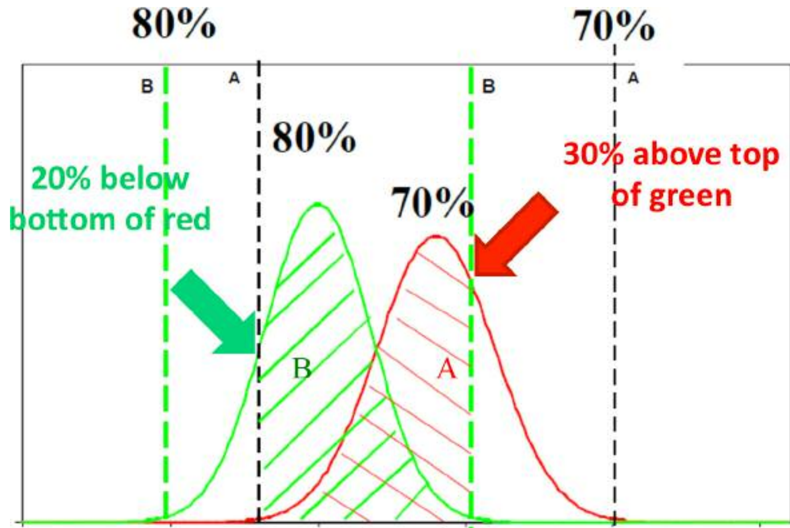
In addition to differences in specific materials, there are other concerns with CMP The polish changes with pattern. The pattern size and density alter the process. Each new reticle set requires that the CMP times and pressures be altered slightly. This is not an acceptable solution for a fabrication line. In order to get around this problem, one may need dummy structures to help make the polishing rate more uniform and protect critical structures from being over-polished. One may also have to trade-off a good polish on a single die to get an acceptable polish across the entire wafer. Since CMP is still a relatively new field, the body of knowledge about how the CMP actually works is still developing. Researchers have discovered that de-ionized water and a pad can work just as well as a pad and slurry system. There is some movement towards using DI water and a pad. This eliminates having to use chemicals; it also creates a process that does not generate near the particulate contamination of a slurry-based process.

The forces placed on the wafer by the CMP process may tear pieces of metal interconnect out of the pattern, rendering the circuit non-functional. A more difficult aspect of this problem is controlling tear out of tungsten or other materials. Big particles in the slurry can create big scratch marks in the die. This also means that the pads must not generate particles, and that the slurries themselves must be highly uniform. Slurry consistency and continued availability is also an issue. Many of the companies that provide slurries are small companies. This area of the industry is still undergoing restructuring. Waste treatment and disposal is also an issue. Some of the waste materials are classified as toxic, and require special disposal procedures. Finally, the cost of ownership of CMP is important. Because CMP is a dirty process, it requires expensive equipment that must be serviced frequently. CMP also uses large amounts of de-ionized water and polishing materials. While the copper dual-damascene process removes some of these CMP steps, it is still an expensive proposition.

Technical Tidbit

Dealing with Sameness in Yield Analysis

Occasionally, one might be asked to compare two distributions. One parameter to help compare distributions is “sameness.” Engineers determine sameness by calculating the overlap area between two distributions. This can help identify how similar two distributions might be in terms of mean and variation. This method is applicable to normal distributions, and is sample size independent. Here we show a plot with two different distributions (see below). The letter A denotes the ±3σ value for distribution A (in red) and the letter B denotes the ±3σ value for distribution B (in green). The sameness value for Distribution A is not equal to the sameness value for Distribution B.



One can use Excel to calculate sameness. The formula for doing this is:

= (NORMDIST(BM+3*BS,CM,CS,TRUE)-NORMDIST(BM-*BS,CM,CS,TRUE))/99.7%

where BM is the baseline mean, BS is the baseline standard deviation, CM is the comparison distribution mean, and CS is the comparison distribution standard deviation. In this example, 80% of Distribution B is between the lower limit of A and upper limit of B, so 20% of Distribution B is below bottom of the lower limit of A. 70% of Distribution A is between the lower limit of A and the upper limit of B, so 30% of Distribution A is above the upper limit of B.

Ask the Experts

Q: What are some factors that affect the activation energy of TDDB?

A: The answer to this question has much to do with the processing conditions for the gate dielectric. For example, activation energy plays a bigger role when the dielectric layer is thicker. When the layer is thicker, the thermal energy imparted to the bonds in the dielectric are more significant. This is reflected in models like the Thermochemical E model. When the gate dielectric is ultrathin, the bonds in the dielectric are fairly few in number, so other factors play a bigger role, like the ionization and movement of atoms in the electric field. Temperature can still play a role, but it is a more minor role. TDDB for BEOL dielectrics is somewhat different. Here, the movement is more related to the drift of copper atoms along interfaces in the dielectric. This behavior is temperature-dependent, so there is an activation energy for this process.

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

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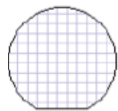

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Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a one-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. high-k gate and capacitor dielectrics
    c. metal gates
    d. SOI
    e. strained silicon
    f. plasma doping

For each of these modules, the following topics will be addressed:

1 fundamentals necessary for a basic understanding of the technique
2 its role(s) and importance in contemporary wafer fab processes
3 type of equipment used
4 challenges
5 trends

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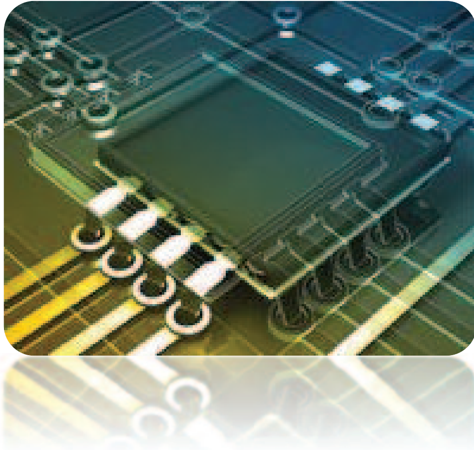

Upcoming Courses

(Click on each item for details)

EOS, ESD and How to Differentiate
September 17 – 18, 2013 (Tue – Wed)
San Jose, California, USA

Wafer Fab Processing
November 7, 2013 (Thur)
San Jose, California, USA

Advanced Thermal Management and Packaging Materials
November 19 – 20, 2013 (Tue – Wed)
Philadelphia, Pennsylviania, USA

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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