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YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In this month's Feature Article, we will continue our discussion of Cleanroom Technology. This Article covers a number of the components of Automated Material Handling Systems.

A key item in the overhead transport scheme is the Overhead Hoist Transport, or OHT. An OHT is an automated transport unit that travels on the overhead track and "directly" accesses the load port of the stocker or process equipment by the belt driven hoisting mechanism. This is widely recognized as the main transport system for 300mm cleanrooms, and is currently used, not only for intra-bay transport, but also factory wide transport. In Figure 1 on the left, we show an image of the OHT, carrying a Front Opening Unified Pod, or FOUP. In Figure 1 on the right, we show an image of a portion of the overhead transport system, with a couple of OHTs visible in the image.

WHAT'S INSIDE?

Want to take control of your learning? See page 07

Upcoming Courses:

- Advanced CMOS/FinFET Fabrication
- Failure and Yield Analysis

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Figure 1- (Left) Overhead Transport (OHT) with FOUP, and (Right) portion of Overhead Transport system with two OHT units visible. Images courtesy Murata Machinery, Ltd.

Another item that is sometimes used in the AMHS is the Overhead Shuttle, or OHS. An OHS is an automated overhead transport system where the transport vehicle travels on the overhead track to transport a carrier. These systems are mainly used for transporting carriers between allocated storage facilities, such as stockers at manufacturing process units for coating and cleaning. The OHS sometimes goes by the name "inter-bay transport system".

Figure 2- Overhead Shuttle (OHS). Image courtesy Murata Machinery, Ltd.

The next item that is sometimes used in conjunction with an AMHS is an Automated Guided Vehicle, or AGV. The AGV is an automated transport system equipped with an industrial robot arm known as a SCARA. SCARA is an acronym that stands for Selective Compliance Assembly Robot Arm or Selective Compliance Articulated Robot Arm. The AGV travels on the floor to "directly" access wafer FOUP stock systems and process equipment. The vehicles can travel in flexible and complex routes through a high-accuracy navigation system to transport carriers to the process equipment. The robotic arm can then move the FOUP from the vehicle to the processing tool, or vice versa. AGVs are also sometimes used in assembly test facilities for transport of wafer lots. We show a photograph of an AGV in Figure 3.

Figure 3- Automated Guided Vehicle (AGV). Image courtesy Murata Machinery, Ltd.

A Carrier Stocker is yet another item that is sometimes used in conjunction with an AMHS. A Carrier Stocker is basically a temporary set of storage shelves in the cleanroom that are intended to absorb variability in timing between the process completion on the current tool and the start of processing on the next tool. Companies like Murata and PRI Automation can provide a wide range of storage solutions to meet cleanroom needs, like stockers for storing wafer carriers. A Carrier Stocker typically combines high-speed vertical transport with storage of Wafers-In-Process between multiple floors in the system. By moving stored Wafers-In -Process between floors, a typical stocker can reduce the cleanroom Wafers-In-Process storage footprint as much as 75% by minimizing the number of stockers required on the production floor. This gives manufacturers greater flexibility in creating the manufacturing environment they need to remain competitive. These systems can also be used to connect multiple production floors together to create a single, integrated manufacturing environment with greater flexibility in routing Wafers-In-Process. Manufacturers can use the freed-up floorspace to reduce the size of the cleanroom or add more process tools to increase manufacturing capacity. Carrier Stocker systems can be used not only for FOUPs, but also for Reticle Storage Pods, or RSPs. Figure 4 shows an example of a Carrier Stocker.

Figure 4- Carrier Stocker. Image courtesy Murata Machinery, Ltd.

Sometimes timing variability can be best addressed at a particular process tool. In this situation, one can use a Tool Front FOUP Buffer. We show an image of a Tool Front FOUP Buffer in Figure 5. It is typically used to hold wafer lots near the next processing step to avoid logistics issues due to backups that might occur if the lots were to be held by the Overhead Transport. Implemented as buffer equipment to be set up at the load port of the process equipment, the Tool Front FOUP Buffer can be set up on either a new or existing production line where the equipment complies with the E15.1 SEMI Standard. FOUPs can be buffered at the nearest position to the process equipment. Additionally, by setting up independent transfer units at each process tool, it is possible to reduce the FOUP replacement time between the FOUP removal after the process completion and the FOUP supply to the next process, enabling improvement in the operational efficiency of the inspection equipment which typically only requires a short time for inspection.

Figure 5- Tool Front FOUP Buffer. Image courtesy Murata Machinery, Ltd.

In next month's Feature Article, we will conclude our discussion of Automated Material Handling Systems.

Technical Tidbit: Highly Accelerated Life Test (HALT)

In this month's Technical Tidbit, we will discuss the Highly Accelerated Life Test, or HALT. HALT is a testing method designed to help improve product reliability. HALT is primarily used at the Board or System Level, but even for semiconductor product and reliability engineers, it is worth understanding the test, since semiconductor components mounted to these boards or in these systems must pass the stresses associated with the test. The principal idea of HALT is to find design weaknesses as quickly as possible and then fix them. After improving one weakness, the next design weakness is found and improved, and so on, until no design weaknesses remain that could result in field failures. During HALT, a product is stressed beyond the product specification to quickly accelerate and identify design weaknesses. It is important to understand that HALT is not a pass/fail test. The idea is to produce failures, so that we can analyze them and then take corrective action to improve the product.

The main standards governing HALT are IPC 9592 and IEST-RP-PR-003. IPC is a trade association whose aim is to standardize the assembly and production requirements of electronic equipment and assemblies. IPC is known globally for its standards, and publishes the most widely used acceptability standards in the electronics industry. The Institute of Environmental Sciences and Technology (IEST) is a non-profit, technical society where professionals who work with controlled environments can connect, gain knowledge, receive advice, and work together to create industry best practices. The organization uniquely serves environmental test engineers, qualification engineers, cleanroom professionals, those who work in product testing and evaluation, and others who work across a variety of industries.

IPC-9592 covers requirements for power conversion devices for the computer and telecommunications industries. Within IPC 9592, there are several sections that cover HALT-related testing. They are listed in Table 1 below.

IPC-9592 Standards			
Design for Reliability	Design and Qualification Testing	Quality Processes	Manufacturing Conformance Testing
Specifying, designing and documenting performance and reliability	Performance to specification, performance in intended environment EST, HALT	Quality Management Systems, Supplier and Sub-Tier Quality Requirements	Burn-In, ORT, HASS, HASA

Table 1- IPC 9592 Standards Sections that apply to HALT.

IEST-RP-PR-003 is a Recommended Practices document that describes the best approaches to performing HALT. This document covers items such as:

- Temperature Humidity Bias (THB)
- High Temperature Operating Bias (HTOB)
- Temperature Cycling (TC)
- Power and Temperature Cycling (PTC)
- Shock and Vibration (S&V)

These items are typically included, either in part or in total, to a HALT plan.

The goal of HALT is to expand the margins between the specification and actual limits. This creates a more robust product, which is important for high-reliability and safety-critical applications, like one might encounter in an automotive, defense, or space environment.

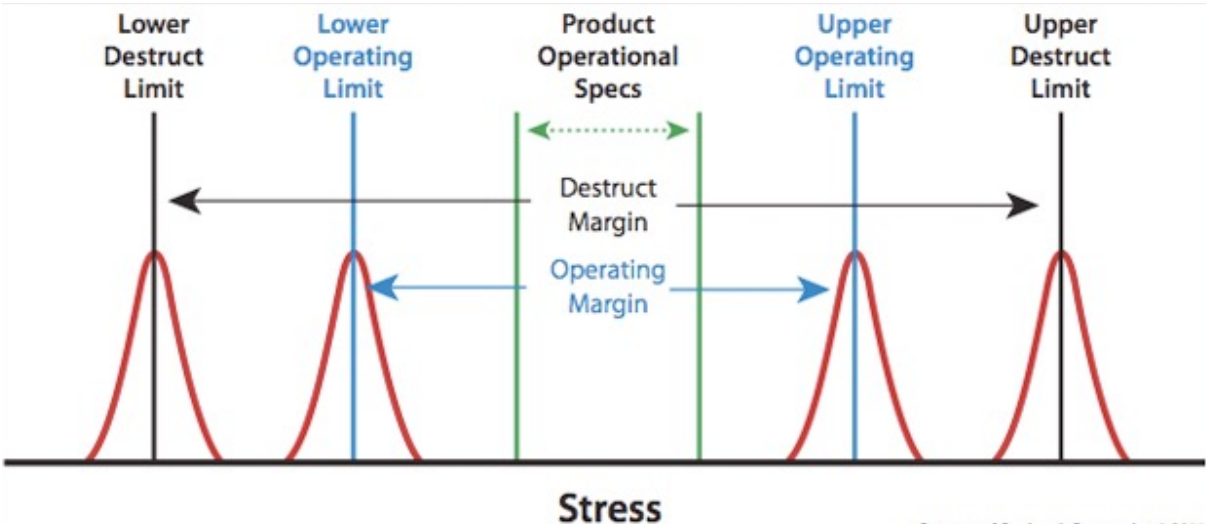


Figure 2- Diagram illustrating the goal of HALT. Diagram courtesy Qualmark Corporation.

If you are interested in further information on this topic, contact us at Semitracks, Inc. at info@semitracks.com.

Ask The Experts

Q: For a new ASIC, we want to define the sample size needed for an ELFR measurement. The target DPPM Level is 10000 DPPM (1%). We looked at the JEDEC Standards and found information which to us sounds contradictory:
JESD47: There is a table (Table 4 on page 11) which tells us that we need 100 units to demonstrate a level of 9163 DPPM at 60% confidence.
JESD74: Here the calculation methods for the ELFR are described, but in this document the acceleration factors are taken into account, while in Table 4 in JESD47, the calculation seems to be independent of any acceleration. If we follow the calculation in JESD74, we would end up with a much lower sample size, since our stress test creates a big acceleration factor.

Our questions are:
1. Why do we get contradicting results if we look at these two JEDEC standards?
2. What is your recommendation for the sample size in our case?

A: Here are my responses on your questions:

1. Why do we get contradicting results if we look at these two JEDEC standards? You get contradicting results because JESD47 does not take into account acceleration factors, whereas JESD74 does use acceleration factors, as you mention in your question. It is almost always appropriate to use JESD74, if you plan to run the ELFR test with the higher temperature and/or voltage level, as compared to the normal operating temperature and voltage level.

2. What is your recommendation for the sample size in our case? I would use the calculation from JESD74 to determine the sample size, again, if you plan to run the ELFR test with the higher temperature and/or voltage level, as compared to the normal operating temperature and voltage level.

Course Spotlight: SEMICONDUCTOR RELIABILITY AND PRODUCT QUALIFICATION

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms, and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability; assessing the impact of new materials; dealing with limited margins, and other factors. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. ***Semiconductor Reliability and Product Qualification*** is a 4-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants will learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product. This skill building series is divided into four segments:

1. **Overview of Reliability and Statistics.** Participants will learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. **Failure Mechanisms.** Participants will learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, and others.

3. **Qualification Principles.** Participants will learn how test structures can be designed to help test for a particular failure mechanism.

4. **Test Strategies.** Participants will learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The course will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The course will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. The course will offer a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

DAY 1

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information

2. Statistics and Distributions
    a. Basic Statistics
    b. Distributions (Normal, Lognormal, Exponent, Weibull)
    c. Which Distribution Should I Use?
    d. Acceleration
    e. Number of Failures

DAY 2

3. Overview of Die-Level Failure Mechanisms
    a. Time Dependent Dielectric Breakdown
    b. Hot Carrier Damage
    c. Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding
    f. BEOL Dielectric Reliability

4. Package Level Mechanisms
    a. Moisture/Corrosion
        i. Failure Mechanisms
        ii. Models for Humidity
        iii. T_{ja} Considerations
        iv. Static and Periodic stresses
        v. Exercises
    b. Thermo-Mechanical Stress
        i. Models
        ii. Failure Mechanisms
    c. Chip-Package Interactions
        i. Low-K fracture
    d. Through Silicon Via Reliability
    e. Thermal Degradation/Oxidation

DAY 3

5. Board Level
    a. Package Attach (Solder) Reliability
        i. Creep/Sheer/Strain
        ii. Lead-Free Issues
        iii. Electromigration/Thermomigration
        iv. MSL Testing
    b. Board Level Reliability Mechanisms
        i. Interposer
        ii. Substrate

6. Use Condition Failure Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation Effects

7. Test Structures and Test Equipment

8. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises

DAY 4

9. Calculating Chip and System Level Reliability

10. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification

11. JEDEC Tests

12. Exercises and Discussion

Upcoming Courses:

Public Course Schedule:

Advanced CMOS/FinFET Fabrication - May 6-7, 2024 (Mon.-Tues.) | Phoenix, AZ - $995

Failure and Yield Analysis - May 13-16, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 22

Semiconductor Reliability and Product Qualification - May 20-23, 2024 (Mon.-Thurs.) | Phoenix, AZ - $2,095 until Mon. Apr. 29

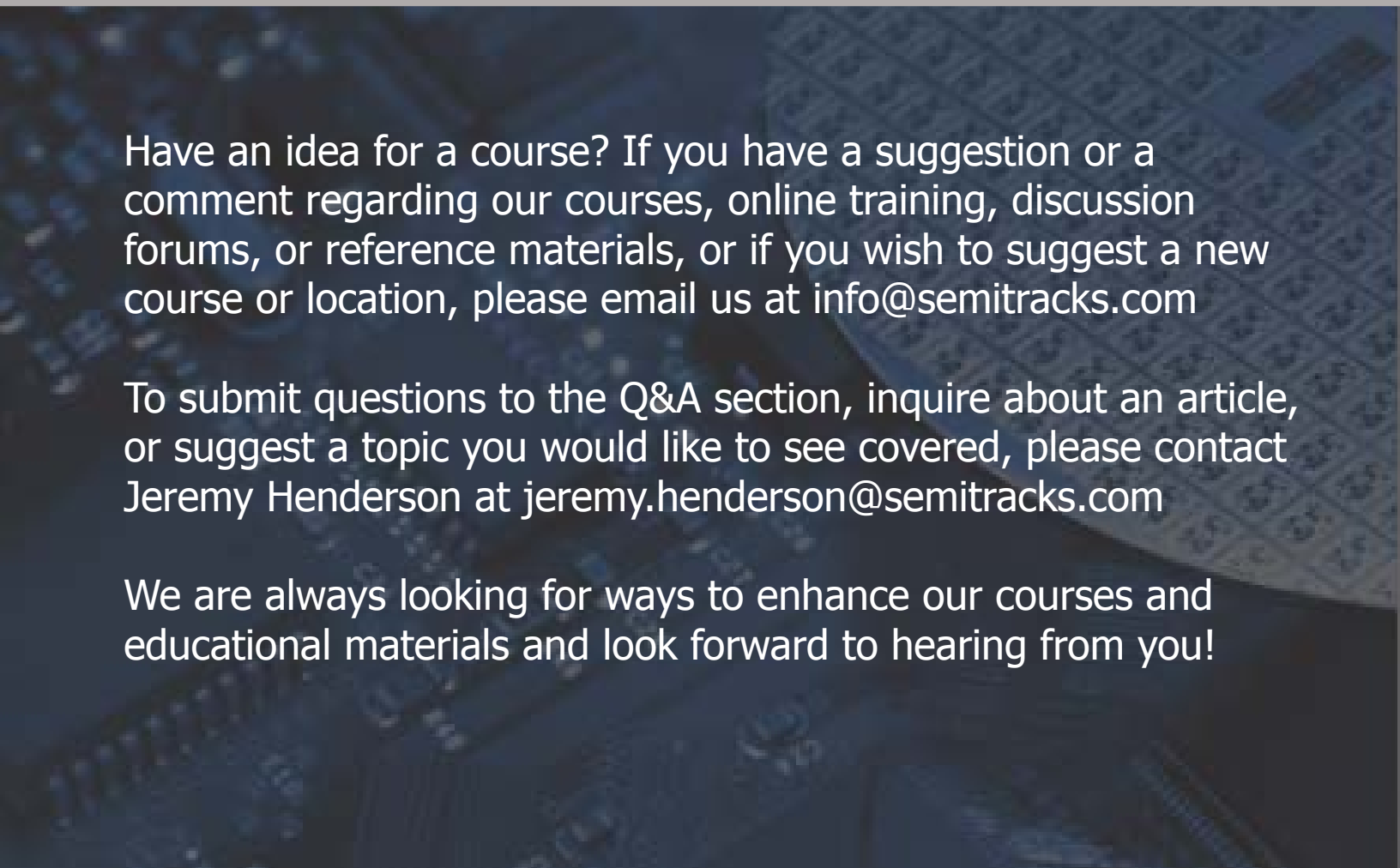
Fundamentals of High-Volume Production Test - May 20-21, 2024 (Mon.-Tues.) | Phoenix, AZ - $1,195 until Mon. Apr. 29

Defect-Based Testing - November 18-19, 2024 (Mon.-Tues.) | Munich, Germany - $1,195 until Mon. Oct. 28

Wafer Fab Processing - November 25-28, 2024 (Mon.-Thurs.) | Munich, Germany -$2,095 until Mon. Nov. 4

Failure and Yield Analysis - December 2-5, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 11

Semiconductor Reliability and Product Qualification - December 9-12, 2024 (Mon.-Thurs.) | Munich, Germany - $2,095 until Mon. Nov. 18



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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!