ISSUE #165
April 2023

SEMITRACKS, INC.

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

By Christopher Henderson

In last month's Feature Article, we continued our series on Cleanroom Technology by discussing Power Usage in a Cleanroom. In this month's Feature Article, we will continue our discussion on Cleanroom Technology with a continued focus on Power Usage in the Fab. Power is an integral part of the cleanroom design and construction, and plays a critical role in the successful processing of wafers.

The exhaust of the cleanroom facility directly affects the fresh air volume of the air conditioning system. As we show in Figure 1, a typical fab uses a make-up air handler, or MUA, to introduce outside ambient air into the cleanroom. Reducing room exhaust can reduce the fresh air volume of air conditioning system, so as to achieve energy saving and emission reduction. The room air balance is achieved by mixing fresh air and cleanroom return air in the Return Air Handler units (RAHs) and sent to the cleanroom through the air duct after treatment. Part of the supply air returns to the RAH, part is discharged to the outdoors, and part is leaked from the cleanroom. Reducing the room exhaust is realized by reusing return air and reducing the local exhaust of the process equipment. The HVAC energy consumption of semiconductor fabrication plants is high. Experts recommend that you reduce room exhaust by process and layout optimization, equipment selection, and risk assessment during the system design phase to achieve energy saving and emission reduction.

WHAT'S INSIDE?

Want to take control of your learning? See page 10

Upcoming Courses:

Failure and Yield Analysis

Semiconductor Reliability and Product Qualification

See page 14 for more details

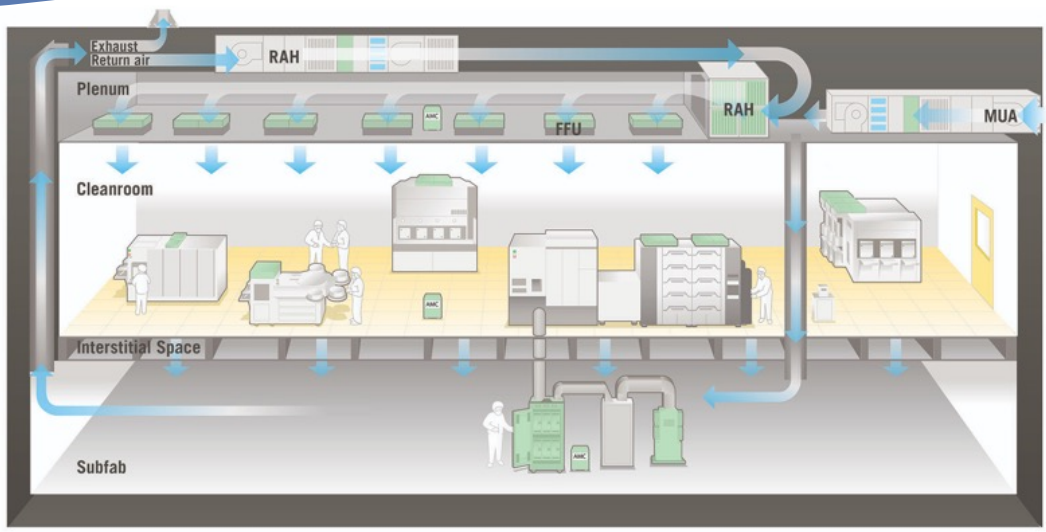

Figure 1- Diagram showing air conditioning flow in a cleanroom (diagram courtesy Entegris).

Sematech performed a survey a number of years ago regarding exhaust optimization, and the list shown below provides good tool exhaust practices that can be used to optimize tool exhaust. They include:

- Talking with the suppliers about the exhaust design and the methods used to achieve a given specification before purchasing and installing a tool
- Conducting an energy survey of fabrication tools, including exhaust measurements
- Following good maintenance practices to check for problems associated with static pressure, duct leaks, and house fans
- Balancing duct static pressure to the specified fabrication requirements as tool installations change
- Using water cooling instead of air to remove heat released from process tools wherever possible
- And finally, using tracer gas testing before a tool is installed to optimize the exhaust requirements from the tools, including gas cabinet enclosures

The next item to discuss is the Fan Filter Unit, or FFU. FFUs consume significant power, so to mitigate power consumption, one should specify high efficiency units. In the past, when engineers chose the required cleanroom classification, the predominant trend at the time had been to specify cleaner and cleaner classifications for the main cleanroom area. Many modern cleanroom designs now depart from that scheme, opting for a fully automated factory, sealed wafer carriers, and tool mini-environments. If the wafers are only exposed to an air stream inside the manufacturing tools, there is no need to operate a cleanroom at Class 1 levels. Instead, each tool has a HEPA filtration system allowing it to achieve Class 1 capability while the ballroom can operate at Class 100 or higher. This change significantly reduced the recirculation air flow rate and number of FFU's required to maintain cleanroom particle specs. The benefits do not stop there; reducing recirculation air flow rate reduces motor power, which in turn reduces sensible heat load, which significantly reduces the requirement for heat rejection equipment such as cooling towers and chillers.

Next, let's briefly discuss low pressure drop air systems. The fab and tool environment pressures must be tightly controlled to prevent turbulent flow, which leads to particle contamination, and even gas phase contamination and backstreaming problems. The air circulation system, coupled with filters, makes this challenging, because effective particle removal requires thicker filters, which slows the movement of air. One can compensate by increasing the air velocity, but this requires stronger fans, which consume more power. State-of-the-art Airborne Molecular Contamination, or AMC, filters are designed from the ground up for gas-phase contamination removal and low outgassing. We show an example of such a filter in Figure 2.

Figure 2- An example of an Airborne Molecular Contamination Filter (photo courtesy Entegris).

High quality materials with low or no AMC outgassing provide chemically clean filter solutions. A pleated design assures low pressure drop and optimized cost of ownership. AMC applications can be categorized into two main flow regimes, low and high flow installations. Air handlers usually require high flows with a 2–3 m/s linear air velocity across the filter. Fan Filter Units and tool filters typically supply air at a lower flow with linear velocity at about 0.5–0.7 m/s, with some installations at 1.0 m/s. The flow regime has a direct impact on filter design, where pressure drop becomes a main concern. That, in turn, dictates how much adsorbent can be accommodated in the filters, having an impact on capacity and filter lifetime. In summary, we need to keep the pressure drop low so that higher air velocities are not required.

Next, let's discuss mini environments. Mini environments can be constructed for various process steps, like chemical mechanical planarization, lithography, defect inspection, periods where wafers might outgas after materials are applied to the surface, or other steps. We show an example of a mini environment for a chemical mechanical polishing tool in Figure 3 on the left. One important example of a mini environment is the Front Opening Unified Pod, or FOUP. We show an example of a FOUP in Figure 3 on the right.

Figure 3- A Chemical Mechanical Polishing mini environment (left), and an example of a Front Opening Unified Pod (right)

FOUP wafer carriers allows semiconductor manufacturers to increase yields by decreasing the contamination that contributes to yield loss. The carrier, which holds up to 26 wafers, limits contact to the wafer edges, thus avoiding potential damage to the back sides of the wafers. The high-performance unit is made from ultrapure materials and features an extremely precise interface to other semiconductor equipment. It is purge-capable and has an electro-static discharge shell option for added wafer protection. This reduces the need for an ultra-clean fab ballroom, and by extension, the power demands of the fab.

There are different technologies used for HVAC Air Systems. One such cleanroom system technology is SWIT, or swirling induction type HVAC, which creates temperature strata inside the cleanroom, and works with rising air currents created by heat-generating equipment to carry airborne dust toward the ceiling. The image in Figure 4 is an example of such a system.

Figure 4- Swirling induction HVAC system (courtesy Fujitsu Semiconductor).

This makes it possible to more efficiently maintain a steady temperature in the work areas at lower elevations in the room, so that the volume of air being supplied can be lower than in conventional HVAC systems. Also, because this allows for air to be supplied at a higher temperature, the chilled-water temperature can also be higher, which contributes to energy savings. Compared to existing systems, the annual energy used is expected to be roughly 47% lower for transport power and roughly 32% lower for heat-source power.

Additionally, this system helps to simplify building construction, so it contributes greatly to a shorter construction process and lower construction costs. Another important approach is to use a decentralized system. Decentralized systems can be tuned to provide the airflow just where it's needed, which can help to reduce the power demands in the fab. The image in Figure 5 shows a Computational Fluid Dynamics simulation of airflow in a fab. The simulation on the left is a non-optimized flow pattern and the simulation on the right is an optimized flow pattern.

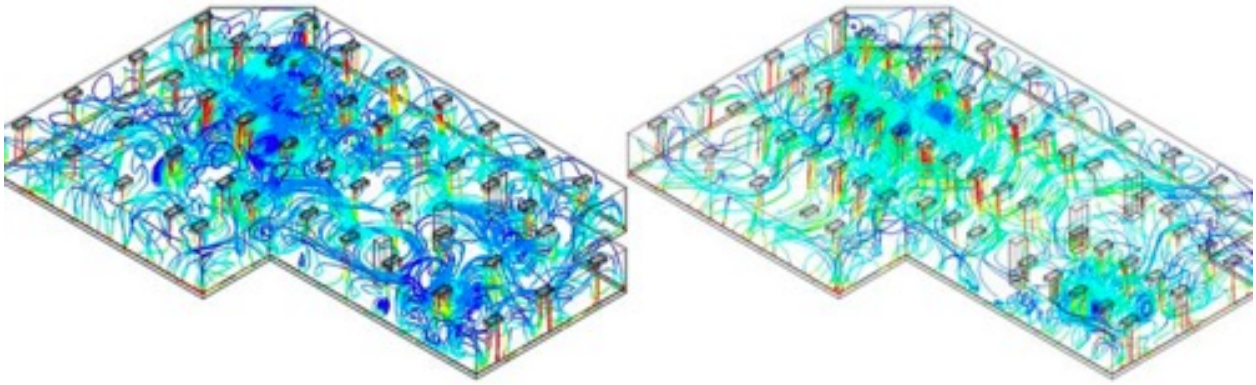

Figure 5- Computational Fluid Dynamics simulation of airflow in a cleanroom (courtesy Cleanroom Technology Magazine)

Another important aspect to power consumption in the fab is the power consumption of the processing tools. Figure 6, from Applied Materials, shows the energy (power consumption) required for process equipment used in the semiconductor device manufacturing process by category.

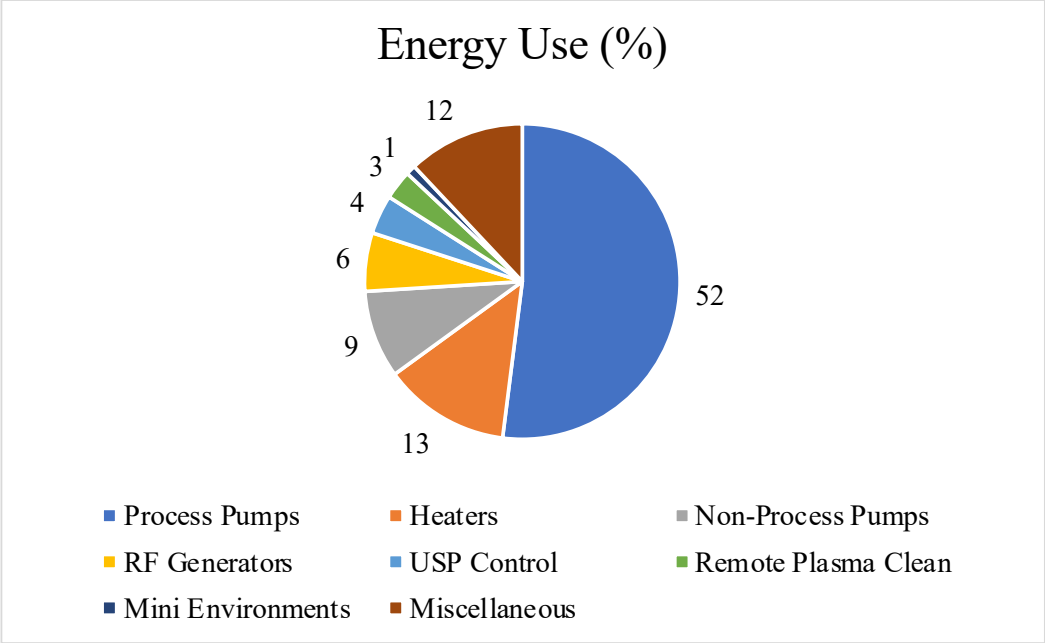

Figure 6- Energy use in a wafer fab cleanroom environment (after Applied Materials)

As shown in the pie chart, process pumps consume, on average, about 52% of the power in a fab tool. For this reason, process vacuum pumps always come first when discussing energy savings within a semiconductor fab. There are a number of approaches to lowering power consumption associated with pumps. They include: lowering the exhaust pressure; using a multi-stage pump; using a pump with a variable frequency drive; using a pump with a high efficiency motor; using variable speeds during idle times; using proximity pumping techniques; lowering the friction within the pump itself; and optimizing the backing or roughing pump.

In conclusion, a number of opportunities exist to reduce power consumption in a wafer fab. We briefly discussed some of these opportunities in this and last month's Feature Articles. Recirculation, chilled water, fans, HVAC systems, vacuum pumps and deionized water generation are but a few of the opportunities for saving power. In the future, power usage will become more critical. Various environmental regulations now limit the generation of power through the burning of fossil fuels, and green energy systems are not yet capable of replacing these power sources. Furthermore, factories are becoming larger and more complex, requiring ever higher power demands. Even when power is available, the heat generation associated with power usage can be significant, and removing that excess heat is expensive. As such, engineers should expect to see an increasing focus on power usage in the semiconductor cleanrooms of the future.

Next month, we will continue our series on Cleanroom Technology by discussing Heating Ventilation and Air Conditioning (HVAC) in more detail.

Technical Tidbit: Functional Block Diagrams

This month's Technical Tidbit covers Functional Block Diagrams. Functional Block Diagrams are a visual aid to understand the layout and functionality of integrated circuits. Historically, a Functional Block Diagram would identify basic circuit elements like transistors. Figure 1 shows an example of a Functional Block Diagram for a 741 Operational Amplifier circuit overlaid on an optical image of the 741 Operational Amplifier circuit, and Figure 2 shows the Functional Block Diagram for the 741 Operational Amplifier circuit overlaid on the schematic for the 741 Operational Amplifier circuit.

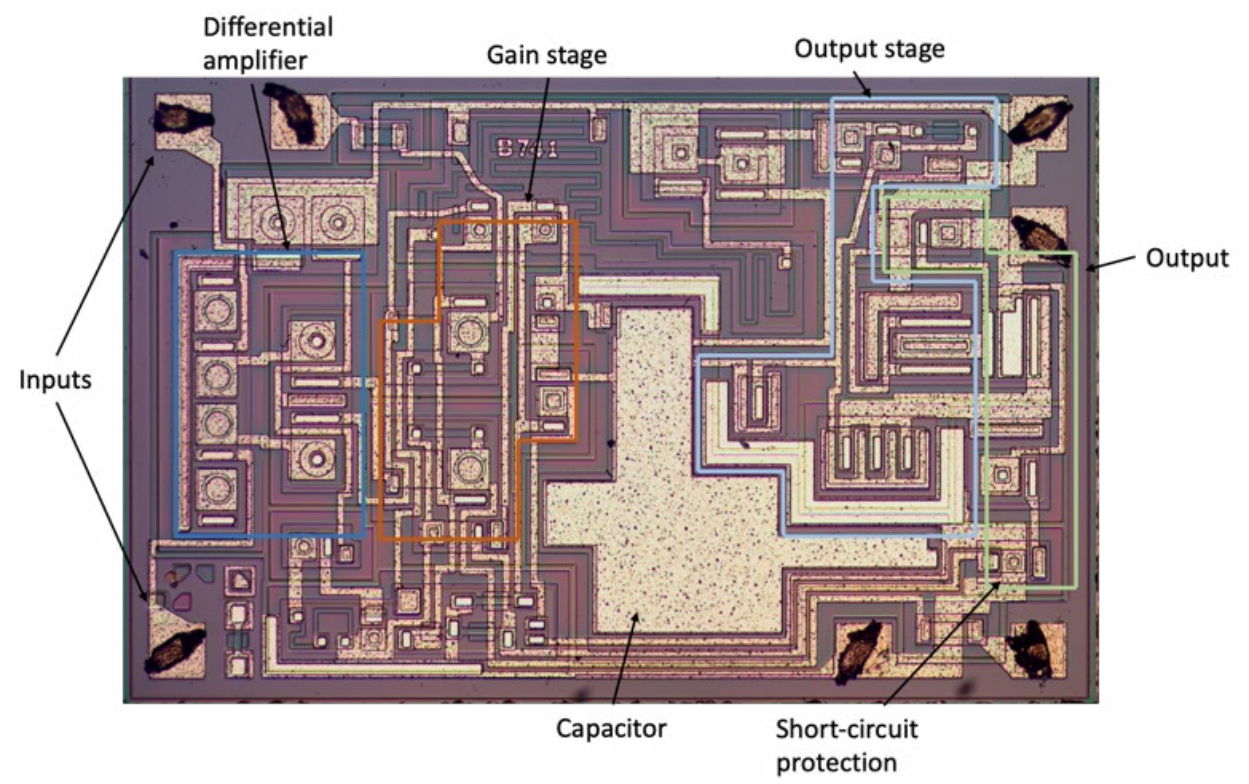

Figure 1- 741 Operational Amplifier Functional Block Diagram overlaid on top of the optical image of the amplifier.

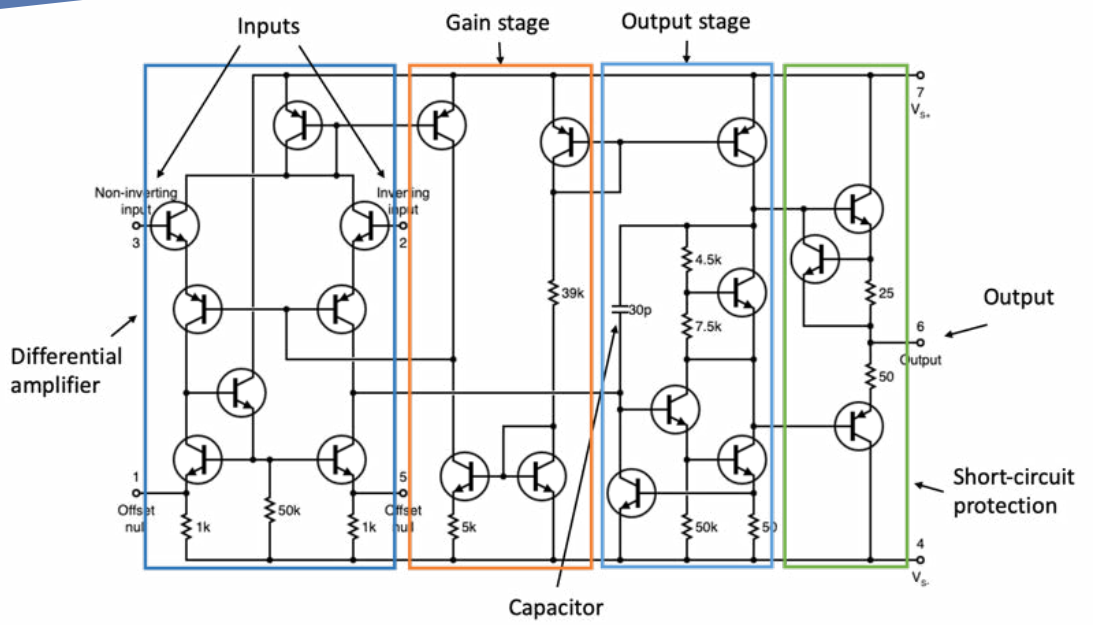

Figure 2- 741 Operational Amplifier Functional Block Diagram overlaid on top of schematic diagram of the amplifier.

For more complex integrated circuits, the Functional Block Diagram contains items that are higher up in the design hierarchy of the integrated circuit. Figure 3 shows an example of an Intel 8085 Microprocessor with the main functional blocks identified, like the Programmable Logic Array (PLA), Arithmetic Logic Unit (ALU), Register File, Instruction Register, Address Bus, Address/Data Bus, and other items.

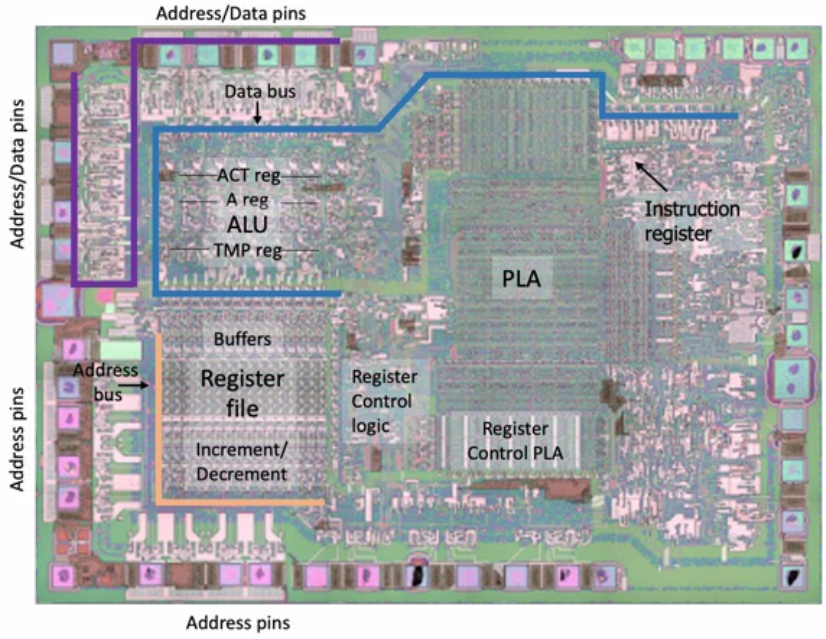

Figure 3- Functional block diagram of an Intel 8085 Microprocessor showing the major blocks or elements of the microprocessor.

For today's integrated circuits, the complexity of the chips means that only the highest levels of the design hierarchy can be shown. Figure 4 shows a Functional Block Diagram for the Intel Core i7 Microprocessor. In this Functional Block Diagram, we show the Central Processing Unit (CPU) cores, the Peripheral Control Interface Express (PCIe) interface, the Level 3 (L3) cache, Memory controller and Instruction Queue.

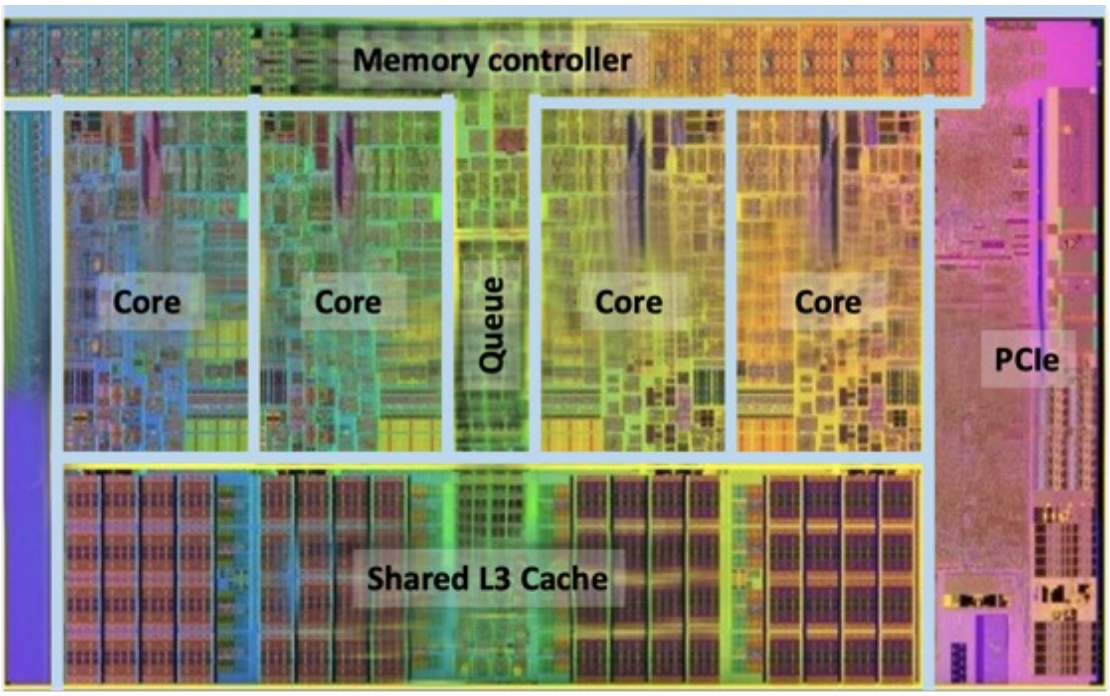

Figure 4- Functional Block Diagram of the Intel Core i7 Microprocessor showing the CPU cores, the PCIe interface, the L3 cache, Memory controller and Queue.

As an engineer working in the semiconductor industry, having a basic knowledge of Functional Block Diagrams can be useful to help understand an integrated circuit's functional behavior. If this topic is of interest to you or your team, please let us know and we can discuss training for your group on this topic.

Ask The Experts

Q: KOH shows a definite preference for etching along certain crystal planes. What about the crystal orientation for other etches like TMAH, EDP, or Choline Hydroxide?

A: This is a complex answer, as there are similarities and differences. With regards to similarities, the short answer is that TMAH, EDP and Choline Hydroxide all show some preference for etching along different crystal planes. These etchants also typically show a minimum amount of etching along the (111) crystal direction. To give you a sense of the differences regarding higher etch rates, we show two plots. Figure 1 shows the plots for TMAH under several different etch conditions. Figure 2 shows the plot for KOH, as a comparison.

Course Spotlight: SEMICONDUCTOR RELIABILITY & PRODUCT QUALIFICATION

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. In particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Product Qualification*** is a 4-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product. This skill building series is divided into four segments:

1. Overview of Reliablility and Statistics. Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. Failure Mechanisms. Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.

3. Qualification Principles. Participants learn how test structures can be designed to help test for a particular failure mechanism.

4. Test Strategies. Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.

2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.

3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.

4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.

7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is application. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

Day One (Lecture Time 8 Hours)

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information
2. Statistics and Distributions
    a. Basic Statistics
    b. Distributions (Normal, Lognormal, Exponent, Weibull)
    c. Which Distribution Should I Use?
    d. Acceleration
    e. Number of Failures

Day Two (Lecture Time 8 Hours)

3. Overview of Die-Level Failure Mechanisms
    a. Time Dependent Dielectric Breakdown
    b. Hot Carrier Damage
    c. Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding
    f. BEOL Dielectric Relability
4. Package Level Mechanisms
    a. Moisture/Corrosion
        i. Failure Mechanisms
        ii. Models for Humidity
        iii. Tja Considerations
        iv. Static and Periodic stresses
        v. Exercises
    b. Thermo-Mechanical Stress
        i. Models
        ii. Failure Mechanisms
    c. Chip-Package Interactions
        i. Low-K fracture
    d. Through Silicon Via Reliability
    e. Thermal Degradation/Oxidation

Day Three (Lecture Time 8 Hours)

5. Board Level
    a. Package Attach (Solder) Reliability
        i. Creep/Sheer/Strain
        ii. Lead-Free Issues
        iii. Electromigration/Thermomigration
        iv. MSL Testing
    b. Board Level Reliability Mechanisms
        i. Interposer
        ii. Substrate
6. Use Condition Failure Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation Effects
7. Test Structures and Test Equipment
8. Developing Screens, Stress Tests, and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises

Day Four (Lecture Time 8 Hours)

9. Calculating Chip and System Level Reliability
10. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification
11. JEDEC Tests
12. Exercises and Discussion

Upcoming Courses:

Failure and Yield Analysis - May 1-4, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Semiconductor Reliability and Product Qualification - May 8-11, 2023 (Mon.-Thurs.) | Oro Valley, Arizona

Have an idea for a course? If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please email us at info@semitracks.com

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!