Issue 118 April 2019

InfoTracks

Semitracks Monthly Newsletter

Overview of Statistical Process Control Part 2

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In this article, we continue with an overview of statistical process control.

Sometimes, data points that we want to measure are not numerical values; they instead might be good or bad values. Put another way, they can be thought of as conforming or non-conforming values. These characteristics can be referred to as attributes.

For conforming or non-conforming data, one can create a control chart by measuring the fraction of data points that are non-conforming:

$$\hat{p} = \frac{D}{n}$$

that is, the number of non-conforming points divided by the total population. For fraction non-conforming, one can set up a control chart with 3σ control limits using the following equations, where p is the centerline.

$$UCL = p + 3\sqrt{\frac{p(1-p)}{n}}$$

$$LCL = p - 3\sqrt{\frac{p(1-p)}{n}}$$

Note: if the LCL value generated by the equation is less than zero, one would substitute in the value 0 rather than use a negative number.

In this Issue:

A variation of the control chart for conforming and non-conforming is the defect chart. It is also known as the small c-chart, or a control chart for the total number defects. For this type of chart, we assume that the presence of defects can be modeled by the Poisson distribution. We show the equation here,

$$P(x) = \frac{e^{-c}c^{x}}{x!}$$

where *x* is the number of defects, and *c,* the population mean number of defects, is a number greater than zero.

One can define limits for a C-chart, or a chart showing the fraction of non-conforming. The upper control limit is shown here,

$$UCL = c + 3\sqrt{c}$$

along with the lower control limit.

$$LCL = c - 3\sqrt{c}$$

This assumes that we know *c,* or the centerline. If we don't know *c,* then we can estimate if from the sample in the control chart ($\bar{c}$). If that is the case, then the UCL and LCL are calculated as shown here.

$$UCL = \bar{c} + 3\sqrt{\bar{c}}$$
$$LCL = \bar{c} - 3\sqrt{\bar{c}}$$

Let's show an example so we can see how this works. Suppose we inspect 25 silicon wafers and identify 37 defects. We then want to set up a control chart to look at the results. First, we estimate the centerline *c* by generating $\bar{c}$ which would be 37 defects divided by 25 wafers.

$$\bar{c} = \frac{37}{25} = 1.48$$

This becomes our centerline. The ULC and LCL values can then be calculated from the deviation away from the control line using the equations here.

$$UCL = \bar{c} + 3\sqrt{\bar{c}} = 5.13$$
$$LCL = \bar{c} - 3\sqrt{\bar{c}} = -2.17$$

This yields a UCL value of 5.13, and an LCL value of -2.17. Since we can't have a negative number of defects, we substitute zero in for the LCL.

Another variation of the control chart for attributes is the defect density chart. This chart is also known as the u-chart, and is a control chart for the average number of defects over a sample size of n products. So, if there are *c* total defects among *n* samples, the average number of defects per sample would be u, shown in the equation here.

$$u = \frac{c}{n}$$

The 3σ limits for a u-chart are given by these two equations,

$$UCL = \bar{u} + 3\sqrt{\bar{u}/n}$$

where $\bar{u}$ is the center line.

$$LCL = \bar{u} - 3\sqrt{\bar{u}/n}$$

We define *u* as the average number of defects over m groups of size *n*.

Let's show an example of the u chart. Suppose we want to establish a defect density chart. We inspect 20 different groups of 5 wafers, and we find a total of 183 defects. We set up the u-chart as follows. First, we estimate the value of u using:

$$\bar{u} = \frac{u}{m} = \frac{c}{mn} = \frac{183}{(20)(5)} = 1.83$$

There are 183 defects, our sample size is 5, and the number of groups is 20. Working through the math we get 1.83 for $\bar{u}$. This forms the centerline. We can then calculate the UCL and LCL from the following equations,

$$UCL = \bar{u} + 3\sqrt{\bar{u}/n} = 3.64$$
$$LCL = \bar{u} - 3\sqrt{\bar{u}/n} = 0.02$$

giving us 3.64 and 0.02 respectively.

Sometimes, quality characteristics might be expressed as specific numerical measurements, like the thickness of a film. In this case, we can use the control chart to provide more information regarding the manufacturing process performance.

For this type of work, we construct an $\bar{x}$ chart to control the mean and variance. $\bar{x}$ is equal to the sum of the individual values divided by the number of data points.

$$\bar{x} = \frac{x1+x2+\cdots xn}{n} = \frac{1}{n}\sum_{i=1}^{n} x_i$$

Likewise, we can monitor variance by constructing an s-chart, where s is given by this equation:

$$s = \sqrt{\frac{1}{n-1}\sum_{i=1}^{n}(x_i - \bar{x})^2}$$

One can then set the control limits for an $\bar{x}$ chart as follows,

$$UCL = \bar{\bar{x}} + 3\sqrt{\sigma^2/n}$$

where the UCL is the grand average plus 3 times the square root of $\sigma 2/n$, and LCL is the grand average plus 3 times the square root of $\sigma 2/n$.

$$LCL = \bar{\bar{x}} - 3\sqrt{\sigma^2/n}$$

We define the grand average as the sum of the individual means divided by the number of groups m.

$$\bar{\bar{x}} = \frac{\bar{x}_1 + \bar{x}_2 + \cdots + \bar{x}_m}{m}$$

Similarly, we can set control limits for the variance. Here we show the equations for UCL and LCL as a function of the center and c_4,

$$UCL = \bar{s} + 3\frac{\bar{s}}{c_4}\sqrt{1 - c_4^2}$$
$$Center = \bar{s}$$
$$LCL = \bar{s} - 3\frac{\bar{s}}{c_4}\sqrt{1 - c_4^2}$$

where the center is defined as one over m times the sum of the individual s values, and c_4 is a constant.

$$\bar{s} = \frac{1}{m}\sum_{i=1}^{m} s_i$$

C_4 is a statistical parameter that is dependent on the sample size. A typical approximation for c_4 is 4(n-1)/(4n-3).

One can also define modified control limits for the mean, shown by these two equations here:

$$UCL = \bar{\bar{x}} + \frac{3\bar{s}}{c_4\sqrt{n}}$$

$$LCL = \bar{\bar{x}} - \frac{3\bar{s}}{c_4\sqrt{n}}$$

Here is an example showing how to calculate limits for mean and variance charts. Suppose $\bar{x}$ and $\bar{s}$ -charts are to be established to control linewidth in a lithography process, and 25 samples of size n = 5 are measured. The grand average for the 125 lines is 4.01 μm. If $\bar{s}$ = 0.09 μm, what are the control limits for the charts? We use the equations we just discussed, shown here,

$$UCL = \bar{\bar{x}} + \frac{3\bar{s}}{c_4\sqrt{n}} = 4.14\mu m$$

$$LCL = \bar{\bar{x}} - \frac{3\bar{s}}{c_4\sqrt{n}} = 3.88\mu m$$

and plug in the values. $\bar{\bar{x}}$ is the grand average. We can look up or calculate a value for c_4 and plug it in. This yields these results for the upper and lower control limits.

Here are the results for the control of the variances in the s-chart. Since the LCL is less than zero, that doesn't make sense as an answer, so we instead substitute in the value of zero.

$$UCL = \bar{s} + 3\frac{\bar{s}}{c_4}\sqrt{1 - c_4^2} = 0.19\mu m$$

$$LCL = \bar{s} - 3\frac{\bar{s}}{c_4}\sqrt{1 - c_4^2} = 0.00\mu m$$

To be continued next month…

Technical Tidbit

Pattern Fidelity

One of the challenges we face in lithography at the leading edge is pattern fidelity. Is the lithography process printing the features as we want them to be printed? One method to analyzing pattern fidelity is to extract the contour of the layer of interest from the SEM image, then use pattern matching to match the intended features to the actual features, and then use edge placement error analysis to determine how far off we are from what we intended. There are a variety of pattern fidelity errors that can occur, and we show several of them in Figure 1. They include size differences in x and y, push out and pull back, maximum and minimum critical dimension violations, protrusions or necking, and tip-to-tip or side-to-side problems. This is good. What do these cause at the product level?

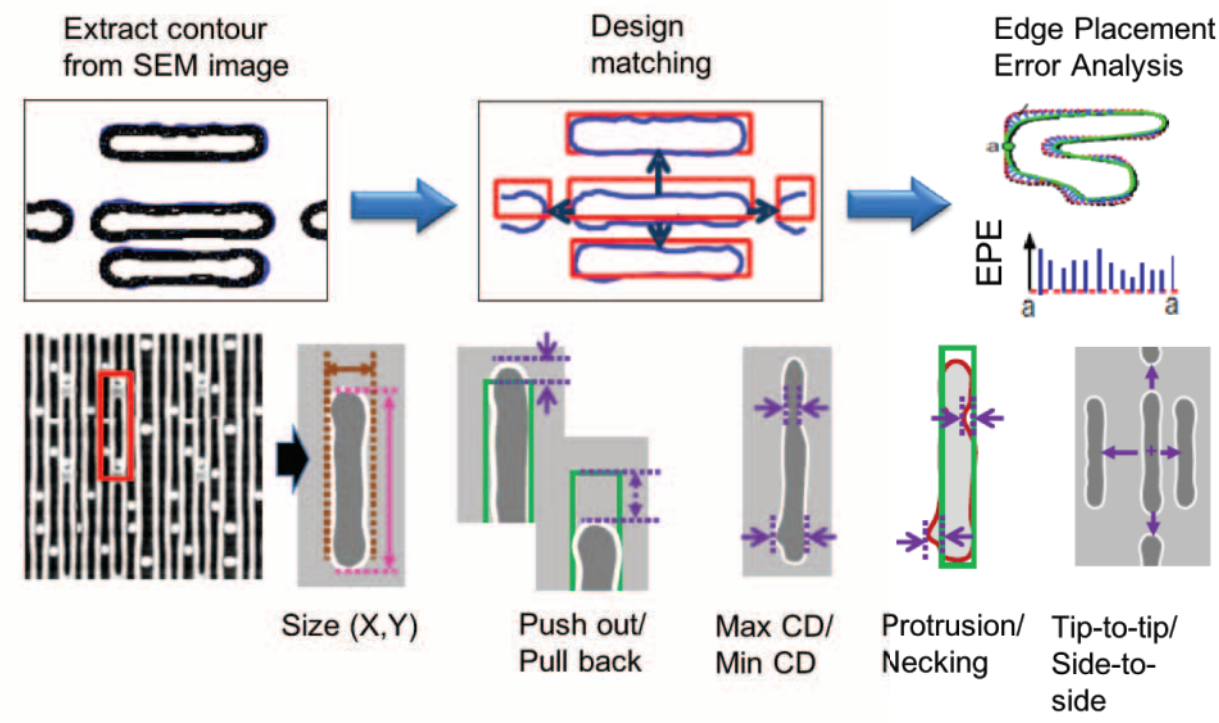


Figure 1. M. Nozoe, Frontiers of Characterization and Metrology for Nanoelectronics, 2017.

Let's now see what the effects of pattern fidelity might be on a standard cell. We show the target layout of the standard cell on the left in Figure 2, and the patterns on the silicon wafer after final etching on the right. In this case we use double-patterning, and have a metal A and a metal B, denoted by MA in green and MB in orange. On the left, we highlight a region of MB where there is a risk of a missing connection due to a potential line-end pull-back. On the right, we highlight a region where there is a risk of leakage current due to a line-end push-out.

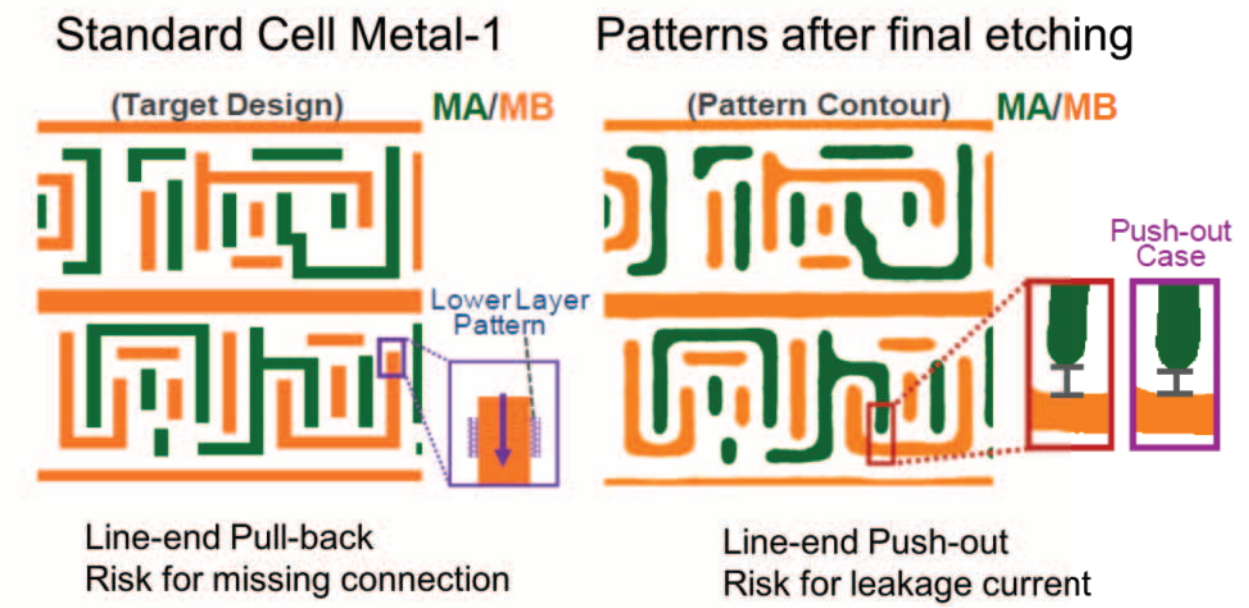


Figure 2. M. Nozoe, Frontiers of Characterization and Metrology for Nanoelectronics, 2017.

To understand pattern fidelity problems, we will need to study the differences between the intended layout and the actual layout in more detail. Let's look at the results from a different standard cell in Figure 3. Again, we have our double-patterning with MA and MB. The intended layout is on the left, and a portion of the actual layout on the right. To create the evaluation points, we align the image to the design data. We can then look at the important differences. In this example, we have 6 end effects. Notice that the end effect at location 1 is the worst, followed by the end effects at locations 6 and 5 respectively. The other line-end pull-backs are not as bad.

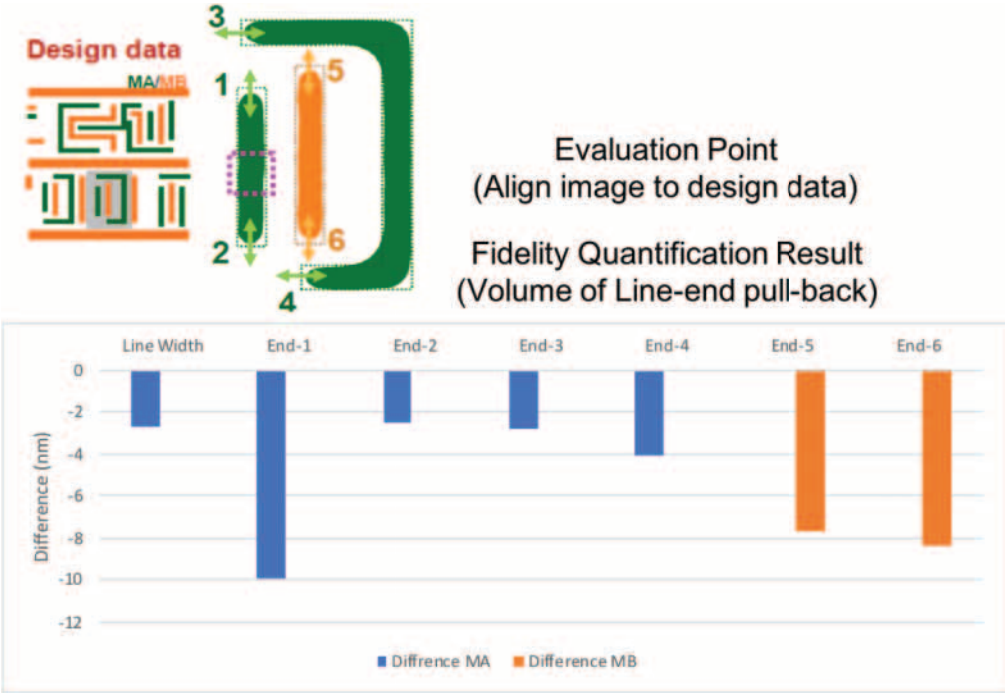


Figure 3. M. Nozoe, Frontiers of Characterization and Metrology for Nanoelectronics, 2017.

Ask the Experts

Q: What does EFO stand for?

A: EFO stands for Electronic Flame Off. Electronic Flame Off is a spark mechanism designed to melt the end of the bond wire just prior to placing the ball bond. EFO is necessary with copper wire bonding, since copper wire bonding must occur in a non-oxidizing environment (using a forming gas N2/H2 mixture) to avoid oxidation of the copper.

Spotlight: Advanced CMOS/FinFET Fabrication

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" Advanced CMOS/ FinFET Fabrication is a 1-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

WHAT WILL I LEARN BY TAKING THIS CLASS

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs and FD-SOI are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including ion implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

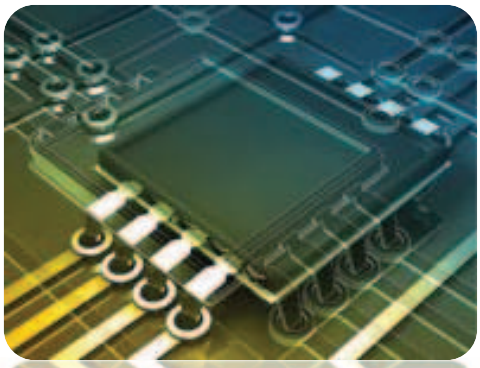
1. The seminar will provide participants with an in-depth understanding of SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.

4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FD-SOI (the leading alternative) and FinFETs.

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
    a. SOI and FD-SOI
    b. Ion Implantation and Rapid Thermal Annealing
    c. Pulsed Plasma Doping
    d. Hi-K/Metal Gates
    e. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology
3. Back End Of Line (BEOL) Processing
    a. Introduction and Performance Issues
    b. Copper
        i. Deposition Methods
        ii. Liners
        iii. Capping Materials
        iv. Damascene Processing Steps
    c. Lo-k Dielectrics
        i. Materials
        ii. Processing Methods
    d. Reliability Issues
4. FinFET Manufacturing Overview
    a. Substrates
        i. Bulk
        ii. SOI
    b. FinFET Types
    c. Process Sequence
    d. Processing Issues
        i. Lithography
        ii. Etch
        iii. Metrology

5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FD-SOI and FinFETs – Are FinFETs a better choice?
   b. Scaling



Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA

Failure and Yield Analysis
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!