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InfoTracks

Semitracks Monthly Newsletter

Low-K Materials Properties Part 2

By Christopher Henderson, continued from last month

In this section, we will continue to discuss the materials properties of low-k materials. The properties of these materials are key to understanding the reliability in these applications. The industry is just beginning to understand these materials and how they behave in thin films and semiconductor applications.

This discussion will center on two materials properties groups. They include the thermal properties, and the chemical properties. First, we'll discuss the thermal properties of low-k materials.

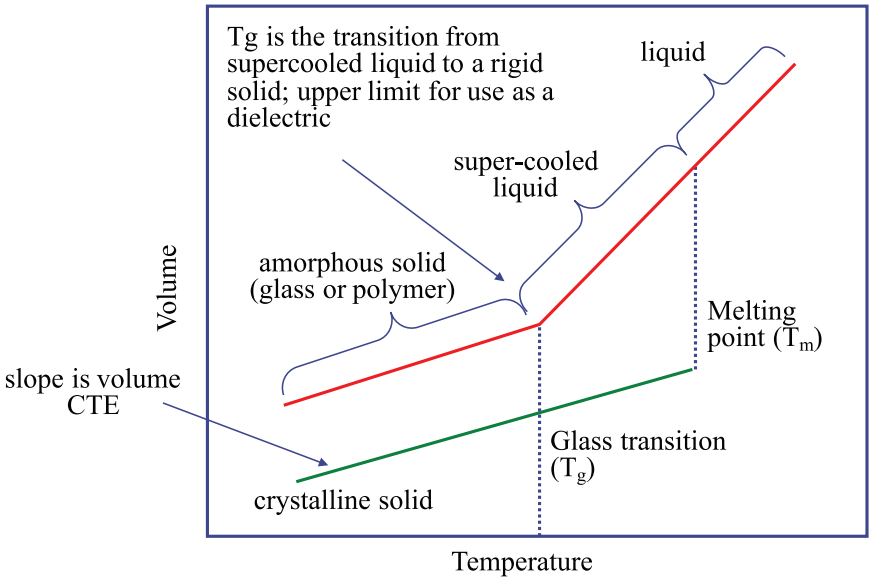


Figure 1. Glass transition temperature.

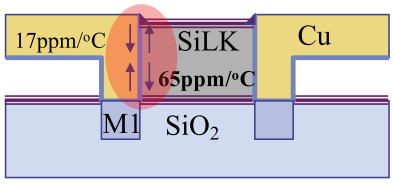
In this Issue:

The first material property we will discuss is the glass transition temperature. If we take a material and cool it from the melting point, we notice a distinct change in the volume versus temperature curve as we go from a liquid to a solid. The green curve shows a crystalline material. For an amorphous material, there is a minor change or no change between a liquid and a super-cooled liquid, but we do have a distinct transition to a solid. The point at which the transition between super-cooled liquid and amorphous solid occurs is called the glass transition temperature. The glass transition temperature represents the maximum temperature to which a material can be exposed during further processing.

$$DL / L_o = \alpha DT$$

α = Linear CTE, Slope of thickness vs. temperature curve (out-of-plane CTE)

- Materials generally expand as temperature increases
- For integrated circuits and packages, thermal cycling occurs during processing and during operation
- Differences in CTE can cause plastic deformation and fatigue



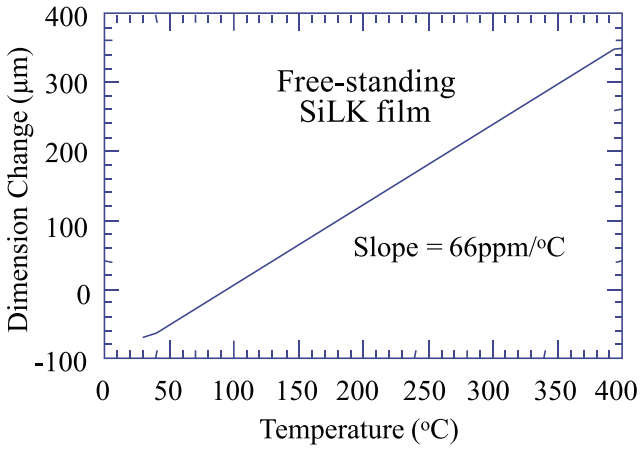


Figure 2. Coefficient of thermal expansion (CTE).

Another important thermal property is the coefficient of thermal expansion. Figure 2 helps to illustrate why the industry would prefer to use materials with lower coefficients of thermal expansion. As we heat a material, it expands. The graph on the right shows how the SiLK polymer expands as a function of temperature. Its slope or coefficient of thermal expansion is quite high, 66 parts per million per degree centigrade. If this material is used in an IC, it will expand and contract during subsequent processing or during use conditions. Since SiLK has a much higher coefficient of thermal expansion than the copper interconnect, there will be a fairly large stress in the copper or at the interface during thermal cycling. The repetitive expansion and contraction can fatigue the copper, causing cracks to form in the vias. This represents the biggest problem with using polymers as a low dielectric constant material. High coefficients of thermal expansion are inherent in polymers, and this in turn leads to high levels of stress in the interconnect.

Therefore, the film stress increases with CTE mismatch between the film and the substrate. One can measure the coefficient of thermal expansion from the slope of the stress versus the temperature curve if one knows the modulus and Poisson's ratio. The film stress σ_f is represented by the equation shown here,

$$\text{Film stress} = \sigma_f = \frac{(\alpha_s - \alpha_f)DT}{(1-\nu_f)/E_f + (1-\nu_s)\, d_f / d_s E_s}$$

D CTE; substrate - film

Poisson's ratio (film)

Young's modulus (film)

thickness (film)

where ν_f is Poisson's ratio for the film, E_f is Young's modulus for the film, and d_f is the thickness of the film.

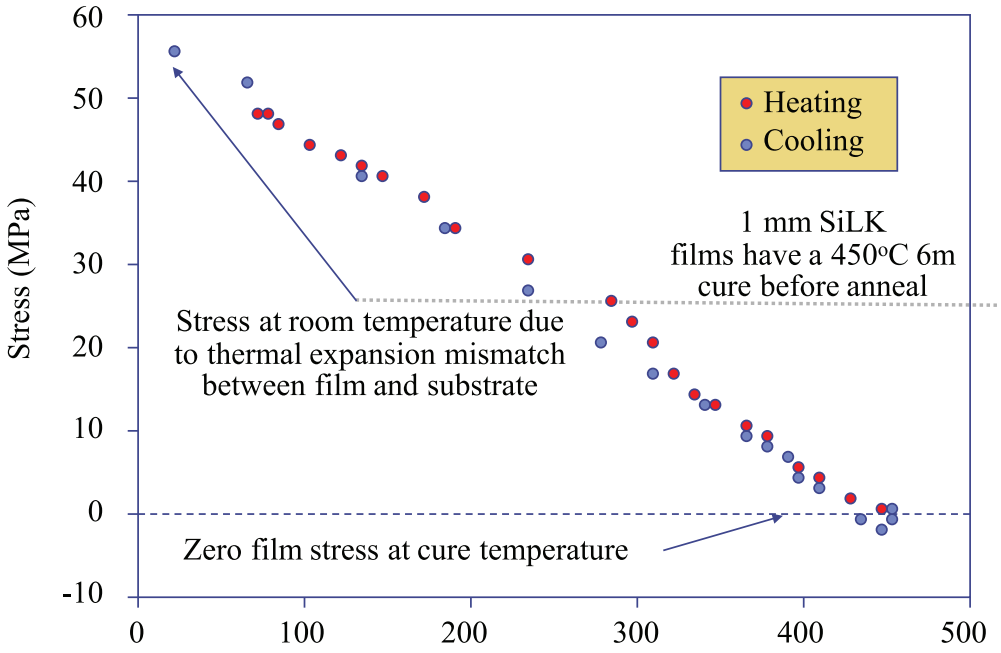


Figure 3. CTE: effect on stress.

Figure 3 shows the stress versus temperature curve for a 1 millimeter thick SiLK film that was cured at 450°C for 6 minutes before anneal. Notice that the stress increases as the temperature gets lower. The zero point for the stress is the film cure temperature, or in this case 450°C.

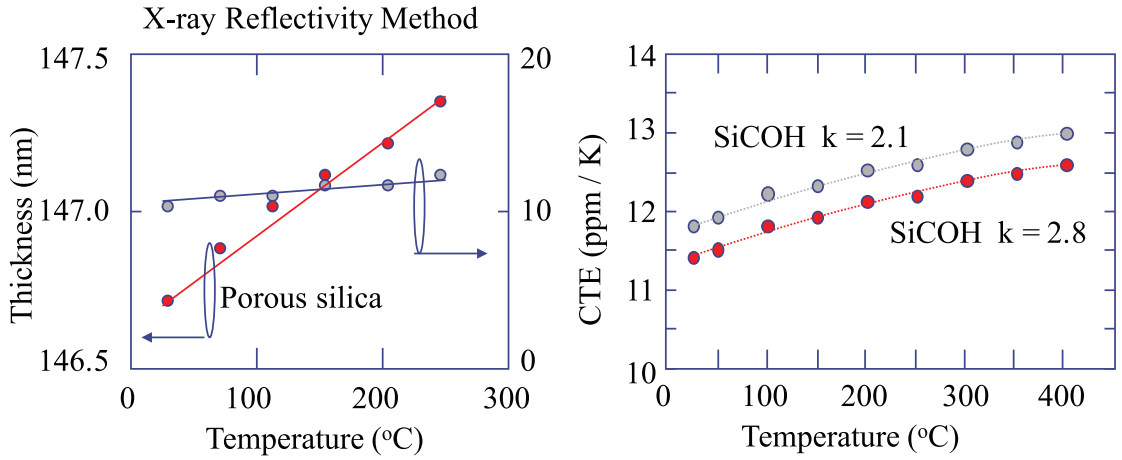


Figure 4. CTE: porous silica and SiCOH.

The oxide-based dielectrics have much smaller coefficients of thermal expansion. The chart on the left in Figure 4 shows that the coefficient of thermal expansion for porous silica is approximately 12 parts per million per degree centigrade, while the graph on the right shows a CTE of about 12 as well for SiCOH. For SiCOH, the CTE appears to be somewhat independent of whether the material is porous or not.

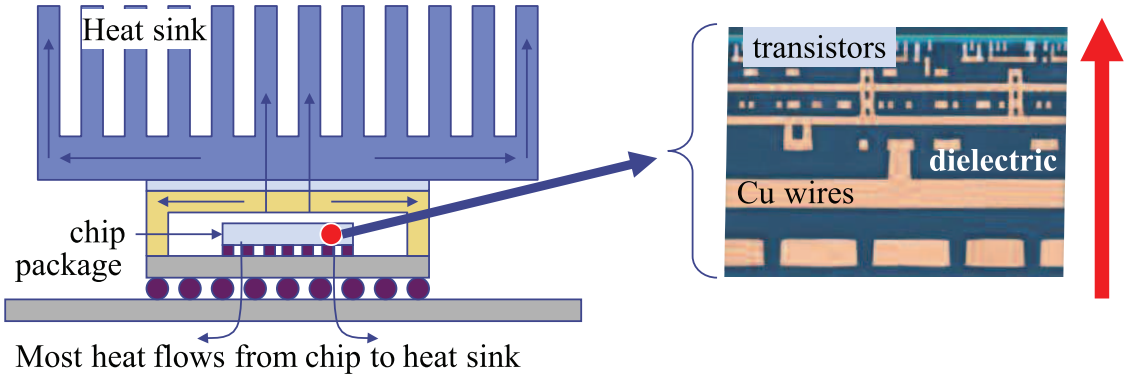


Figure 5. Low-k materials have low thermal conductivity.

Thermal conductivity is another big problem with these materials. It becomes lower as one introduces porosity into the material. Thermal conductivity is an important issue. As we shrink devices and run them at higher currents, there is more power consumption. This leads to more current through the wires. Smaller wires mean higher current densities which lead to additional heating. This can cause higher wire resistance and can lead to electromigration failures. This heat must be dissipated somehow. The only way to remove the heat is to conduct the heat through the IC to a heatsink (Figure 5, left). This means the heat must travel through the dielectric materials (Figure 5, right). If we reduce the thermal conductivity of the dielectric, it will be harder to get the heat out and away from the wires.

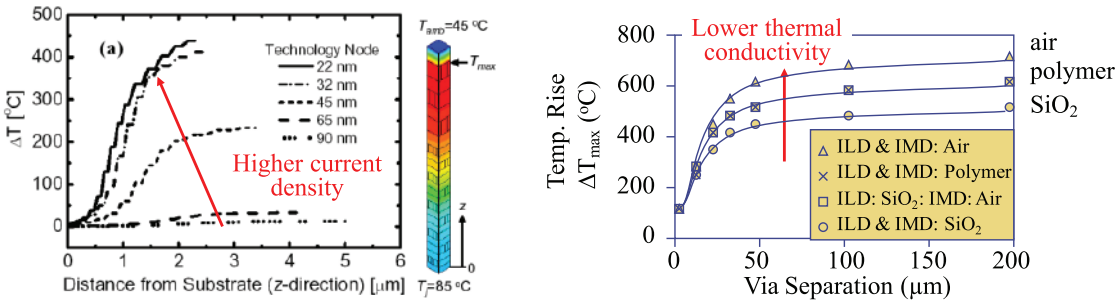


Figure 6. Thermal conductivity: effect on ICs.

These graphs in Figure 6 show how the temperature rises as we move from SiO_2 as a dielectric to a polymer and eventually to air. As we do this, the thermal conductivity gets worse. One way to help dissipate heat is to make better use of the metal to dissipate the heat. By creating vias to other layers, there is more opportunity to dissipate the heat in the wires.

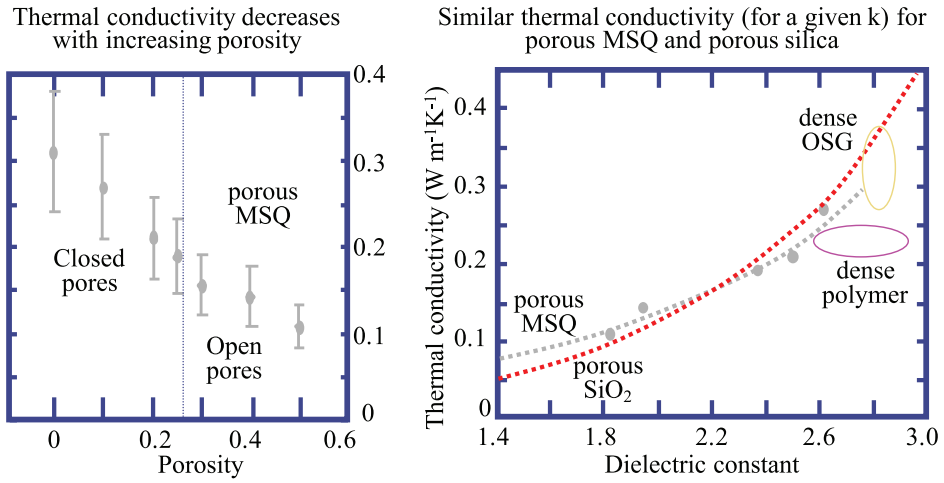


Figure 7. Thermal conductivity: effect of porosity.

In summary, the glass transition temperature represents the upper limit at which the material can be used or subsequently processed. The coefficient of thermal expansion is important during thermal cycling. A large difference in the thermal coefficients of expansion in the materials system can cause the metal to fatigue. Thermal conductivity is important due to the increased power dissipation. Unfortunately, the thermal conductivity goes down as the dielectric constant decreases. This makes it more difficult to reduce heating in the chip.

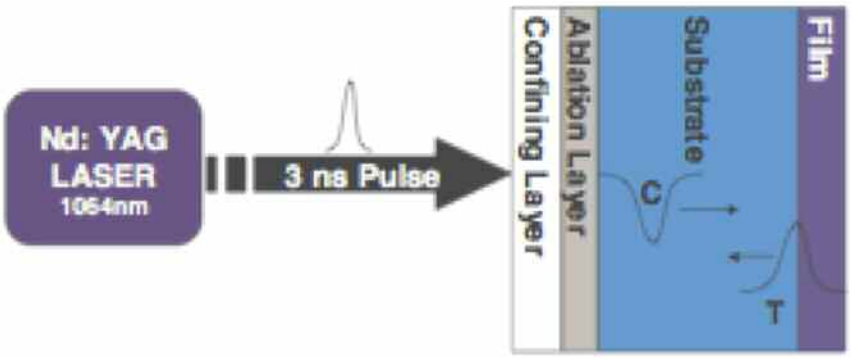
In next month's issue, we'll continue this section and cover chemical stability issues with low-k materials.

Technical Tidbit

Laser Spallation

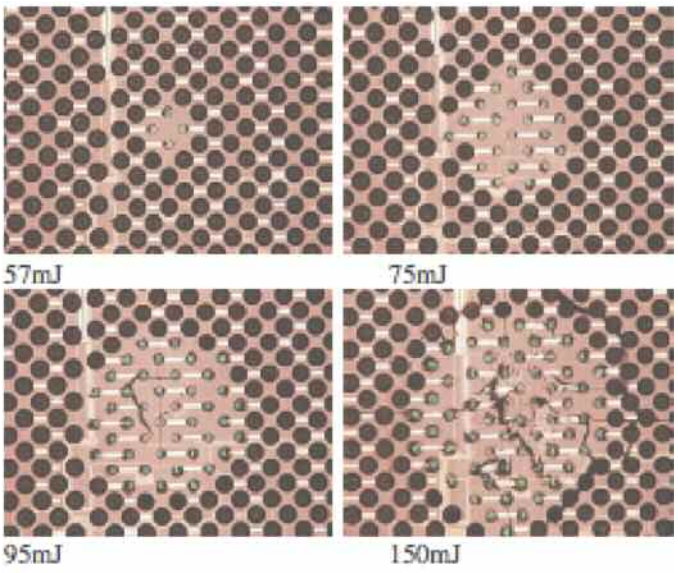
For this month's technical tidbit, we will briefly discuss laser spallation.

Laser induced spallation is a recent experimental technique developed to understand the adhesion of thin films with substrates. A high energy pulsed laser (typically Nd:YAG) is used to create a compressive stress pulse in the substrate wherein it propagates and reflects as a tensile wave at the free boundary. This tensile pulse spalls/peels the thin film while propagating towards the substrate. Using theory of wave propagation in solids it is possible to extract the interface strength. The stress pulse created in this fashion is usually around 3 – 8 nanoseconds in duration while its magnitude varies as a function of laser fluence. Due to the non-contact application of load, this technique is very well suited to spall ultra-thin films (1 micrometer in thickness or less).



Schematic of stress pulse generation

It is also possible to mode convert a longitudinal stress wave into a shear stress using a pulse shaping prism and achieve shear spallation. In the example we show here, we use laser spallation to examine the adhesion of solder bumps to pads.



Notice that at increased energies, the laser dislodges more solder bumps. When the energy is high enough, it also begins to damage the low-k dielectric materials as well.

Ask the Experts

Q: I have automotive customers who are asking me to demonstrate 1 DPPM levels. Is this really even possible?

A: This is an often-asked question and one that does not have a simple answer. The short answer is "maybe." The more nuanced answer follows. To even begin to demonstrate this, you will need to do further testing beyond what you normally do with JEDEC 47 or AEC-Q100. Probably the best thinking on this topic that is generally available to the public is a concept known as Robustness Validation. ZVEI has a publicly available document which discusses this topic in some detail. Although it doesn't directly answer the 1 DPPM question, it will get you thinking about what might be required to demonstrate whether or not you can reach it.

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Spotlight: CMOS, BiCMOS, and Bipolar Process Integration

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's mixed-signal chips perform a wide range of applications unheard of a few years ago, including wireless applications, high speed communications, and signal processing. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. A corollary to Moore's Law is that frequencies on mixed-signal devices continue to rise. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***CMOS, BiCMOS, and Bipolar Process Integration*** is a 3-day course that offers detailed instruction on the physics behind the operation of a modern mixed-signal integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to designing and manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the fundamentals of transistor operation and performance, participants will learn why advances in the industry are occurring along certain lines and not others. Our instructors work hard to explain how semiconductor devices work without delving too heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Device Operation.** Participants learn the fundamentals of transistor operation. They learn why BiCMOS devices dominate the mixed-signal industry today.
2. **Fabrication Technologies.** Participants learn the fundamental manufacturing technologies that are used to make modern integrated circuits. They learn the typical CMOS, Bipolar and BiCMOS process flows used in integrated circuit fabrication.
3. **Current Issues in Process Integration.** Participants learn how device operation is increasingly constrained by three parameters. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future..
4. **An Overview of Issues Related to Process Integration.** Participants learn about the image of new materials, yield, reliability and scaling on technology and process integration. They receive an overview of the major reliability mechanisms that affect silicon ICs today.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind transistor operation and performance.
3. The seminar will identify the key issues related to the continued growth of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of device operation and manufacturing.

5. Participants will be able to identify basic and advanced technology features on semiconductor devices. This includes features like silicon-germanium, emitter islands, copper, and low-k dielectrics.
6. Participants will understand how reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate new CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor devices and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
2. Basic Semiconductor Concepts
    a. Diffusion/Drift
    b. PN Junction Diodes
    c. Bipolar Junction Transistor
    d. MOS Transistor
    e. Additional Concepts
        i. Avalanche Breakdown
        ii. Zener Breakdown
        iii. Tunneling
        iv. Schottky Barriers
3. General Scaling Issues
    a. Constant Field Scaling/Constant Voltage Scaling
    b. Process Integration Issues
        i. Transistors (Ion vs Ioff, Mobility Enhancement, short channel effects, etc.)
        ii. Interconnect (RC delay, power dissipation, etc.)
    c. Limitations to Scaling

Day 2

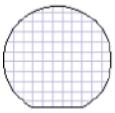
4. Conventional CMOS
   a. Well/Substrate Engineering
   b. Device Isolation
   c. Gate Stack
   d. Contacts/Silicide
   e. Scaling Issues
   f. Basic CMOS Flow Presentation
5. Conventional BiCMOS
   a. Bipolar Transistor Fundamentals
   b. BiCMOS Process Overview
   c. Scaling and Limitations
   d. Basic BiCMOS Flow Presentation
6. Bipolar Enhancement Techniques
   a. SiGe
   b. SiGe:C
7. Power Technologies
   a. LDMOS
   b. DECMOS
   c. BCD
8. Additional Analog Circuit Elements
   a. Resistors
   b. Capacitors
   c. JFETs

Day 3

9. Interconnects
   a. Aluminum Interconnects, Issues
   b. Copper Interconnects, Issues
   c. Low-k Dielectrics
10. CMOS/Bipolar/BiCMOS Reliability Considerations
   a. Electrostatic Discharge
   b. Electromigration and Stress Migration
   c. Soft Errors, Plasma Damage
   d. Dielectric Reliability
   e. Bias Temperature Instabilities
   f. Hot Carrier Reliability
   g. Burn-In
11. Yield Considerations
   a. Yield Detractors
   b. Models
   c. Monitors
12. Conclusion/Wrap Up

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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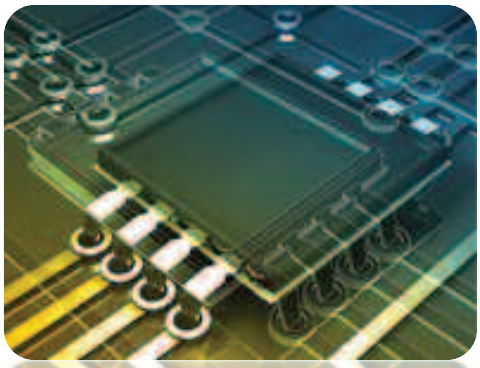
Semitracks is planning to demonstrate our Online Training Software for Failure Analysis at ISTFA. For more information, please contact us at info@semitracks.com



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(Click on each item for details)

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April 16 – 19, 2018 (Mon – Thur)
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Wafer Fab Processing
June 4 – 6, 2018 (Mon – Wed)
Singapore

Semiconductor Reliability / Product Qualification
June 11 – 14, 2018 (Mon – Thur)
Singapore

CMOS, BiCMOS and Bipolar Process Integration
September 10 – 12, 2018 (Mon – Wed)
San Jose, California, USA