

# InfoTracks

Semitracks Monthly Newsletter

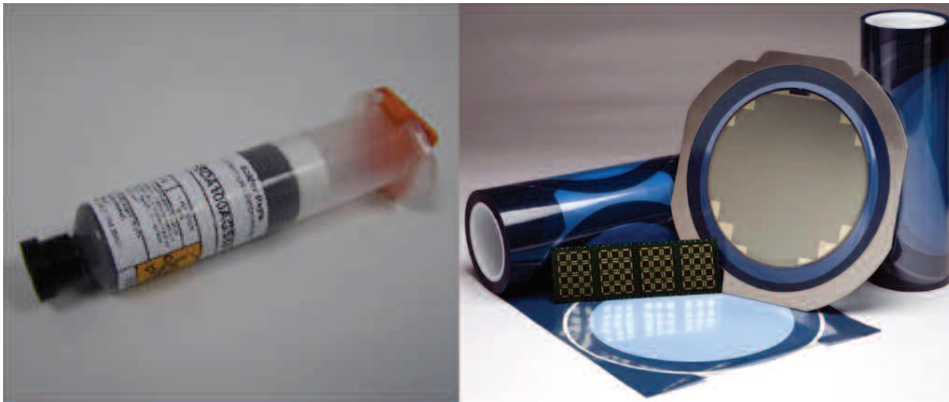


## Die Attach 1

By Christopher Henderson

In this section we will cover die attach materials. There are several major classes of materials, including liquid-dispensed materials and adhesive films. Stay tuned as we cover this topic in the following slides.

We will cover the two major types of die attach: epoxy die attach, and eutectic die attach. An epoxy die attach consists of a polymer thermoset loaded with a conductive material, like silver. A eutectic die attach consists of two conductive metals alloyed together in the correct ratio to produce a eutectic material.



There are some other additional properties that can be important for certain applications. For instance, a one-component epoxy system

## In this Issue:

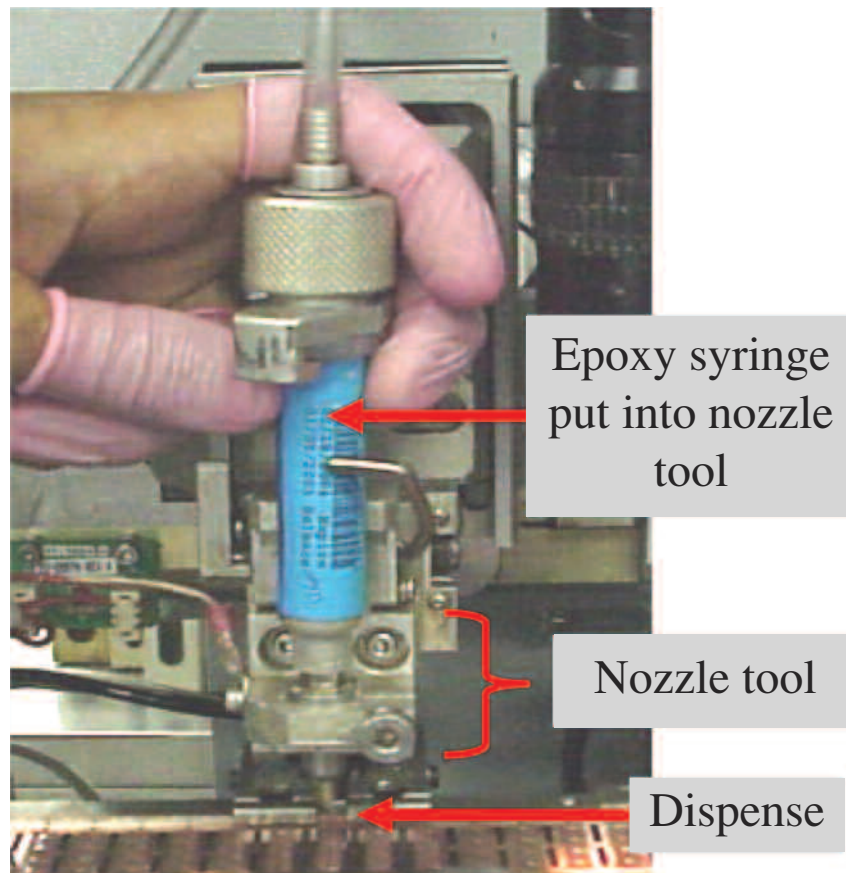
Page 1	Die Attach 1
Page 5	Technical Tidbit
Page 6	Ask the Experts
Page 7	Spotlight
Page 11	Upcoming Courses



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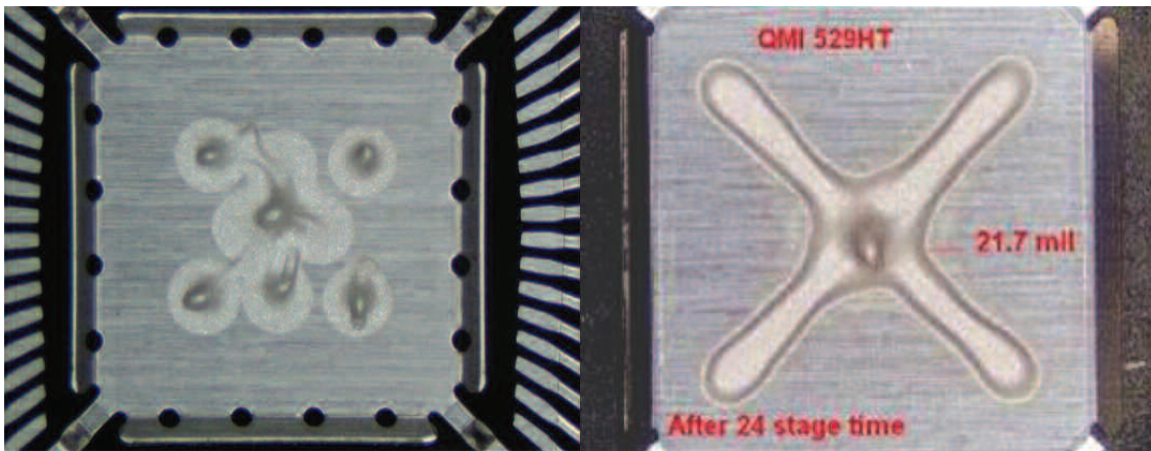
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can be stable at room temperature for applications where frozen storage and shipment cannot occur. However, these epoxies require higher curing temperatures. A quick curing epoxy might be necessary for high volume manufacturing. Low outgassing is necessary when engineers use epoxy die attach materials in hermetically sealed components as the outgassing can lead to moisture or hydrocarbon buildup. Low curing temperatures can help reduce stress in certain packaging systems. Engineers use UV curable epoxies for some optoelectronics applications where thermally-induced outgas byproducts can degrade optical performance. And low ionic impurities can reduce issues with ionic contamination in sensitive transistors.



The manufacturers ship fast cure die attach frozen in a syringe. The assembly engineers then let it thaw and use it. These materials have a floor life of 24 hours so they need to be used relatively quickly. There are also shelf stable epoxies that do not require refrigeration. These don't require mixing either, but they do need higher temperatures to cure. 250 to 300 degrees centigrade is common, so this may not be feasible for high volume manufacturing. The image above shows the general use of epoxies in high volume manufacturing. An operator inserts the epoxy syringe into the nozzle mechanism in the die attach machine. The system then uses pressure to dispense the epoxy onto the leadframe.

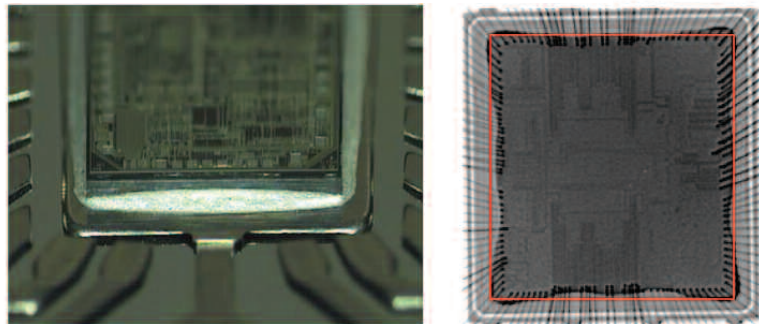
There are two methods for die attach dispense: the shower dispense and the writing dispense. For large dice, the writing pattern works better, but it takes longer to do in assembly. Most companies will use shower dispense on small dice, and a writing dispense on a larger die. The machinery can write various patterns onto the leadframe, similar to the way a dot matrix works. Fillet height is important, so the engineers program the machinery to control the fillet height to between 25 and 75% of the die height on the side of the die. After die attach dispense, one can use optical or x-ray imaging techniques to examine the coverage and the fillet.



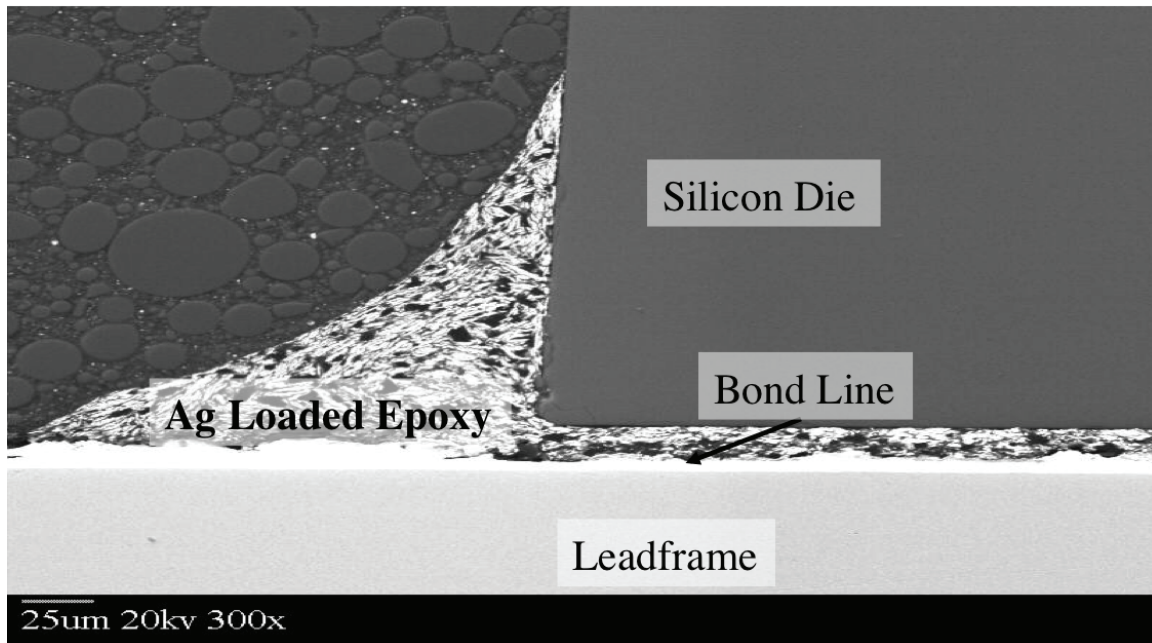
Shower Dispense

Writing Dispense

Can examine coverage with optical and x-ray imaging techniques



## Cross Section View



The image above shows a cross-sectional view of a proper die attach fillet. In a plastic package, the die is bonded to the die paddle, or the leadframe, using a silver-filled or silver-loaded epoxy. The silver flakes are the bright regions within the die attach. The die attach not only provides a mechanical connection between the die and the leadframe, but also provides an electrical connection. Problems can arise if there is insufficient silver in the epoxy, or if the silver becomes stratified. This can increase the resistance between the die and the leadframe. The silver-filled epoxy should also “wet” or make good contact to both the die and the leadframe. A good wetted epoxy contact will form a long smooth contact to the surface while a poor contact might ball up and have limited contact to the surface. This can occur as a result of poor cleaning processes, contamination, or low temperatures.

## Technical Tidbit

### T-Test

The next technique is the T-Test. The T-Test assesses whether the means of two groups are statistically different from each other. We use this analysis to compare the means of two groups. Explained in layman's terms, the T-Test determines a probability that two populations are the same with respect to the variable tested. For example, suppose we collected data on the heights of male basketball and football players, and compared the sample means using the T-Test. A probability of 0.4 would mean that there is a 40% likelihood that we cannot distinguish a group of basketball players from a group of football players by height alone. That's about as far as the T-Test—or any statistical test, for that matter—will work. If we calculate a probability of 0.05 or less, then we can reject the null hypothesis (that is, we can conclude that the two groups of athletes can be distinguished by height). We can perform the T-Test knowing just the means, standard deviation, and the number of data points. Note that the raw data must be used for the T-Test—or any statistical test, for that matter. If we record only the means, we lose a great deal of information and this usually renders our work invalid. The two sample T-Test yields a statistic *t*, in which the signal to noise ratio is given by the difference between the two group means divided by the variability of the two groups. We show some of the associated mathematics here as well.

$$\frac{\text{Signal}}{\text{Noise}} = \frac{\text{Difference between two group means}}{\text{Variability of groups}} = \text{ABS} \left( \frac{\mu_1 - \mu_2}{A \cdot B} \right)$$

$$A = \sqrt{\frac{1}{n_1} \div \frac{1}{n_2}} \quad B = \sqrt{\frac{(n_1 - 1) \cdot \sigma_1^2 + (n_2 - 1) \cdot \sigma_2^2}{n_1 + n_2 - 2}}$$

$\mu$  = mean  
 $\sigma$  = std. dev.  
 $n$  = # samples

The following Excel sheet shows an example of a T-Test calculation on propagation delay data. One calculates the means, standard deviations, and determines the number of samples in each group. One can then use the equations we discussed, or, one can use the Microsoft Excel formulas T.TEST and T.INV.2T to

	A	B	C	D	E	F	G	H	I	J	K	L	M	N
1			First Tester	Second Tester										
2			CLK_OUT Prop Delay	CLK_OUT Prop Delay										
3			1.2041	1.2046		Upper Limit	1.208	1.208						
4			1.2036	1.204		Lower Limit	1.2	1.2						
5			1.2058	1.2028		Min	1.2015	1.2023						
6			1.2026	1.2032		Max	1.2058	1.206						
7			1.2029	1.2052		Mean	1.203673841	1.204158968						
8			1.2026	1.2054		Std. Dev.	0.000982965	0.000925324						
9			1.2032	1.2051										
10			1.2029	1.2054		Sameness	0.999016892							
11			1.2033	1.2053										
12			1.2024	1.2046										
13			1.2026	1.203		No of Samples - 1st	840							
14			1.2042	1.2056		No of Samples - 2nd	1995							
15			1.2022	1.2056		Degrees of Freedom	2833		A =	$\sqrt{\frac{1}{n_1} \div \frac{1}{n_2}}$	$n_1$ = number of samples on first tester	$n_2$ = number of samples on second tester	$\sigma_1$ = standard deviation on first tester	$\sigma_2$ = standard deviation on second tester
16			1.2039	1.2054										
17			1.2033	1.2048		A (SX1X2)	0.041130637							
18			1.2021	1.205		B (S of X1,X2)	0.000942762							
19			1.2036	1.2043		T-Test (calc)	12.51088781							
20			1.2021	1.205										
21			1.202	1.2054		T-Test (Excel)	5.06373E-35		B =	$\sqrt{\frac{(n_1 - 1) \cdot \sigma_1^2 + (n_2 - 1) \cdot \sigma_2^2}{n_1 + n_2 - 2}}$				
22			1.2035	1.2059		T inverse (Excel)	12.5159849							
23			1.2045	1.2051										
24			1.2037	1.2035										
25			1.2041	1.2051										
26			1.2047	1.2058										
27			1.2029	1.203					T-Test =	$\text{ABS} \left( \frac{\mu_1 - \mu_2}{A \cdot B} \right)$	$\mu_1$ = mean of values on first tester	$\mu_2$ = mean of values on second tester		
28			1.2049	1.2047										
29			1.2056	1.2049										
30			1.2037	1.2029										

calculate the T-statistic and the confidence. The higher the T-statistic, the greater the likelihood that the two samples have come from the same two underlying populations that have the same mean. The T.INV.2T value gives us the probability that associated with the T-distribution. The equations actually generate the same value as the T.INV.2T function. In this example, the value for T.INV.2T is quite low, indicating that there is an extremely low probability that these samples come from different distributions. Another way to put it – these two samples likely come from the same distribution, or the machines used to produce this data are almost identical.

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### Ask the Experts

**Q: How can I make backside temperature measurements during RTP at multiple locations?**

**A:** There are two main methods for making temperature measurements during RTP: optical pyrometry and thermocouples. To make measurements at multiple locations, one would need multiple optical pyrometers, or multiple thermocouples. Another possibility with optical pyrometers is to mount the pyrometer such that it can be moved to focus on different areas, or use an infrared camera system to make a map. The challenge with optical pyrometry is that one must compensate for emissivity due to backside metallization schemes. Mounting of the optical pyrometer may also be problematical, as many detectors cannot be directly exposed to high temperatures.

## Spotlight: EOS, ESD, and How to Differentiate

### OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. Although EOS and ESD damage can at times look quite similar to each other, the source each and the solution can be quite different. Therefore, it is important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a two-day course that offers detailed instruction on EOS, ESD and how to distinguish between them. This course is designed for every manager, engineer, and technician concerned with EOS, ESD, analyzing field returns, determining impact, and developing mitigation techniques.

Participants learn to develop the skills to determine what constitutes a good ESD design, how to recognize devices that can reduce ESD susceptibility, and how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism.** Participants learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.
2. **Overview of the ESD Failure Mechanism.** Participants learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.
3. **ESD Circuit Design Issues.** Participants learn how designers develop circuits to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.
4. **How to Differentiate.** Participants learn how to tell the difference between EOS and ESD. They learn how to simulate damage and interpret pulse widths, amplitudes and polarity.
5. **Resolving EOS/ESD on the Manufacturing Floor.** Participants see a number of common problems and their origins.

### COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. Participants will understand the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. The seminar will identify the major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. Participants will be able to identify basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.
5. Participants will be able to distinguish between EOS and ESD when performing a failure analysis.
6. Participants will be able to estimate a pulse width, pulse amplitude, and determine the polarity of an EOS or ESD event.
7. Participants will see examples of common problems that result in EOS and ESD in the manufacturing environment.

## INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, written text material, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The course notes offer dozens of pages of additional reference material the participants can use back at their daily activities.

## COURSE OUTLINE

### Day 1

1. Introduction
  - a. Terms and Definitions
  - b. ESD Fundamentals
  - c. EOS Fundamentals
2. Electrical Overstress Device Physics
  - a. Sources of EOS
  - b. EOS Models
  - c. Electrothermal Physics
3. Electrostatic Discharge Device Physics
  - a. ESD Models
  - b. ESD Testing and Qualification
  - c. ESD Failure Criteria
  - d. Electrothermal Physics
  - e. Electrostatic Discharge Failure Models
  - f. Semiconductor Devices and ESD Models
  - g. Latchup
4. EOS Issues in Manufacturing
  - a. Charging Associated with Equipment
    - i. Testers
    - ii. Automated Handling Equipment
    - iii. Soldering Irons
  - b. Charge Board Events
  - c. Cable Discharge Events
  - d. Ground Loops/Faulty Wiring
  - e. Voltage Differentials due to High Current
  - f. Event Detection



## Day 2

5. ESD Protection Methods
  - a. Semiconductor Process Methods
  - b. MOSFET Design
  - c. Diode Design
  - d. Off-Chip Drivers
  - e. Receiver Networks
  - f. Power Clamps
6. Differentiating Between EOS and ESD
  - a. EOS Manifestation
  - b. ESD Manifestation
  - c. Circuit considerations
    - i. Chip level
    - ii. System level
  - d. Simulating ESD
  - e. Simulating EOS
7. EOS/ESD Design and Modeling Tools
  - a. Electrothermal Circuit Design
  - b. Electrothermal Device Design
  - c. ESD CAD Design

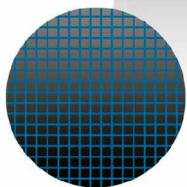
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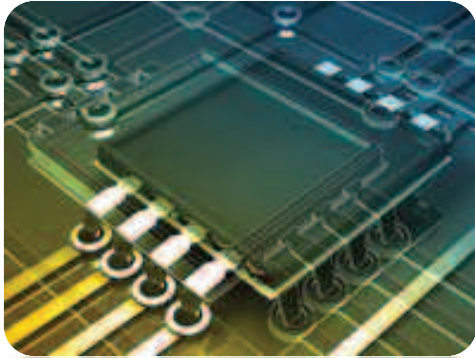
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**Chris Henderson, IRPS General Chair**

**Chris would be happy to meet with you and discuss any training needs you have.**

**Contact him at [henderson@semitracks.com](mailto:henderson@semitracks.com) during the symposium!**



## Upcoming Courses

(Click on each item for details)

### Failure and Yield Analysis

May 17 – 20, 2016 (Tue – Fri)  
Munich, Germany

### EOS, ESD and How to Differentiate

May 23 – 24, 2016 (Mon – Tue)  
Munich, Germany

### Semiconductor Reliability / Product Qualification

May 30 – June 2, 2016 (Mon – Thur)  
Munich, Germany

### Advanced Thermal Management and Packaging Materials

June 7 – 8, 2016 (Tue – Wed)  
Albuquerque, New Mexico, USA

### Wafer Fab Processing

June 27 – 30, 2016 (Mon – Thur)  
San Jose, California, USA

### Semiconductor Reliability

July 11 – 13, 2016 (Mon – Wed)  
Singapore

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## Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us ([info@semitracks.com](mailto:info@semitracks.com)).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email ([jeremy.henderson@semitracks.com](mailto:jeremy.henderson@semitracks.com)).

We are always looking for ways to enhance our courses and educational materials.

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*To post, read, or answer a question, visit our [forums](#).  
We look forward to hearing from you!*