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InfoTracks

Semitracks Monthly Newsletter

Chemical Vapor Deposition Basics Part 1

By Christopher Henderson

This month we will begin a two-part series that provide an overview of chemical vapor deposition and the basic principles behind the technique. Process engineers usually refer to chemical vapor deposition by its short name CVD so we will refer to it that way as well.

Probably the commonly used technique for deposition is chemical vapor deposition or CVD. CVD is a highly versatile method for depositing a wide variety of materials. It is a process that deposits a solid film on a heated substrate by reacting vapor-phase chemicals. One can use CVD to deposit epitaxial silicon, polysilicon, a variety of oxide layers, metal layers, barrier metals, and silicides.

Let's describe the generic CVD process. The system introduces the reactant gases into the reaction chamber, and the gases diffuse through the boundary layer to the wafer surface. The reactants adsorb on the wafer surface. Once they do so, the reactants are now referred to as adatoms. The adatoms migrate to the growth sites, where they react and add to the film being formed. These reactions create a solid film and gaseous by-products, and these reactions may be the result of pyrolysis, reduction or oxidation. The gaseous by-products then desorb from the surface and diffuse through the boundary layer into the gas flow, where they are exhausted.

The basic idea behind chemical vapor deposition is rather simple: we react chemicals on the surface to grow a desired layer. For the purposes of this discussion let's assume the CVD chemicals we

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are considering are gases. Of course, there are many complicating details. These include the gas transport to the wafer surface, the gas phase reactions, the gas adsorption onto the surface, the mobilities of the precursors used on the surface, the reaction of the precursors, whether they be surface or gas-phase reactions, the reaction byproducts, the byproduct desorption, and the byproduct transport away from the wafer surface. Each of these can affect the growth rate, the uniformity and the purity of the deposited layer.

As thin films grow, they follow the Gibbs free energy principle. The free energy rule states that the total free energy of a system decreases with increasing size of particles. This leads to the growth pattern described above. First, particles nucleate. Next, the individual nuclei grow. As they increase in size, the individual nuclei begin to impinge on each other. The overall system lowers the free energy through coalescence. As growth continues, the remaining area forms channels, which slowly fill in, leaving holes, which are the last to close up.

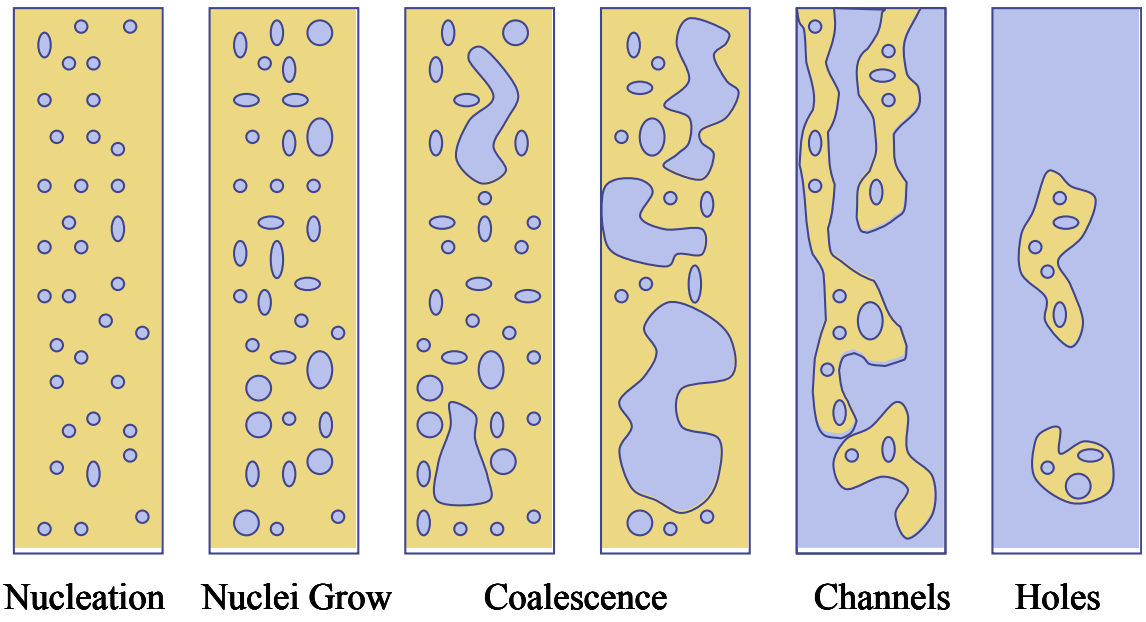
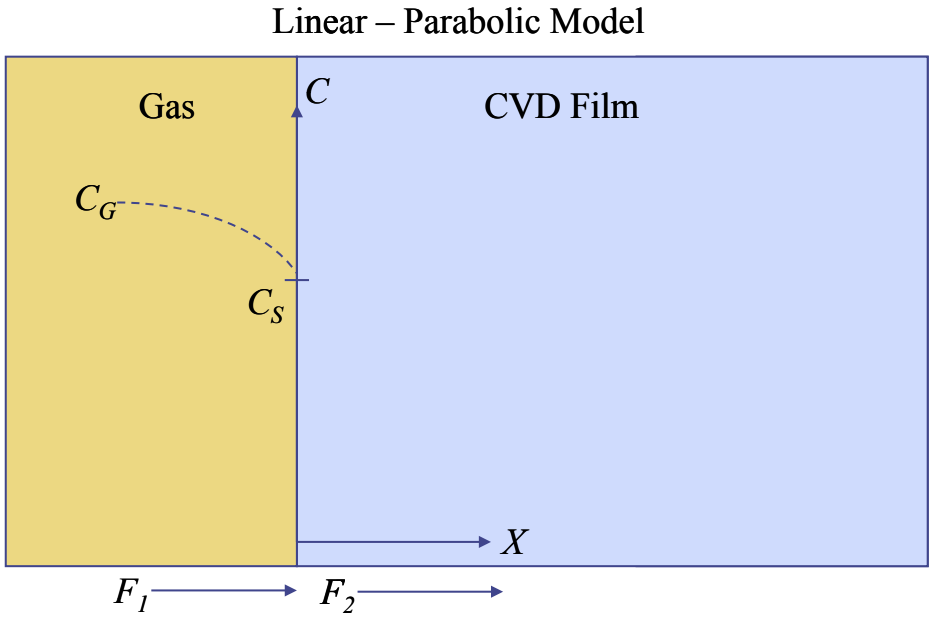


Figure 1. Diagram showing the basic chemical vapor deposition process.

In chemical vapor deposition there are two types of reactions: heterogeneous and homogeneous. In a heterogeneous reaction, the reaction occurs on or very close to the wafer surface. This is preferred since the reactions occur selectively on the heated surfaces. In a homogeneous reaction, the reaction occurs in the gas phase. This is undesirable since it results in sold particles of material falling down onto the film.

The best way to model the CVD process is through the Deal-Grove Model. This model is named after Andrew Grove, the famous leader of Intel, and Bruce Deal, a research colleague of his, and has been around since the late 1960s. Before we show the equations, we need a few basic terms and assumptions. The five steps of the CVD process we mentioned two slides back can be grouped as gas phase and surface processes. In each group, one step will be the rate-limiting step. Grove described these processes in terms of flux *F,* where flux units are atoms per square centimeter second. This term is used both for transport and reaction flux.

The Deal-Grove model is also used for oxidation, but we will show how it is used to model the CVD reaction process. The concentration distribution of the reactant gas and the flux from the bulk of the gas to the surface is given by F_1. F_2 corresponds to the flux or the consumption of the reactant gas. In this model, F_1 is equal to the gas phase mass transfer coefficient times the difference between the reactant concentration in the gas (C_G) and the reactant concentration at the surface (C_S).



F_1 – flux of reacting species moving from gas to gas-Film interface
F_2 – flux of reacting species diffusing through existing Film interface

$$F_1 = h_G\left(C_G - C_S\right)$$

Figure 2. The Deal-Grove model, expressed graphically.

The Deal-Grove model leads to two film growth regimes, a mass transport-limited regime and a surface reaction rate-limited regime. The mass transport-limited regime dominates at higher temperatures, and the growth rate is only a weak function of temperature. In this regime, the reaction rate is fast enough to use all of the incoming and available reactants, so the flux of the reactants is the key process control parameter. The surface reaction rate-limited regime dominates at lower temperatures. Here the growth rate is a strong function of temperature, since the reaction rate is governed by temperature.

Next month, we will cover the second part of chemical vapor deposition.

Technical Tidbit

Injection Induced Breakdown Voltage (BV_{ii})

A parameter associated with snapback is Injection Induced Breakdown Voltage, or BV_{ii}. BV_{ii} is a good monitor parameter for snapback, since it encompasses the effects of the current gain of the parasitic bipolar transistor, the avalanche multiplication factor, and the effective substrate resistance. Changes to these three values will affect BV_{ii}, and therefore give an indication of a transistor's susceptibility to snapback. One of the challenges with BV_{ii} is the gate voltage at which one should take the measurement. Historically, measuring BV_{ii} at $V_G = 0.5*V_D$ worked well, since snapback tends to occur in the saturation condition. With smaller feature sizes, that may change as the maximum in hot carrier injection moves more toward $V_G = V_D$. This graph shows an example of both a good (green) snapback curve, and a poor (red) snapback curve. We also point out where BV_{ii} lies on the plot.

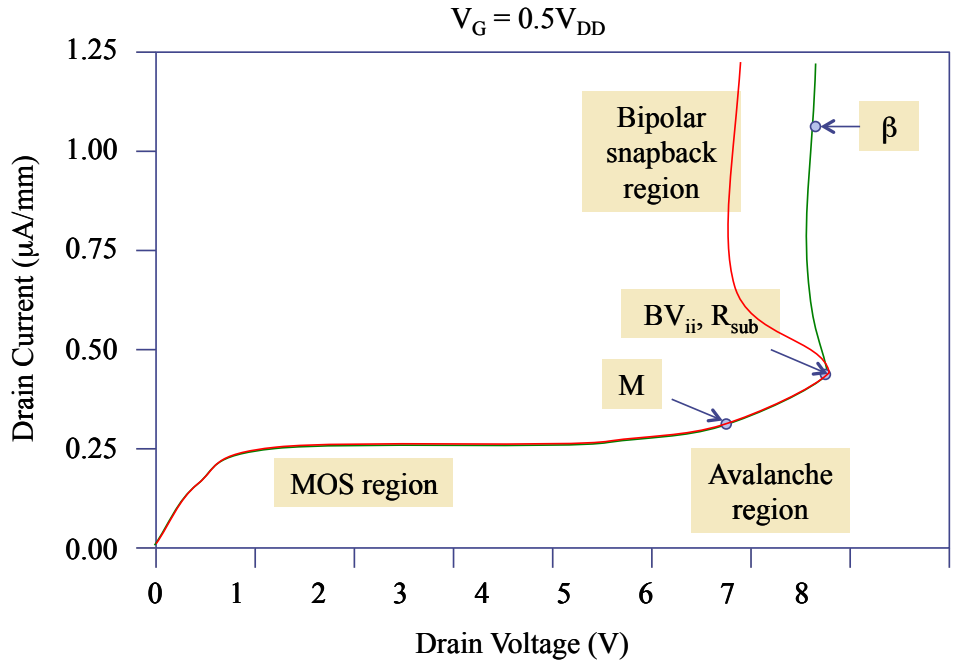


Figure 1. I_D versus V_D curve showing the snapback behavior of an NMOS transistor. The green curve represents robust transistor design/processing, while the red curve represents a poor transistor design/processing for snapback.

A good paper to read concerning process effects on BV_{ii} is "ESD-related Process Effects in Mixed-voltage Sub-0.5mm Technologies" by Vikas Gupta, Ajith Amerasekera, Sridhar Ramaswamy, and Alwin Tsao. You can find this paper in the the 1998 EOS-ESD Symposium Proceedings start on page 161.

Spotlight on our Courses: Advanced Failure And Yield Analysis

We will be offering our Failure and Yield Analysis Course in Munich, Germany, May 13 – 16, and in Penang, Malaysia, July 1 – 4. Here is information on the course. If you are interested in further information, please feel free to contact us at (505) 858-0454, or at info@semitracks.com.

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a two-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy

8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).

Semitracks will be present at the 2013

IEEE International Reliability Physics Symposium

April 14 – 18, 2013

Hyatt Regency Monterey Resort & Spa • Monterey, California

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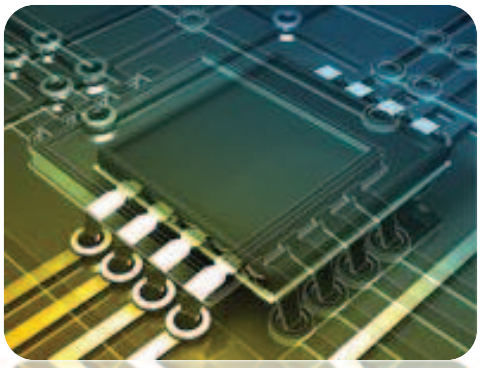

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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For more information on Semitracks online training or public courses, visit our web site!

http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Photovoltaics Reliability (co-sponsored by SEMI)
April 18, 2013 (Thurs)
San Jose, California

Advanced Thermal Management and Packaging Materials
April 22 – 23, 2013 (Mon – Tues)
Philadelphia, Pennsylvania

Semiconductor Reliability
May 6 – 8, 2013 (Mon – Wed)
Munich, Germany

Copper Wire Bonding Technology and Challenges
May 13 – 14, 2013 (Mon – Tue)
Munich, Germany

Failure and Yield Analysis
May 13 – 16, 2013 (Mon – Thur)
Munich, Germany

MEMS Technology
May 15 – 16, 2013 (Wed – Thurs)
Munich, Germany

IC Packaging Design and Modeling
May 27 – 29, 2013 (Mon – Wed)
Penang, Malaysia

Semiconductor Reliability
June 26 – 28, 2013 (Wed – Fri)
Penang, Malaysia

Failure and Yield Analysis
July 1 – 4, 2013 (Mon – Thur)
Penang, Malaysia