SEMITRACKS, INC.

ISSUE 159
SEPTEMBER
2022

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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This month, we begin a new series of Feature Articles on cleanroom technology. Cleanroom technology is essential to the successful fabrication of all integrated circuits and semiconductor components. When most engineers think about wafer fab processing equipment, they don't always think about the infrastructure needed to support the chip fabrication. The cleanroom is the fundamental piece of infrastructure technology required for chip fabrication. In the next several Feature Articles, we will cover various aspects of this topic. In this month's Feature Article, we will provide an overview of Semiconductor Cleanroom Technology.

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WHAT'S INSIDE?

Want to take control of your learning? See Page 7

UPCOMING WEBINARS:

Wafer Fab Processing

IC Packaging Design and Modeling Course

See page 11 for more details

At the beginning, let's define what we mean by a cleanroom. According to ISO 14644-1, a cleanroom is "a room in which the concentration of airborne particles is controlled, and which is constructed and used in a manner to minimize the introduction, generation, and retention of particles inside the room, and in which other relevant parameters (e.g., temperature, humidity, and pressure) are controlled as necessary." Engineers create a cleanroom environment through the use of appropriate HVAC (Heating, Ventilation, Air Conditioning) systems and HEPA (High Efficiency Particulate Air) filters that maintain the correct pressurization, temperature, and humidity of the cleanroom, as well as the air flow of the circulating and continuously filtered air. Since cleanrooms are atmospherically isolated from the external environment, engineers provide them with special passageways to allow the transport of people and materials to and from them. 'Air showers' and 'pass-through windows' are the major modes of transfer between cleanrooms and the outside environment. Historically, cleanrooms were classified by particle numbers and sizes through Federal Standard 209E, but this has been replaced by ISO 14644-1. We will have more to say about this in a moment. Cleanrooms can range from Class 10,000, which is only slightly better than standard office conditions, to better than Class 1, which is an environment that is free from almost any particulate in the air. Most modern integrated circuit wafer manufacturing requires a Class 1 cleanroom.

Cleanrooms were originally classified in terms of the number and sizes of particles suspended in its atmosphere. A particle is defined as a solid or liquid object between 0.001 and 1000 μm in size. Table 1 shows the various cleanroom classes and their corresponding statistically allowable number of particles per cubic foot of air, as defined by the historical document that contained Federal Standard 209E. To illustrate, in a Class 100 cleanroom, a cubic foot of air is only allowed to have 100 particles whose size is 0.5 μm.

Class Name	0.1 µm	0.2 µm	0.3 µm	0.5 µm	5 µm
1	35	7.5	3	1	N/A
10	350	75	30	10	N/A
100	N/A	750	300	100	N/A
1000	N/A	N/A	N/A	1000	7
10000	N/A	N/A	N/A	10000	70
100000	N/A	N/A	N/A	100000	700

Table 1- Old cleanroom classification technology, as defined in Federal Standards 209E

Table 2 shows the current cleanroom classification technology, as defined in ISO 14644-1. We show the older Federal Standard equivalent in the right-hand column for reference.

ISO 14644-1 Cleanroom Standards							
Classification	Maximum Particles/m^3						FED STD 209E Equivalent
	≥0.1µm	≥0.2µm	≥0.3µm	≥0.5µm	≥1µm	≥5µm	
ISO 1	10	2.37	1.02	0.35	0.083	0.0029	
ISO 2	100	23.7	10.2	3.5	0.83	0.029	
ISO 3	1,000	237	102	35	8.3	0.029	Class 1
ISO 4	10,000	2,370	1,020	352	83	2.9	Class 10
ISO 5	100,000	23,700	10,200	3,520	832	29	Class 100
ISO 6	1.0×10^6	237,000	102,000	35,200	8,320	293	Class 1,000
ISO 7	1.0×10^7	2.37×10^6	1,020,000	352,000	83,200	2,930	Class 10,000
ISO 8	1.0×10^8	2.37×10^7	1.02×10^7	3,520,000	832,000	29,300	Class 100,000
ISO 9	1.0×10^9	2.37×10^8	1.02×10^8	35,200,000	8,320,000	293,000	Room Air

Table 2- Current cleanroom classification technology, as defined in IS0 14644-1

In semiconductor manufacturing, wafer fab processes usually require an ISO 3 or ISO 4 cleanroom, while assembly processes prior to encapsulation of the die require an ISO 7 cleanroom. An ISO 8 cleanroom is all that post-encapsulation assembly and test processes typically require.
Let's say a few words about the history of the cleanroom. Willis Whitfield invented the cleanroom in 1962 at Sandia National Laboratories. To solve problems of dust particles causing reliability and quality issues with nuclear weapon components, Whitfield envisioned a room that blew air in from the ceiling and sucked it out from the floor, allowing the air to move at a constant, steady rate. Filters scrubbed the air before it entered the room and gravity helped any remaining particles exit. When he tested his cleanrooms, particle detectors started showing numbers so low that many did not believe his claims. Whitfield's design made it possible to standardize cleanrooms across the government research divisions found in such agencies as the Department of Defense, the Department of Energy, and NASA. Cleanrooms have also been instrumental in the research and development that has produced much of the technology that surrounds us. They are essential for the manufacture of many products such as computer chips, photovoltaics, and microelectromechanical systems.

In order to build a properly functioning cleanroom for high volume manufacturing, companies must make enormous investments. Although trade magazines and news articles use numbers like US$10 Billion Dollars to build a chip factory, this includes the cost of the equipment. However, the cost of the cleanroom is still a significant portion of this cost.

For a US$10 Billion Dollar chip factory, the cost of the building and cleanroom technology can be upwards of US$1 Billion. Figure 1 shows a photograph of the Samsung Hwaesong Fab complex in South Korea nearing completion of construction in 2019. The cost of this chip fab is on the order of US$10 Billion Dollars, so the investment in cleanroom technology is approximately US$1Billion Dollars.

Figure 1- The Samsung Hwaesong Fab complex in South Korea, nearing completion in 2019

In next month's Feature Article, we will discuss contamination, and how cleanroom technology assists with contamination control.

Technical Tidbit: Vacuum Systems and Outgassing

This month's Technical Tidbit covers vacuum systems and outgassing. Outgassing is a challenge to creating and maintaining clean high-vacuum environments.

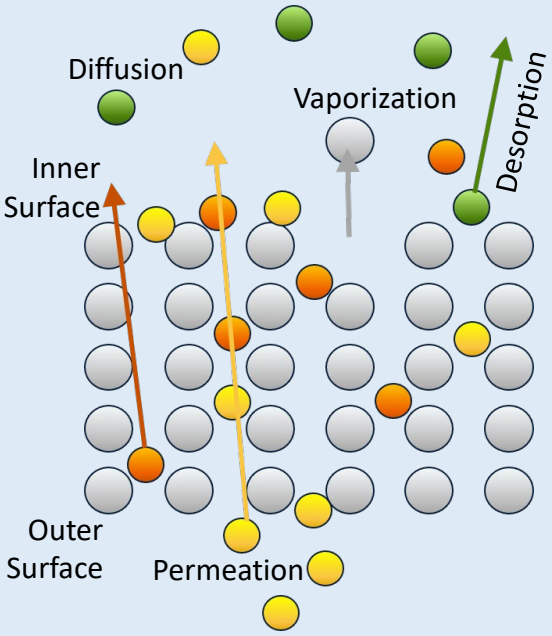

Figure 1- Diagram illustrating the 4 main mechanisms that contribute to outgassing

Figure 1 shows the sources of atoms and molecules that comprise an outgassing flow. Outgassing products can condense onto optical elements, thermal radiators, or solar cells and obscure them. Materials not normally considered absorbent can release enough light-weight molecules to interfere with industrial or scientific vacuum processes. Moisture, sealants, lubricants, and adhesives are the most common sources, but even metals and glasses can release gases from cracks or impurities. This is also important when it comes to semiconductor manufacturing chambers. The rate of outgassing increases at higher temperatures because the vapor pressure and rate of chemical reaction increases. For most solid materials, the method of manufacture and preparation can reduce the level of outgassing significantly. Cleaning of surfaces, or heating of individual components or the entire assembly (a process called "bake-out") can drive off volatiles.

There are 4 main mechanisms which contribute to outgassing (shown in Figure 1):

1. Vaporization — this is the removal of the actual surface material itself (in metals, this is negligible at typical operating temperatures)
2. Desorption — this is the reverse process of adsorption; the release of molecules bound at the surfaces of the chamber and internal fixtures
3. Diffusion — this is the movement of molecules from the inner structure of the material to the surface
4. Permeation — this is the movement of molecules from the external atmosphere through the bulk to the vacuum surface

The extent to which each of these affect outgassing depends on the composition of both the gas and the surface material (and the previous environment in which the surface material has been). Outgassing rates are a sum of these contributions.

Ask The Experts

Q: What is a WAP ring?

A: WAP stands for Wafer Area Pressure. WAP rings are typically used in plasma processing chambers and provide improved wafer area pressure control. The WAP ring is basically a confinement ring which defines an area above a wafer. The wafer area pressure is dependent on the pressure drop across the confinement ring. The confinement ring is part of a device that provides wafer area pressure control for more uniform etching or plasma-enhanced chemical vapor deposition.

Course Spotlight: IC Packaging Design and Modeling

We will be hosting this course in an upcoming webinar. For more information, see page 11 for dates and times. We hope to see you there!

COURSE OBJECTIVES

With focused guidance from your instructor, you will gain insight into the following:

1. An in-depth understanding of semiconductor packaging design and its technical issues.

2. Understanding the basic concepts behind thermal and mechanical simulations of packages.

3. Identifying the key issues related to the continued growth of the semiconductor industry. This includes the need for high power dissipation, and designs that can mitigate the increasing fragility of the die because of low-k dielectrics.

4. You'll see a wide variety of sample modeling problems to solve in class, to gain a hands-on knowledge of the fundamentals of packaging modeling.

5. Identifying basic and advanced principles for mechanical stress and thermal diffusion.

6. Understanding how package reliability, power consumption and device performance relate to each other.

7. Learning to make decisions about packaging construction and strategies for evaluating new packaging designs and technologies.

8. You will also be introduced to wafer level simulations; an increasingly necessary skill with the advent of low-k dielectrics.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor packaging and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field.

OVERVIEW

Semiconductor and integrated circuit technology continues to develop at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The industry is also pushing to use semiconductor devices in an increasing array of applications. To accomplish this, the industry is also driving prices down. This has created a number of challenges related to the packaging of these components.

IC Packaging Design and Modeling is a three day course that offers thorough instruction on the design and modeling of semiconductor packages. We place special emphasis on package interactions with the die. This course is essential for every manager, engineer, and technician who works in semiconductor packaging, using semiconductor components in high performance applications or nonstandard packaging configurations, or supplying packaging tools to the industry.

By focusing on the fundamentals of packaging design and modeling, you'll learn why advances in the industry are occurring along certain lines and not others. Our instructors clearly explain semiconductor packaging without delving heavily into the complex physics and materials science that normally accompany this discipline. You'll learn basic but powerful aspects about the semiconductor packaging. This skill-building series is divided into four segments:

1. **Packaging Design Overview.** Learn the fundamentals of packaging design, and why modeling has become critical to semiconductor packaging for today's designs.

2. **Mechanical Simulations.** Learn the fundamentals of displacement, strain, stress, and energy. You'll be able to leverage St. Venant's Principle and apply fracture mechanics to a problem.

3. **Thermal Simulations**. Learn heat transfer modeling, and steady-state and transient thermal modeling. The instructor also explains industry standard and compact thermal models.

4. **Modeling Semiconductor Packages.** Learn about the software used for modeling a variety of aspects of semiconductor packaging. You'll also see a number of examples using current modeling tools used by Package Design experts.

COURSE OUTLINE

1. Package Design Principles
    a) Background
    b) ITRS Roadmap Issues
    c) JEDEC Standards for Packaging
    d) Semiconductor Package Designs: What is a Good Packaging Design?
    e) Modeling Software
2. Assembly and Packaging Processes
    a) Assembly and Packaging Processes
    b) Selecting Package Materials
    c) Advanced Packaging
    d) Stacked Die & Stacked Packages
    e) Through Silicon Via (TSV) Interconnects
3. Stress Simulations
    a) Solid Mechanics Concepts
        i. Basics of Displacement, Strain, Stress and Energy
        ii. Leveraging St. Venant's Principle
        iii. Applying Fracture Mechanics
    b) Manufacturability
        i. Thermomechanical Modeling Metrics
        ii. To Model or Not to Model
        iii. Assembly Process Simulations
4. Thermal Simulations
    a) Heat Transfer Principles
    b) JEDEC Thermal Test and Simulations
    c) SteadyState and Transient Thermal Modeling
    d) Application Specific Thermal Simulations
    e) Using Compact Thermal Models
7. Reliability and Coupled Mechanics
    a) Thermomechanical Reliability
        i. Solder Joint Reliability (SJR)
        ii. Single Chip & Multiple Chip Package SJR
        iii. Solder Joint Shape Predictions
    b) Coupled Mechanics
        i. Moisture Diffusion
        ii. Plastic Package "Popcorn" Cracking
8. WaferLevel Simulations
    a) Venturing into New Territory (Submodeling)
    b) ChipPackage Interactions
        i. Interfacial Fracture Mechanics
        ii. Bridging IC Interconnect and Package Gaps
    c) Microelectromechanical Systems (MEMS)
        i. Device Operations
        ii. MEMS Packaging
9. Drop Tests Simulations
    a) Drop Test & Structural Dynamics
    b) Solder Selection & Performance
        i. Leaded Solders
        ii. LeadFree Solders
        iii. Surface Finishes, Solder Pastes, & Metallization
    c) Package Design Effects
        i. Stand-Off Heights
        ii. Ball Array Pattern
        iii. Single Chip & Multiple Chip Packages

Upcoming Webinars:

Wafer Fab Processing WEBINAR
4 Sessions of 4 Hours each
US: October 3 - October 6, 2022 (Mon - Thurs), 8:00AM - 12:00Noon PDT
Visit: https://www.semitracks.com/courses/processing/wafer-fab-processing.php

IC Packaging Design and Modeling WEBINAR
4 Sessions of 4 Hours each
US: October 10 - October 13, 2022 (Mon - Thurs), 8:00AM - 12:00Noon PDT
Visit: https://www.semitracks.com/courses/packaging/ic-packaging-design-and-modeling.php

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!