Issue 147 September 2021

InfoTracks

Semitracks Monthly Newsletter

Semitracks—20 Years

By Christopher Henderson

This month, we start our 3rd decade of operation, so I thought it might be interesting to our customers and followers to give you an overview of all that has transpired over the last 20 years of our operation.

Early Years

Semitracks was the result of discussions between myself (Chris Henderson), Dan Barton, Ed Cole and Tom Moore. Early in my career at Sandia National Laboratories, my manager at the time (Rich Anderson) told me that I should be involved in a research project related to our group's activities in semiconductor failure analysis. He suggested looking into AI techniques to help guide the failure analysis process. It sounded interesting to me so I dove into the project while waiting for a security clearance to come through. I initially looked into Expert System technology to do this, and developed an expert system that provided basic guidance. This work was published at the International Reliability Physics Symposium (IRPS) in 1991, and generated quite a bit of interest. Several companies approached me to further develop the concept, including Intel and Schlumberger Technologies (this group is now part of Thermo Fischer Scientific). We developed the concept to include integration with CAD and knowledge libraries to help guide fault isolation of integrated circuits. We presented our work at IRPS in 1994.

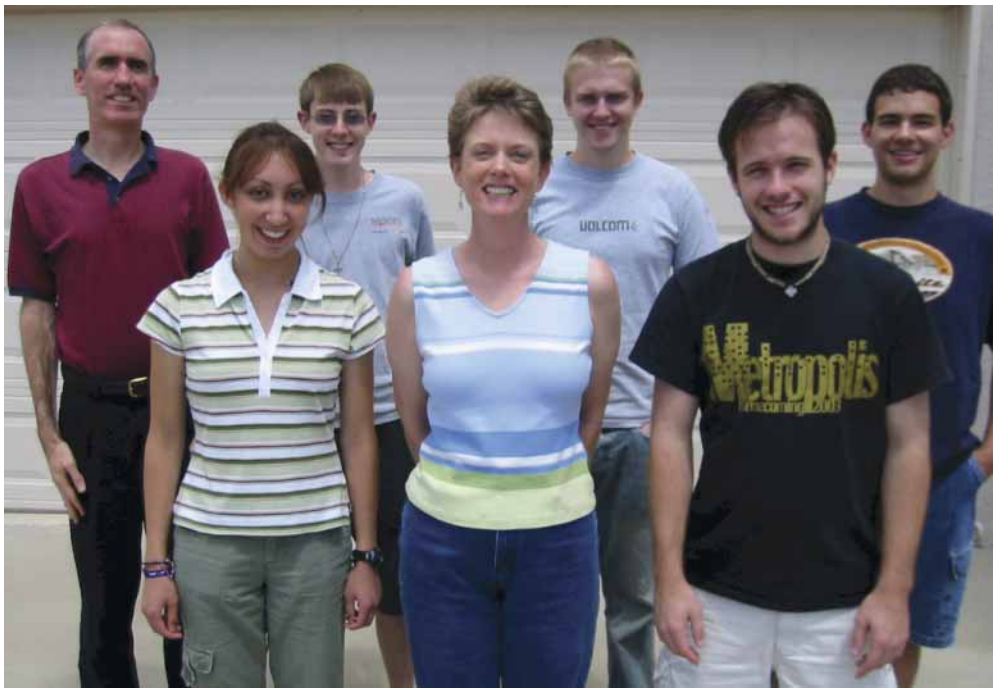
In this Issue:

During this timeframe, the World Wide Web began to take shape. At Sandia, we took a portion of the joint Sandia/Schlumberger work and turned it into an online library that could be accessed through this new medium. Tom Moore (working then as a manager at Texas Instruments) and I had several conversations about the usefulness of this work. He encouraged me to continue to work on this idea, as many people would find this to be beneficial to their learning. This work later became the foundation of the "Reference Materials" on Semitracks' website.

A few years later, Dan, Ed, and I had the opportunity to teach a failure analysis course through Sandia to outside companies. This course was successful, and we received additional requests to do the course again. During this timeframe, Sandia was heavily involved in Technology Transfer and Commercialization, so we received permission to run the course through an outside entity, Analytical Solutions (now part of Integra Technologies). Over a two-year period, we held the course at several locations in the United States and the United Kingdom. By 2001, we believed that there was sufficient demand that the concept could be expanded to multiple courses and become a viable business. In June and July of 2001 Dan, Ed, Tom, and I had meetings with venture capital firms. One of those firms (Ardesta, then headed by Rick Snyder – the former governor of Michigan) was excited and ready to invest in our idea. We incorporated Semitracks, Inc. on August 6, 2001. Then "9/11" happened…

A Change in Direction

The collapse of the World Trade Centers and the subsequent travel restrictions brought our training courses to a standstill. Even after air travel resumed, many companies would not allow their employees to travel, and still others were scared to travel. It wasn't until 2003 that we were able to hold our next course. In parallel, the environment at Sandia changed from a focus on Technology Transfer to Defense and Homeland Security. Sandia was no longer supportive of outside interactions. Sandia disengaged with Ardesta, and the opportunity for funding disappeared. This change eventually led to Sandia giving us an ultimatum – either work for Sandia full-time, or leave to do Semitracks full-time. Dan and Ed decided to remain at Sandia. Tom was then involved with his own start-up (Omniprobe), so he decided to pursue that opportunity full-time. I decided to move ahead and bought out the other shareholders. I left Sandia on Friday, November 13, 2004, and started my full-time career at Semitracks on Saturday, November 14 at our booth at the International Symposium for Testing and Failure Analysis (ISTFA) in the Boston area.



Semitracks Staff Photo in 2006.

Growing the Business

In 2005, Semitracks began to increase its course offerings. We held courses in Germany for the first time, as well as Singapore. Later that year, we introduced our Online Training System. Initially, the system was focused on training around failure analysis and reliability, but over the next few years, we increased our online training content to include training on wafer fab processing, packaging, failure mechanisms, quality, and other technology topics. We formed a partnership with Semiconductor International, the leading semiconductor trade magazine at the time, and jointly held courses. By 2008, Semitracks was running courses in the United States, Israel, SE Asia, and multiple countries in Europe. Even though the economy in the US was beginning to struggle from the effects of the housing bust, Semitracks' global presence helped shield it from the effects, for a while…

The Financial Crisis and Recovery

On September 15, 2008, Lehman Brothers declared bankruptcy, and the world's financial system "locked up", for lack of a better term. Quickly, our customers clamped down on their spending and cancelled future courses. By November, Semitracks was no longer holding any courses. The next six months were bleak – everyone was afraid to do any business for fear of spending cash they needed for basic operations. We sat down as a company and seriously debated whether we should continue operating Semitracks. In the end, we decided to press ahead. It wasn't until the summer of 2009, when

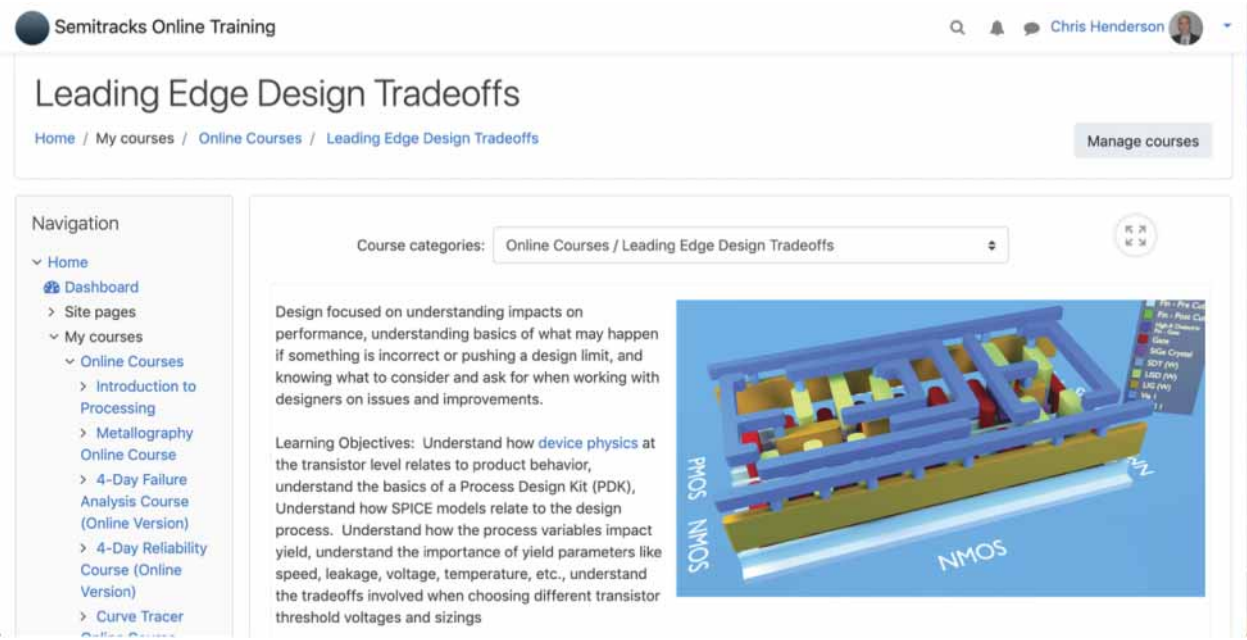
US Federal Reserve had stepped in to stabilize the financial system, did companies begin to have confidence to spend on training. Business for 2009 was only 50% of what it was the previous year. By 2010, business was doing better, and we began to re-build our customer base and hold public courses. During the next several years, Semitracks developed partnerships with several large semiconductor firms which helped provide more stability to the business.

Semitracks Reliability Course offering at Semicon West in 2007

The COVID-19 Pandemic and Transformation

At the beginning of 2020, business was strong; we were coming off of two of our best years as a company, and had high hopes for the year, until Covid-19 struck. The pandemic and ensuing lock-downs wreaked havoc on our business. At the beginning of 2020, approximately 70% of our business was in-person training, and 30% was virtual (webinars and self-paced online training). We had to cancel all of our public courses, and our customers quickly stopped their in-house courses, leaving only webinars and self-paced online training. We made some painful decisions to scale back our workforce, and re-focus our business around virtual training (webinars and self-paced online training). Fortunately, our customers were thinking along the same lines, and in some cases, engaged us to help them with the transformation from in-person courses to virtual courses. As of this writing, all of our business is now virtual, but hasn't grown enough to completely fill the gap left by the lack of in-person training. As part of this

transformation, we also made the decision to move the business to Arizona to be closer to some of our key customers, should future lock-downs occur. That way, we would still potentially be able to see some of our customers in person. We are hopeful that we can fill the remaining portion of the gap left by a lack of in-person training with virtual training. We are not sure if and when in-person training will return. If it does, we are prepared to offer in-person courses, and if it doesn't, we will continue to offer virtual courses.



Self-paced training through the Semitracks Online Training System

Technical Tidbit

MEMS Pressure Sensors

This month's Technical Tidbit covers MEMS Pressure Sensors. Microelectromechanical Systems, or MEMS, are now quite common in sensor applications, and pressure sensing is an important application where the sensor must be small and low power.

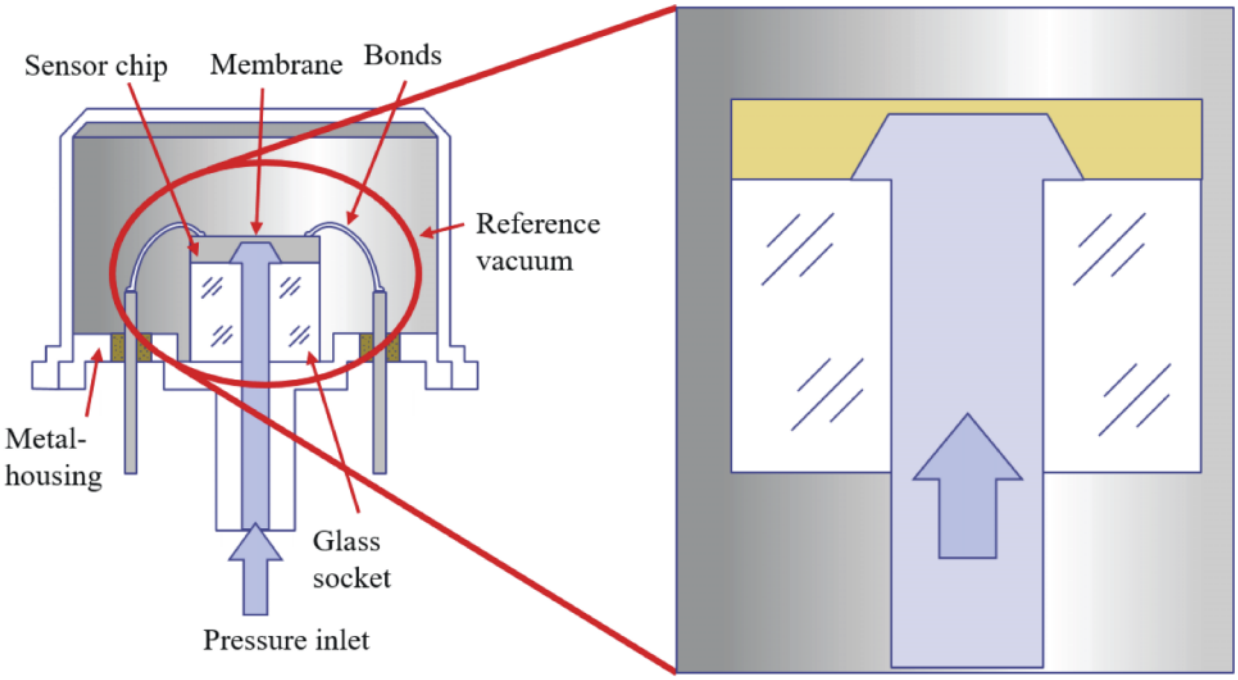


Figure 1. Cross-section View of a MEMS Pressure Sensor.

Pressure sensors are a common type of sensor in many applications; for example, tire pressure is an important automotive application. Pressure sensors can also be easily fabricated using MEMS processes. Figure 1 shows the working principle behind a pressure sensor. The sensor itself is a semiconductor chip mounted in a sealed package, typically made from metal, like a Transistor Outline, or TO-style, metal can. The pressure inside of the can is typically quite low, providing a reference vacuum level on one side of the sensor. There is an opening in the bottom of the TO-package to allow an outside pressure to make contact to the other side of the sensor. The sensing element is a thin membrane of semiconductor material with piezoresistive properties that can be measured. Wire bonds connect the two ends of the electrical connections on the membrane to the outside of the package. The membrane is thin and will flex with changes in pressure, causing changes in resistivity that can be detected.

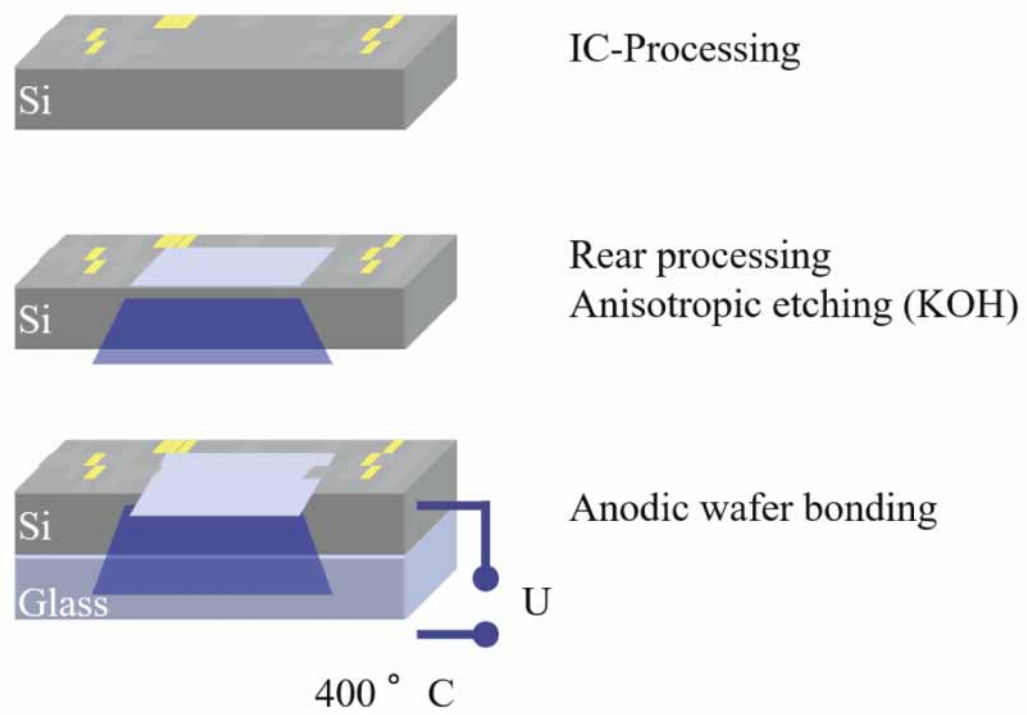


Figure 2. Steps Involved in Creating a Silicon-based MEMS Pressure Sensor .

Engineers manufacture this type of sensing element using bulk micromachining technology, as shown in Figure 2. First, the engineers create the integrated circuit elements using traditional fabrication processing. Next, they flip the wafer over and perform an anisotropic etch using potassium hydroxide to create the thin membrane. Finally, they apply a glass layer to the back side of the wafer and use anodic bonding to complete the sensor structure.

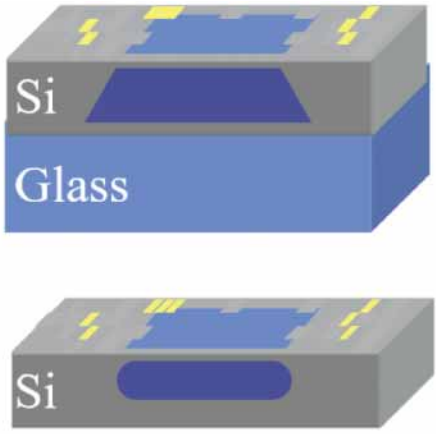


Figure 3. (Top) Traditional Silicon-based MEMS Pressure Sensor;
(Bottom) Surface Micromachined Silicon-based MEMS Pressure Sensor.

Although engineers commonly use the traditional bulk micromachining approach to create pressure sensors, this approach does require a wafer bonding step and long etch times. Because of this, engineers now utilize surface micromachining techniques for some types of sensors. We show diagrams of the two sensor technologies in Figure 3. Surface micromachined pressure sensors are also CMOS compatible and use piezoresistive measurement techniques, but no wafer bonding is necessary, and shorter etch times can be used.

Ask the Experts

Q: Do you have to use 3 lots of 77 units when performing an HTOL, or can you use a larger number? Related to this, can you run more than 3 lots of 800 units each for the ELFR calculation?

A: Yes, you can certainly use a larger number if you would like. Some engineers will run additional devices in case there are handling failures due to EOS or ESD. That way, you still have 77 units in each lot after the testing is complete. Furthermore, larger sample sizes will provide better statistical insight into low FIT rates and low DPPM levels.

Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

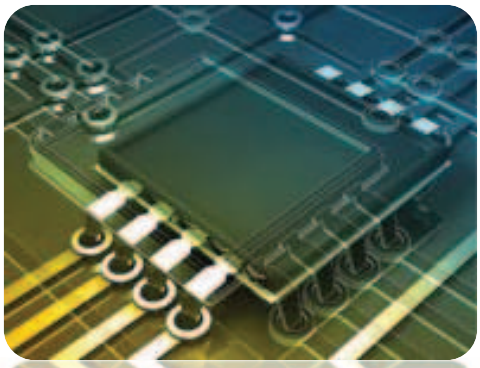
3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills
   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless

f. Thermal Interface Materials (TIMs) and Lids
g. Fine Pitch Warpage Reduction
h. Stacked Die and Stacked Packages
i. Material Selection for Board Level Temperature Cycling and Drop Reliability

4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow



Upcoming Webinars

(Click on each item for details)

Failure and Yield Analysis

4 sessions of 4 hours each
US: November 29 – December 2, 2021
(Mon – Thur), 11:00 A.M. – 3:00 P.M. EST;
8:00 A.M. – 12:00 NOON PST

Advanced CMOS/FinFET Fabrication

4 sessions of 2 hours each
US: December 6 – 9, 2021
(Mon – Thur), 11:00 A.M. – 1:00 P.M. EST;
8:00 A.M. – 10:00 A.M. PST

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!