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Photonics Device Fundamentals

By Christopher Henderson

Photonics Device Fundamentals

In this month’s feature article, we will continue our series on photonics device fundamentals. This is the second in a series of four articles. This month we discuss the Vertical Cavity Surface Emitting Laser (VCSEL).

Edge Emitting Laser Diode | Vertical Cavity Surface Emitting Laser Diode (VCSEL)

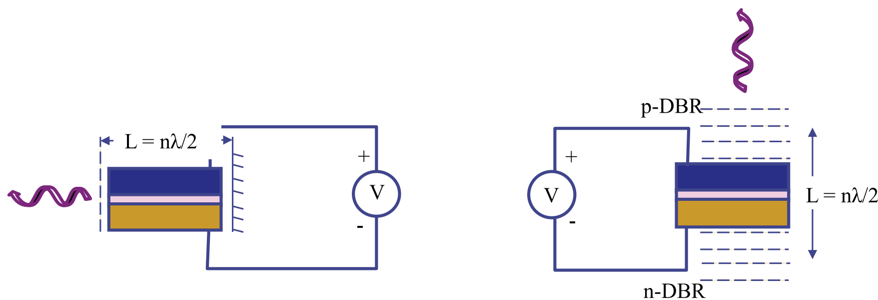

Figure 12. Vertical Cavity Surface Emitting Laser Diode.

Next, let’s discuss the Vertical Cavity Surface Emitting Laser Diode. Also known as the VCSEL, this device works better with planar semiconductor processes. On the left in Figure 12, we show a standard edge emitting laser diode. The light emanates from the edge of the junction. This can make it hard to integrate the laser light into a

In this Issue:

Page 1	Photonics Device Fundamentals
Page 5	Technical Tidbit
Page 7	Ask the Experts
Page 8	Spotlight
Page 12	Upcoming Courses

system because the semiconductor packaging must allow the light to emerge from the side of the package. In the VCSEL (shown on the right of Figure 12), the light emanates from the top surface, making it easier to package the device in such a way that we can make use of the light.

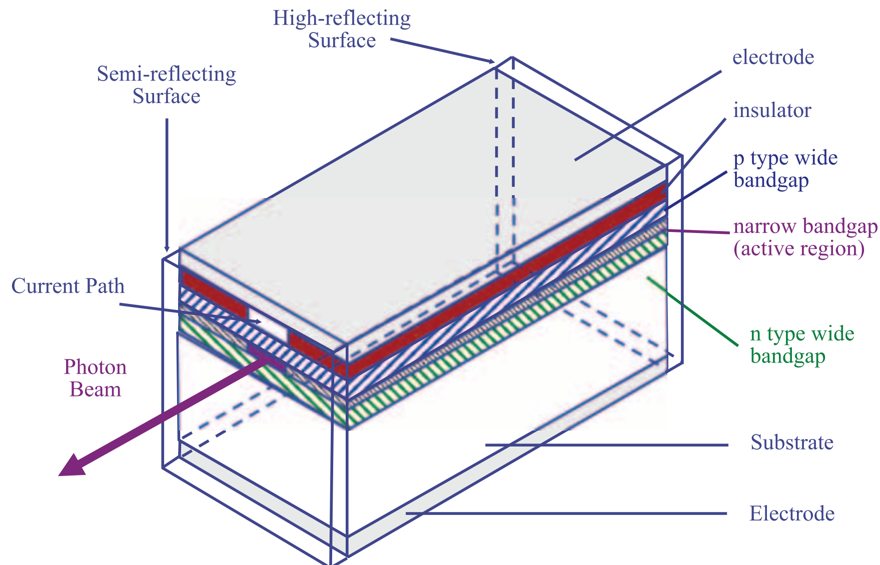

Figure 13. Basic construction for an edge-emitting laser diode.

Here in Figure 13, we show the basic construction for an edge-emitting laser diode. The bottom electrode is made from a metal compatible with the semiconductor substrate. We then deposit the n-type wide bandgap semiconductor on top of the substrate, followed by the narrow bandgap semiconductor, which forms the active region of the device. Next, we deposit the p-type wide bandgap semiconductor. The structure is surrounded by an insulating layer to direct the current path in the structure. Finally, the surface is covered with a highly reflective material to help confine the photons within the structure.

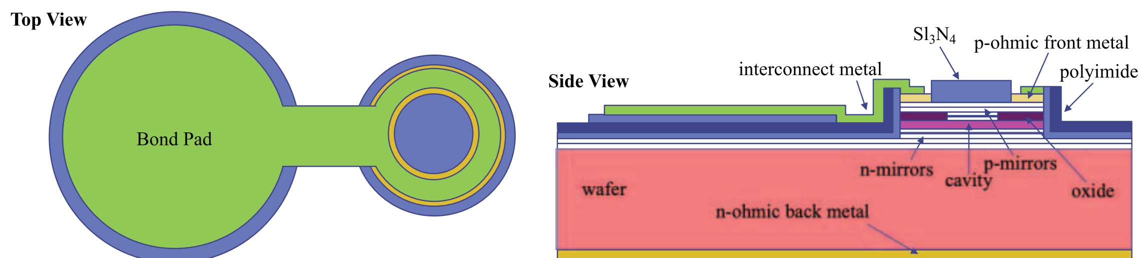

Figure 14. Example of an oxide-isolated VCSEL.

Figure 14 is an example of an oxide-isolated VCSEL. We show the top view on the left, and the side view on the right. An n-type ohmic metal coats the back side of the wafer. On top of the substrate we have the active semiconductor layers, followed by the n-mirror layers, then the semiconductor cavity, then the p-mirror layers, and then the oxide. We deposit polyimide on top of the oxide layer, followed by the interconnect metal. In the area where the light emanates, we pattern and remove the oxide and deposit the p-type ohmic metal layer and silicon nitride.

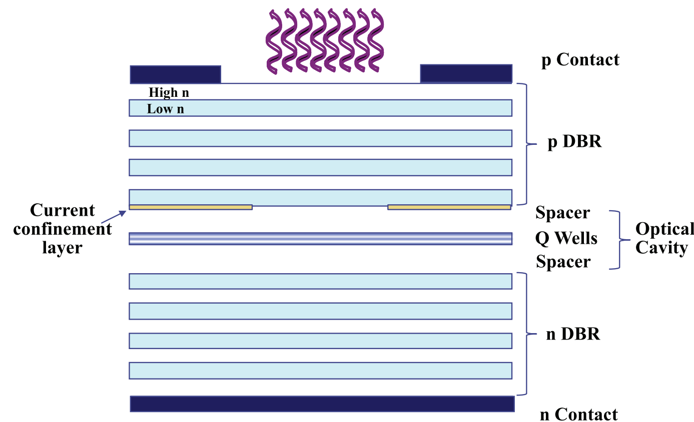

Figure 15. VCSEL MESA schematic details.

The light in a VCSEL structure is generated in a MESA structure that looks like this diagram shown here in Figure 15. On the bottom is the n-type contact, and on the top is the p-type contact. The upper and lower mirror structures consist of a number of layers designed to create a Distributed Bragg Reflector, or DBR, which consists of alternating high and low index of refraction materials. The center of the structure is the optical cavity. It consists of a current confinement layer on top, and spacer oxides above and below the semiconductor quantum well structure. The light emanates from the top in the opening in the p-contact metal.

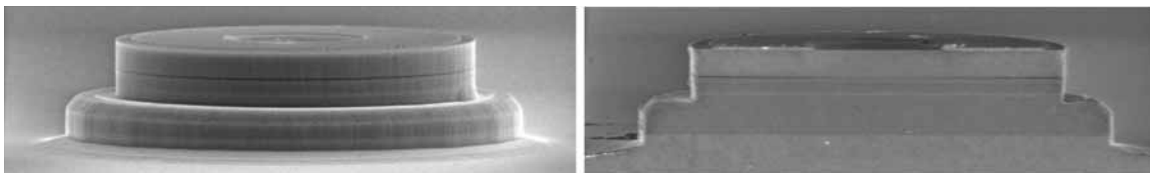

Figure 16. SEM images of VCSEL MESA structure.

Figure 16 is an example of an actual VCSEL MESA structure. We show a perspective scanning electron microscope image on the left, and a cross-section scanning electron microscope image on the right. The mesa structure is clearly evident in the images.

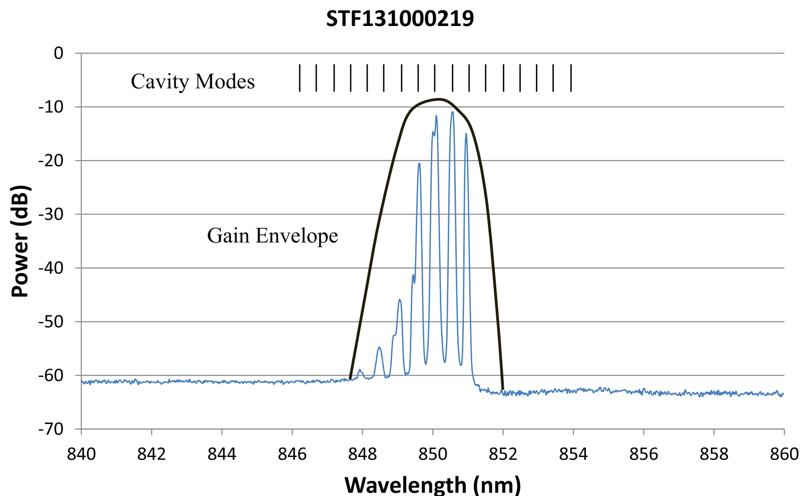

Figure 17. Actual emission spectrum from a VCSEL.

The VCSEL takes advantage of the cavity mode spectrum concept we mentioned earlier. Here in Figure 17, we show the actual emission spectrum from a VCSEL. The cavity modes are illustrated at the top, and the gain envelope is illustrated in the middle. This gain envelope is fairly tight in terms of the frequency, with a center frequency of 850 nm, varying approximately 2 nm on either side.

Next month, we will continue with part three in the series.

Technical Tidbit

Constraint Management

This month's technical tidbit covers Constraint Management.

Manufacturing a product in a timely manner in quantities required by the customer is a challenging activity. This process is only as good as the weakest link in the process. Conceptually, we can think about this chain as a supply chain. We have simplified it into five links to illustrate the concept. Here we have chains associated with marketing, planning, manufacturing, shipping, and the customer. If one of these links breaks down, the entire chain is disrupted. For the purpose of this discussion, we will primarily focus on the manufacturing portion of the diagram, since that is the portion we can directly influence.

We can measure productivity in terms of throughput and operation expenses. Net profit is equal to throughput, or revenue, minus operation expenses, excluding fixed costs. Return on investment, or ROI, is equal to net profit divided by investments, or fixed costs. Therefore, productivity then is defined as throughput, or revenue, divided by operation expenses.

$$Net\ Profit = \underset{\text{(Revenue)}}{Throughput} - \underset{\text{(Excluding Fixed Costs)}}{Operation\ Expenses}$$

$$Return\ on\ Investment = \frac{Net\ Profit}{\underset{\text{(Fixed Costs)}}{Investments}}$$

$$Productivity = \frac{\overset{\text{(Revenue)}}{Throughput}}{Operation\ Expenses}$$

Next, let's discuss constraints by describing what a constraint is. A constraint is anything that prevents the supply chain from achieving more of its goal. Quite often it is just a few, or even just one constraint that creates problems. Constraints might be internal or external to the supply chain. An internal constraint occurs when the market demands more than the supply chain can deliver. If this is the case, then the organization should focus on discovering that constraint; the steps to reduce its effect; and the potential to remove it.

What types of internal constraints might occur? Constraints can occur in three main areas: equipment, people, and strategy. The first constraint is equipment. The way equipment is currently used

limits the ability of the system to produce more salable goods and services. The second is people. Lack of skilled people limits the supply chain. Also, mental models held by people can cause behavior that becomes a constraint. The third is strategy. This a written or unwritten approach to business that prevents the organization from making more product. A constraint, however, is different than a breakdown. A breakdown, for example, could be the failure of a processing tool, which is not a constraint in the true sense, because once the tool is fixed, the supply chain production resumes. The constraint is the limiting factor that prevents the organization from getting more throughput of its products or services. This is typically revenue through sales.

An external constraint exists when the supply chain produces more than the market will bear. If this is true, the organization should focus on creating more demand for its products and services.

Managing constraints is very important. Constraints are also called bottlenecks because they have the smallest flow capacity, relative to the need, in a process. The higher the capacity utilization, the more pronounced the bottleneck in the process. The organization will need to analyze suspected bottlenecks; they don't necessarily manifest themselves where inventory builds up. The bottleneck will regulate the total output capacity and line speed for the process, and will determine the organization's strategic flexibility to capitalize on market swings.

What are the critical objectives for managing a constraint? There are four key points. First, there must be the correct inventory mix ready to load. Second, there must be a qualified equipment operator available at all times. Third, the constraint must be the number one priority for repair and maintenance. Fourth, the organization must engineer and monitor for productivity enhancement via set-up time reduction, statistical process control (SPC), and machine speed.

Ask the Experts

Q: What are the advantages/disadvantages of 2 masks vs 3 masks for Thin-Film Resistors?

A: The main advantage of using 3 masks is the ability to use a refractory contacting metal like TiW to make contact to the TaN, SiCr, or NiCr thin-film resistor material, as this makes a better connection. In a 2-mask process, one would use TiN, which also serves as the via liner, to make contact to the thin film metal. There is limited ability to react TiN and the thin-film resistor material together to make a lower resistance connection. Using 2 masks saves money, but the connection may degrade more easily, while 3 masks provides a more stable connection, but creates a more costly process. Sometimes, dummy metals are used under the thin-film resistor material as stress buffers, and this might require an additional mask, as well.

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Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting

6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing

13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

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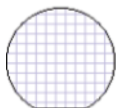

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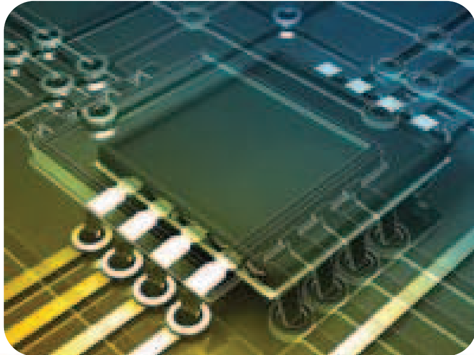
Semiconductor, Microelectronics, Microsystems and Nanotechnology Training

6501 Wyoming NE, Suite C215
Albuquerque, NM 87109-3971
Tel. (505) 858-0454
Fax (866) 205-0713
e-mail: info@semitracks.com



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Munich, Germany

Failure and Yield Analysis
April 12 – 15, 2021 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 19 – 20, 2021 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
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