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Bipolar Junction Technologies Part 1

By Christopher Henderson

In this document, we'll cover bipolar junction technologies. Although bipolar devices were very common for many years, their use in the 1980s and 1990s fell off due to the rise of CMOS. However, there are still some useful properties of bipolar devices, and we will discuss them here.

We'll begin with a history of the bipolar junction transistor, and then we'll discuss the operation of the bipolar transistor and conclude with some applications of these devices.

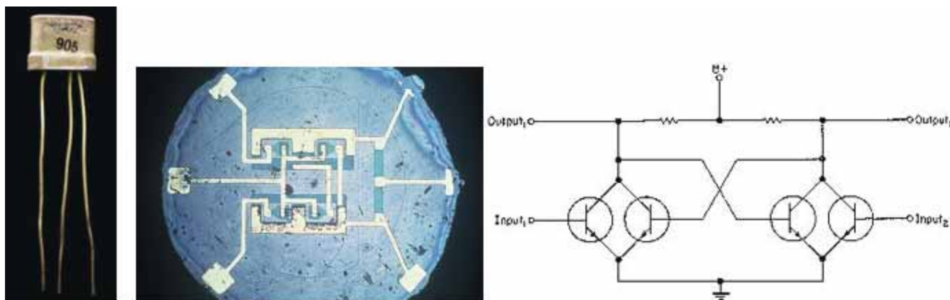

Figure 1. First silicon bipolar transistor (left) and first bipolar IC layout (center) and schematic (right).

The first silicon bipolar transistor was manufactured by Texas Instruments in 1954, followed up by the first bipolar IC from Fairchild, ten years later in 1964. There is an interesting story behind the development of the silicon transistor, and we show a clip from

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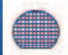

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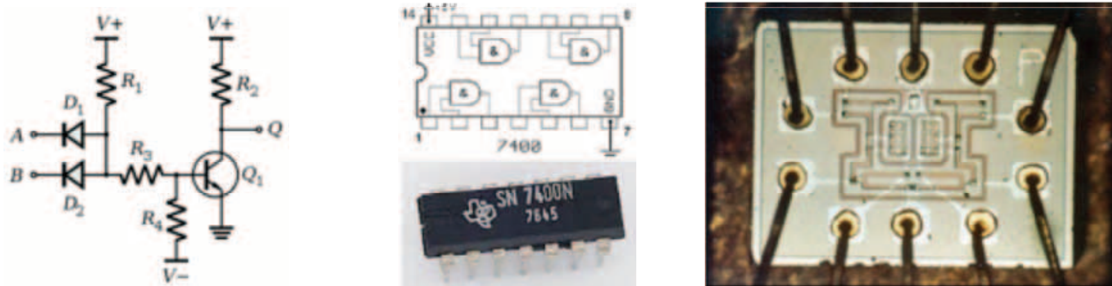
IEEE Spectrum, detailing the announcement of the silicon transistor below. This quote is from Michael Riordan, writing in IEEE Spectrum in April 2004. In 1954, a long and till-then uneventful session on silicon devices had been winding down at the Institute of Radio Engineers (IRE) National Conference on Airborne Electronics, in Dayton, Ohio. There, a parade of engineers and scientists were lamenting the sobering challenges of developing and eventually manufacturing silicon transistors. Amid the torpor, scattered attendees were stifling yawns, glancing at watches, and nodding off. But that was before Gordon Teal of Texas Instruments Inc. made his surprising announcement—and jaws dropped in disbelief. “Did you say you have silicon transistors in production?” asked a stupefied listener about 10 rows back in the audience, which now began to perk up noticeably. “Yes, we have three types of silicon transistors in production,” Teal replied, pulling several out of his pocket to the general amazement and envy of the crowd. Then, in a bit of quaint but effective razzle-dazzle, he cranked up a record player which began blaring out the swinging sounds of Artie Shaw’s big-band hit, “Summit Ridge Drive.” Amplified by germanium transistors, the music died out instantly as Teal dunked one into a beaker of hot oil. But when he repeated his demonstration immersing a silicon transistor instead, the music played on without faltering. Bell Labs actually had a device working as well, but they delayed introducing the device. The delay allowed fledgling Texas Instruments to leap forward and claim victory in this race. And it stood alone as the first company to manufacture silicon transistors in volume. Thanks to its foresight and aggressiveness, TI had the silicon transistor market essentially to itself for the next few years—and started down the road to becoming the international giant we know today.



Diode-Transistor Logic (DTL) Resistor-Transistor Logic (RTL) 7400 Series (Quad 2-input NAND)

Figure 2. Example circuit diagram (left), package and logic diagram (center), and die layout (right).

There are a few other important dates in the development of bipolar ICs, and they relate to the various logic implementations associated with bipolar integrated circuits.

- IBM (1959) — DTL (Diode Transistor Logic)
- Fairchild (1961) — RTL (Resistor-Transistor Logic)
- Sylvania (1963) — TTL (Transistor-Transistor Logic)
- Texas Instruments (1964) — 7400 series 1964, and then starting in 1971 they introduced the 74L, 74H, 74S, 74LS, 74AS, 74ALS series devices
- Philips (1972) — I2L (Integrated-Injection- logic)

We show an example circuit diagram, logic diagram and die layout, and package here in Figure 2 to give the reader an indication of the types of circuits and the physical construction of these devices.

Figure 3. Example of uA741 op amp.

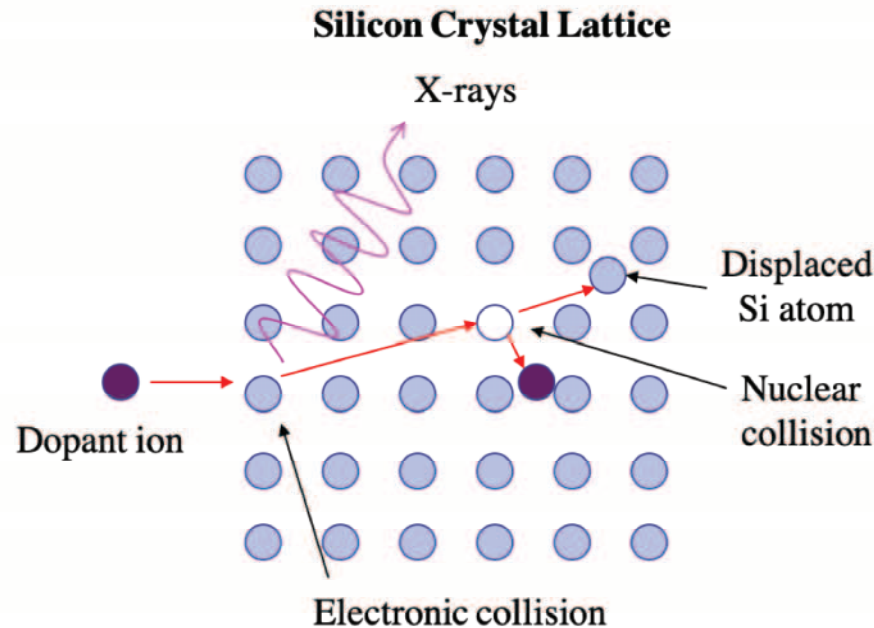
One popular circuit manufactured in bipolar technologies was the operational amplifier, or op amp for short. Bob Widlar at Fairchild designed the first operational amplifier in 1963, known as the uA702. Five years later, Fairchild introduced the uA741 general purpose operational amplifier, which would go on to become one of the most popular circuits ever used in electronics. We show an example of the uA741 op amp here, packaged in a Transistor Outline (TO) package.

To be continued next month.

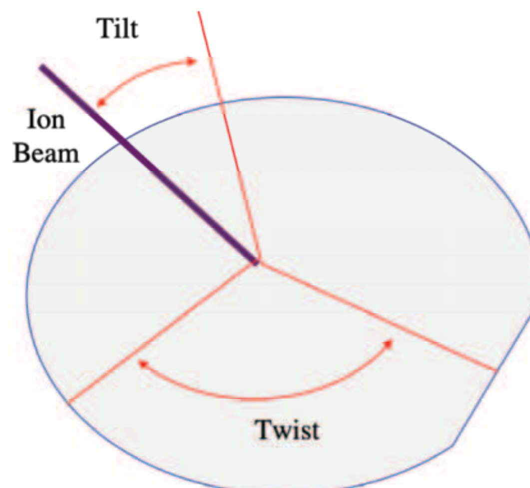
Technical Tidbit

Ion Implantation Concepts

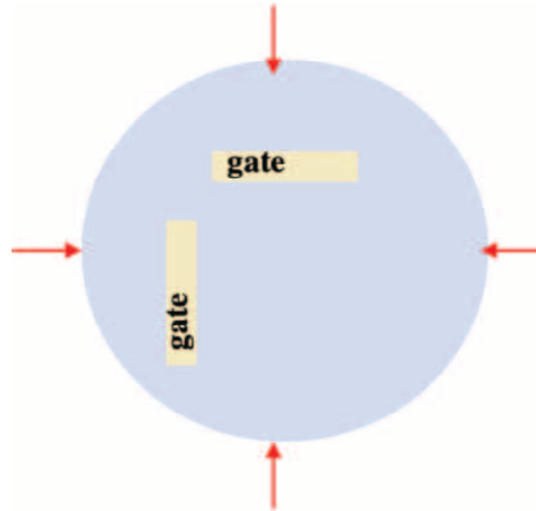
This technical tidbit provides the reader with a quick overview of the important concepts behind ion implantation. For a more in-depth discussion, please consult our Online Training System.



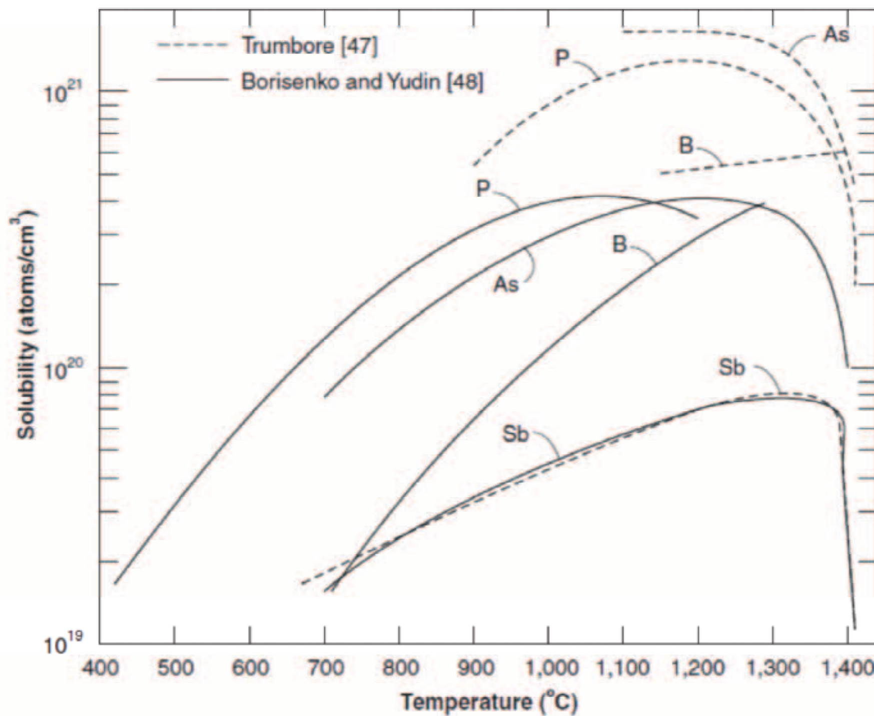
During ion implantation, impurity atoms are implanted into the substrate. These atoms do not magically attach themselves to the lattice structure and become electrically active, so we need an anneal step to activate the impurities and repair the implant damage. The advantages of ion implantation include good dose control for low or high impurity concentrations, good depth control, unique doping profiles, low temperature processing, and a wide choice of masks to stop the ions where they are not needed. The disadvantages to ion implantation include: lattice damage that needs to be repaired; transient enhanced diffusion, which causes existing atoms to move out of position; charging, which can lead to discharge damage or incorrect profiles; and incorrect distributions, due to the fact that ion implantation is a directional process.



Engineers will typically use a non-zero tilt angle to avoid ion channeling, or to implant into the sidewall of a trench, or even implant under the edge of the gate region. Engineers may also use the twist angle to avoid ion channeling as well as implant into the sidewall of a trench, or under the edge of the gate region.



One technique is to use a "quad" implant, where one implants 25% of the dose in each of four directions 90 degrees apart from one another. This generates a symmetrical implant profile around the gate.



This graph shows the solid solubility of dopants in silicon. The maximum dopant activation occurs at temperatures between 1100 and 1200°C, so engineers will typically use a laser anneal to reach these temperatures but keep the times short for a lower thermal budget. At lower temperatures between 500 and 800°C, dopant deactivation is more common, so it is important to avoid these temperatures once the dopants are activated.

Ask the Experts

Q: What size are the silica particles in mold compounds?

A: The silica particles within mold compounds are typically specified by the suppliers and can have a range of sizes. As a rule of thumb, their size is on the order of the diameter of the bond wires, but the size will have a distribution associated with it, meaning some will be smaller and some will be larger. The distribution will be wider with crushed (fumed) silica compared to colloidal silica.

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Spotlight: Introduction to Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Introduction to Processing*** is a 2-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.
4. **Current Issues in Assembly and Packaging.** Participants learn how packaging is a key enabler for semiconductor components. They also learn why we are seeing an explosion of different packaging types.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.

4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.
5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.
7. The seminar will provide an introduction to the packaging process and discuss the fundamental drivers behind the current developments in packaging.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. High-k gate and capacitor dielectrics
    c. Metal gates
    d. SOI
    e. Strained silicon
    f. Plasma doping

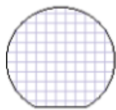
13. Overview of Semiconductor Packaging
    a. Purpose of the package
    b. Drivers
    c. Types of Packages
    d. Packaging Processes

For each of these modules, the following topics will be addressed:

1) fundamentals necessary for a basic understanding of the technique
2) its role(s) and importance in contemporary wafer fab processes
3) type of equipment used
4) challenges
5) trends

You may want to stress some aspects more than others or conduct a simple one-day overview course. Many of our clients seek ongoing just-in-time training that builds in-depth, advanced levels of reliability expertise. We'll work with you to determine the best course of action and create a statement of work that emulates the very best practices of semiconductor reliability analysis.

Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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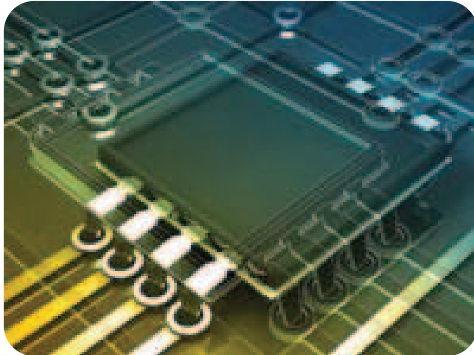

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Introduction to Processing
March 2 – 3, 2020 (Mon – Tue)
Portland, Oregon, USA

Failure and Yield Analysis
March 2 – 5, 2020 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
March 4, 2020 (Wed)
Portland, Oregon, USA

IC Packaging Technology
March 5 – 6, 2020 (Thur – Fri)
Portland, Oregon, USA

Semiconductor Reliability / Product Qualification
March 9 – 12, 2020 (Mon – Thur)
Portland, Oregon, USA

Wafer Fab Processing
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 30, 2020 (Thur)
Munich, Germany