Issue 111 September 2018

InfoTracks

Semitracks Monthly Newsletter

Latch-Up Overview Part 1

By Christopher Henderson

In this section, we will discuss the topic of latch-up. Latch-up is a form of electrical overstress that results in malfunction of the circuit, but may not cause permanent damage. Furthermore, latch-up is specific to CMOS ICs or other semiconductor devices that contain a PNPN structure. We'll discuss what this means further in a few minutes.

Here is the outline for this section. First we will provide an introduction to the topic of latch-up. Next, we'll show some examples of latch-up. We will then discuss what causes latch-up, including some of the preconditions or dependencies in circuits, as well as the various triggering modes. Finally, we will discuss latch-up testing. We perform latch-up testing to determine the robustness of the device to latch-up, much like we perform ESD testing to determine the robustness of the device to ESD.

Latch-up is a condition that causes high current on a circuit. While some devices—such as thyristors—take advantage of this phenomenon, generally, it is undesirable, as it causes an integrated circuit to malfunction and can result in permanent damage. Latch-up can occur when a regenerative pnpn circuit turns on. The pnpn circuit is sometimes referred to as a silicon-controlled rectifier or an SCR. Although there are numerous triggers for latch-up, the fundamental event is caused by the avalanche breakdown of the pnp collector-base junction which forward-biases the npn transistor in the silicon-controlled rectifier. Latch-up resistance is partially a

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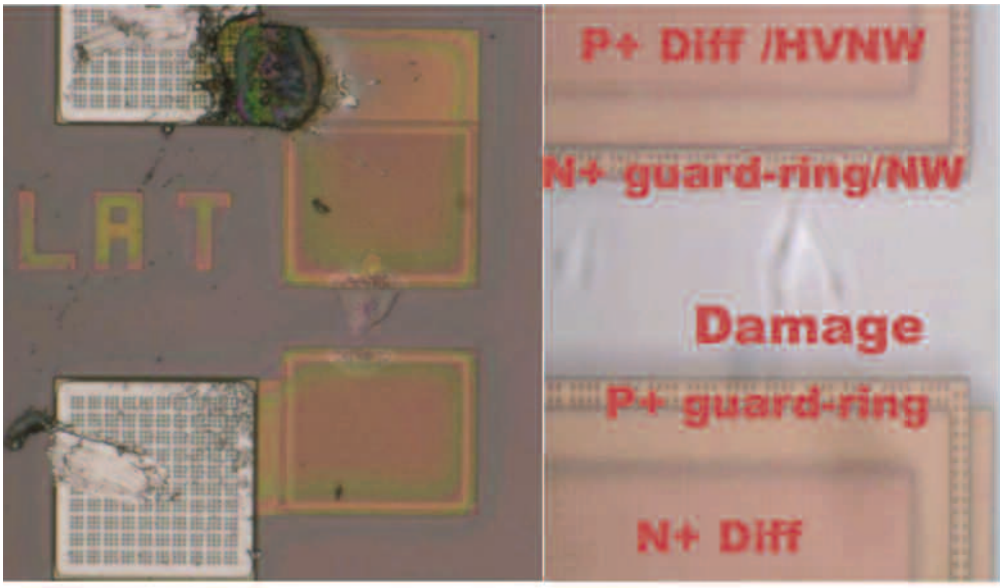
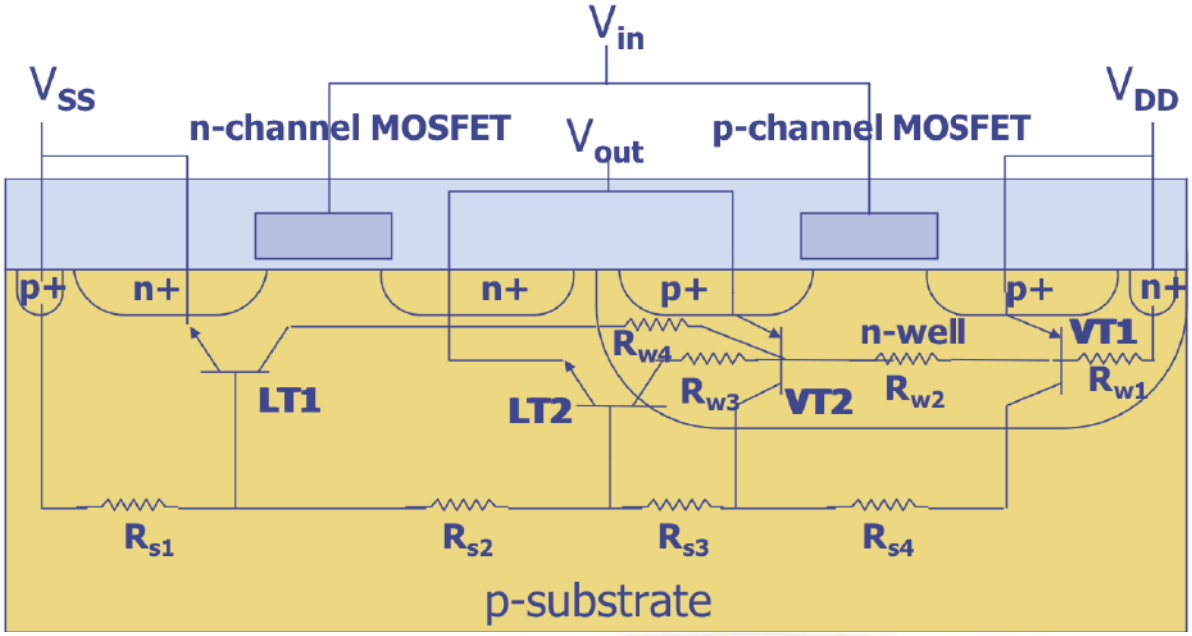
function of the circuit layout and processing. Spacing is a common problem. For example, a diffusion tied to VDD might be placed too close to an oppositely-tied diffusion connected to ground. P+ guard rings might be too closely placed to the n-well. Processing can also be a factor. For example, a narrow well depth will raise the inherent resistance value causing a large voltage drop that will trigger the SCR.



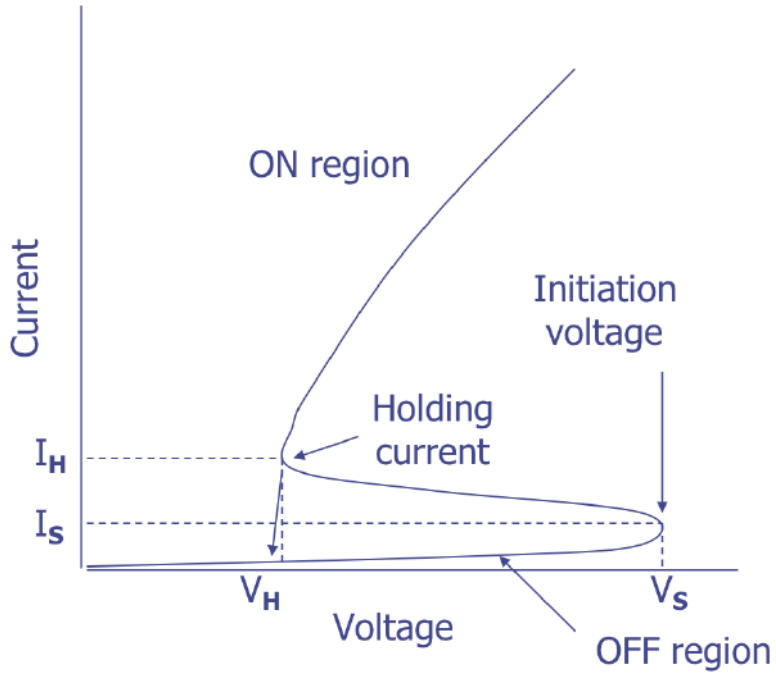
Catastrophic damage showing metallization burn-out

More limited damage from faster pulse

Many times latch-up will simply disrupt the operation of the chip. However, in some instances, latch-up can cause damage to occur. The two images here show examples of damage caused by latch-up. The image on the left shows metallization burn-out due to high current levels resulting from the latch-up condition. The image on the right shows more limited damage in the metallization—just a faint indication of melting in the metal—due to the fact that this was a faster pulse with less time to create damage.



Let's discuss how latch-up occurs in a CMOS circuit. At the bottom of page 2 we show a cross-section view of an inverter circuit. This circuit contains an n-channel transistor on the left and an p-channel transistor on the right. The p-channel transistor is located in an n-well. Now, let's view the parasitic elements over the cross section. Notice that there is a parallel network of circuit elements that exist in the substrate, and they can affect the operation of the circuit if turned on. When either VT1 or VT2 go into avalanche, LT1 or LT2 can be biased on.



An SCR exhibits a current-voltage behavior as shown here. The current starts off low as the voltage increases. This is known as the off region. At a voltage known as the initiation voltage, the current begins to increase quickly. In order for latch-up to occur, the voltage across the pnpn structure must exceed the initiation voltage. The curve then folds back on itself to a lower voltage but higher current. This is known as the holding current. Above this point, the curve again turns around, and the current increases more rapidly if additional voltage is applied. This is known as the on region. The on region can be damaging to an IC, particularly if the holding current exceeds the current capability of metal lines or bond wires. One should also note that this curve traces the current-voltage characteristics for an increasing voltage/current regime. If the voltage drops below the holding voltage, the SCR will turn off and the current will jump down to its lower value in the off region.

The presence of a pnpn structure does not mean that latch-up will occur. In addition to the voltage reaching an initiation voltage, the gain of the pnpn configuration must exceed one. The bias condition must also exist long enough for the current through the parasitic base-emitter junction to turn the junction on. Very short pulses may not turn the SCR on. Finally, the power supply must be capable of supply enough current to maintain the holding current. If not, the SCR will drop back into the off condition.

There are a number of triggering modes that can send a chip into latch-up. The late Ron Troutman, who did extensive research on CMOS latch-up, lists ten major triggering modes. Please refer back to the latch-up circuit schematic on page 2 for the location of the circuit elements mentioned here. The first triggering mode is an output going below V_{SS}. This creates a bias across R_{S1} and R_{S2}, turning the npn transistor L_{T2} on. The second mode is an output going above V_{DD}. This creates a bias across R_{W2}, turning the pnp transistor V_{T2} on. The third mode is an input node going above V_{DD} or below V_{SS}. In order for this to cause a problem though, the input must be connected to an n+ or p+ diffusion. These are the most common triggering modes. A fourth mode is the avalanche breakdown of the n-well junction. With V_{T1} conducting, R_{S1} will conduct current, turning L_{T1} on. Punchthrough from the n-well to the n+ diffusion is the fifth mode. This creates a low resistance path that in turn takes L_{T2} out of the circuit and replaces it with a short.

Punchthrough from the p-well to the p+ diffusion is the sixth mode. This creates a low resistance path that in turn takes V_{T1} and/or V_{T2} out of the circuit and replaces it with a short. The seventh mode requires a parasitic field device. An example of this would be a metal or polysilicon line that bridges the n- and p-channel transistor regions. A bias on this line can invert the silicon immediately below, causing a short. Light or radiation effects constitute the eighth mode. Photocurrents in the lateral npn or vertical pnp can turn on the transistors, causing the circuit to enter latch-up. The ninth mode is the avalanching of the source or drain junctions. This can inject charge into the base regions of L_{T1} or L_{T2}, causing them to turn on. Finally, a ramped power supply or noise can create a displacement current, turning on one of the transistors.

There are several techniques used to suppress latch-up in CMOS circuits. The first method is to increase diffusion spacings in the I/O circuitry. Because of their size and their connection to the outside world, I/O circuits are more likely to latch-up than core logic. By increasing the diffusion spacings, the punchthrough voltages are higher, and the field parasitic devices are weaker. Another method is to use double guard rings in the I/O circuitry. For example, an NMOS transistor can be surrounded by an n+ ring in an n-well, which in turn can be surrounded by a p+ ring. Guard rings help to diminish parasitic transistor activity by forcing the silicon surface into depletion, rather than inversion. Another layout trick is to place the same polarity transistors adjacent to one another. This helps to reduce punchthrough effects. One can double guard ring the core logic from the I/O logic to reduce parasitic activity in the core logic. Shallow trench isolation can also reduce latch-up by reducing parasitic effects. The thicker oxide layer makes inverting the silicon more difficult. Lastly, one can eliminate latch-up by switching to silicon on insulator, or SOI. SOI uses isolated transistor regions, so the parasitic pnpn structure does not exist.

(To be continued in the October 2018 Newsletter)

Technical Tidbit

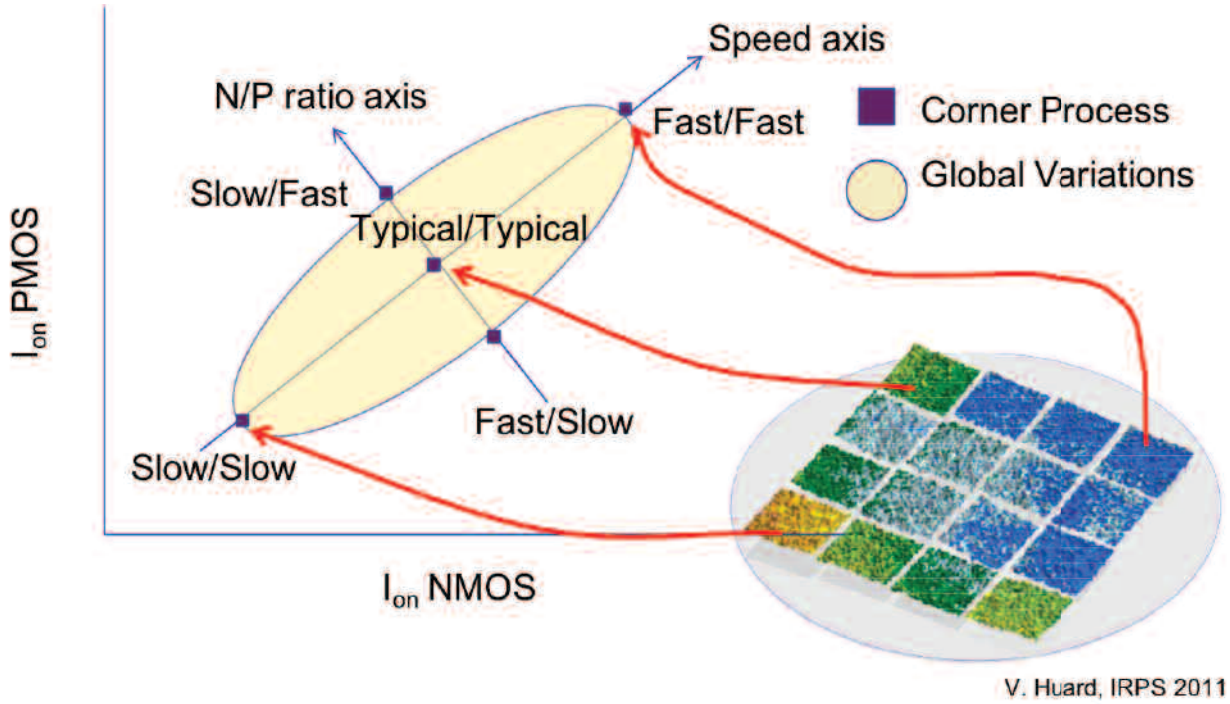
Process Corners

In semiconductor manufacturing, a process corner is an example of a design-of-experiments (DoE) technique that refers to a variation of fabrication parameters used in applying an integrated circuit design to a semiconductor wafer. Process corners represent the extremes of these parameter variations within which a circuit must function correctly. A circuit running on wafers fabricated at these process corners may run slower or faster than specified and at lower or higher temperatures and voltages, but if the circuit does not function at all at any of these process extremes the design is considered to have inadequate design margin. In order to verify the robustness of an integrated circuit design, semiconductor manufacturers will fabricate corner lots, which are groups of wafers that have had process parameters adjusted according to these extremes. They will then test the devices made from these specially-processed wafers at varying increments of environmental conditions, such as voltage, clock frequency, and temperature, applied in combination (two or sometimes all three together) in a process called characterization. The results of these tests are plotted using a graphing technique known as a shmoo plot that indicates clearly the boundary limit beyond which a device begins to fail for a given combination of these environmental conditions. Corner-lot analysis is most effective in digital circuits because of the direct effect of process variations on the speed of transistor switching during transitions from one logic state to another, which is not relevant for analog circuits, such as amplifiers.

There can be both FEOL and BEOL process corners. For FEOL, a common naming convention for process corners is to use two-letter designators, where the first letter refers to the N-channel MOSFET (NMOS) corner, and the second letter refers to the P channel (PMOS) corner. In this naming convention, three corners exist: typical, fast and slow. Fast and slow corners exhibit carrier mobilities that are higher and lower than normal, respectively. For example, a corner designated as FS denotes fast NFETs and slow PFETs. There are therefore five possible corners: typical-typical (TT) (not really a corner of an n vs. p mobility graph, but called a corner, anyway), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF). The first three corners (TT, FF, SS) are called even corners, because both types of devices are affected evenly, and generally do not adversely affect the logical correctness of the circuit. The resulting devices can function at slower or faster clock frequencies, and are often binned as such. The last two corners (FS, SF) are called "skewed" corners, and are cause for concern. This is because one type of FET will switch much faster than the other, and this form of imbalanced switching can cause one edge of the output to have much less slew than the other edge. Latching devices may then record incorrect values in the logic chain.

One can also define BEOL corners. In addition to the FETs themselves, there are more on-chip variation (OCV) effects that manifest themselves at smaller technology nodes. These include process, voltage and temperature (PVT) variation effects on on-chip interconnect, as well as via structures. Extraction tools often have a nominal corner to reflect the nominal cross section of the process target. Then the corners C_{best} and C_{worst} were created to model the smallest and largest cross sections that are in the allowed process variation. A simple thought experiment shows that the smallest cross section with the largest vertical spacing will produce the smallest coupling capacitance. CMOS digital circuits were more sensitive to capacitance than resistance, so this variation was initially acceptable. As processes

evolved and resistance of wiring became more critical, the additional RC_{best} and RC_{worst} were created to model the minimum and maximum cross-sectional areas for resistance. But the one change is that cross sectional resistance is not dependent on oxide thickness (vertical spacing between wires), so for RC_{best} the largest is used, and for RC_{worst} the smallest is used.



V. Huard, IRPS 2011

Let's now look at process corners from a more visual perspective. This graph shows how global variations can impact device operation. The graph shows the on current in PMOS transistors as a function of the on current in NMOS transistors. The range of operation typically defines a tilted ellipse, where the major axis or the line through the short axis defines the n- or p-channel ratio, and the minor axis forms the speed axis. The intercepts form the corners of the process. For example, the lower left corner axis is labeled slow/slow. This indicates both slower speed n and p-channel transistors. Slow/Fast, located near the N/P ratio axis, indicates a slow n-channel transistor and a fast p-channel transistor. Typically, engineers make measurements to define the corners of the process. They can then be related to position on the wafer to define global variations.

Ask the Experts

Q: What techniques are typically used to determine oxidation on a bond pad?

A: The two most commonly used techniques would be Auger Electron Spectroscopy and Time-of-Flight Secondary Ion Mass Spectroscopy (TOF-SIMS). Energy Dispersive X-ray analysis (EDX) is not a good analysis technique for this problem, since the oxide layer is quite thin. EDX data comes from deeper beneath the surface, so it is not as useful for detecting an oxide layer on the surface of a bond pad.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

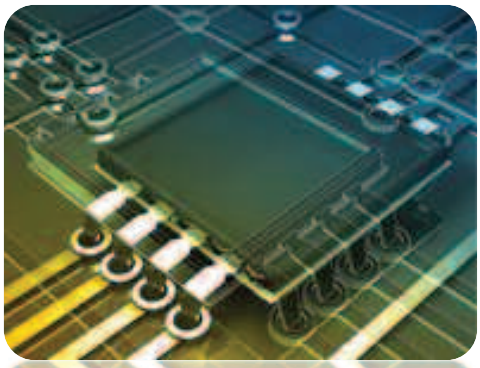
Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks

17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of "Conventional" Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs
20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

Wolf, Microchip Manufacturing,
Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.



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If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Wafer Fab Processing
September 17 – 20, 2018 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
October 29 – November 1, 2018 (Mon – Thur)
Singapore

Failure and Yield Analysis
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

Wafer Fab Processing
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

Introduction to Processing
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

Failure and Yield Analysis
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA