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Laser Decapsulation

By Christopher Henderson

Historically, failure analysts used either mechanical or chemical means to decapsulate integrated circuits. They used primarily mechanical means on hermetically-sealed components (ceramic and metal packages) and primarily chemical means on plastic encapsulated microcircuits. The advent of newer bonding materials like copper wire creates problems for traditional methods though. Chemical decapsulation can damage copper wires. While engineers work on new solutions and procedures for chemical decapsulation in these devices, other companies developed alternate methods for decapsulation. The most important of these new tools is the laser decapsulation system.

Laser decapsulation uses the energy from a laser beam to remove the mold compound from plastic encapsulated microcircuits. Scientists developed three different laser systems for this purpose: Pulsed CO_2, Nd-YAG, and KrF Excimer laser systems.

One can remove mold compound epoxies with pulsed CO_2 systems that operate a 10.6μm wavelengths. This wavelength is an infrared energy source. As such, the epoxy absorbs the energy from the laser, causing the epoxy in the mold compound to melt and eventually vaporize. However, this wavelength damages the die surface. The passivation layers absorb this energy and couple it into the interconnect below, creating damage and rendering circuits non-functional.

One can remove mold compound epoxies with pulsed

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neodymium: yttrium-aluminum-garnet (Nd:YAG) lasers operating at 532nm. At this wavelength, the dark-colored epoxy also absorbs the energy, causing it to melt and then vaporize. However, this wavelength also damages the die. At 532nm, the laser energy passes through the dielectric, but is partially absorbed by the metal layers below. In fact, this wavelength can be used in laser cutting systems that cut metal lines. Again, this leads to damage to the interconnect, rendering circuits non-functional.

One can also remove mold compound epoxies with a pulsed krypton-fluoride (KrF) excimer laser than operates at 248nm. At this wavelength, the energy is deposited very close to the surface of the epoxy. This leads to an ablative removal method. This wavelength also induces less damage to the die surface, as the top passivation absorbs more of the energy from the laser. Although this does less damage, it will still render sensitive circuits non-functional. This laser wavelength is also slower than the other wavelengths.

It is important to control the pulse repetition rate. If one uses too high of a pulse repetition rate or too long of a pulse width, this action can result in the epoxy polymerizing and not being removed. Also, the laser removes the epoxy in the mold compound, but not the silica particles. To remove the silica particles, one needs airflow to blow them away from the active cutting surface. Since the laser decapsulation process will render most circuits non-functional, one must stop the cutting process just short of the die surface. To keep the circuit functional, one must use plasma cleaning or a chemical decapsulation for the final remaining material.

Figures 1 and 2 show a low magnification and a high magnification image of a chip that has been decapsulated using the laser decapsulation method.

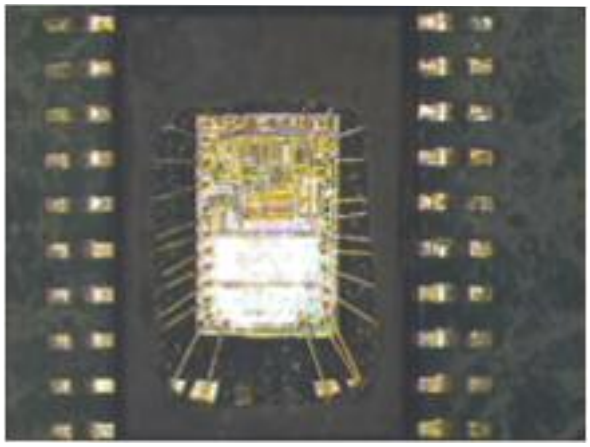

Figure 1. Low magnification image of an integrated circuit after laser decapsulation

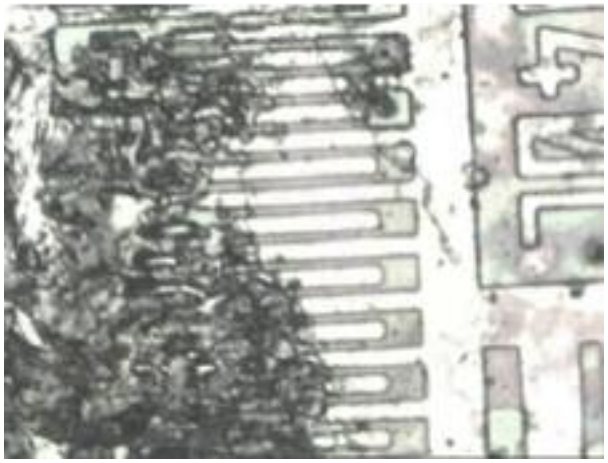

Figure 2. High magnification image of the sample surface after laser decapsulation.

Several companies manufacture laser decapsulation systems. Both Controlled Laser Corporation and Digit Concept make these systems. Digit Concept also licenses some technology from Controlled Laser Corporation to make several tools. We show an example of a system from Controlled Laser Corporation below (Figure 3).

Figure 3. Example of laser decapsulation tool (courtesy Control Laser Corporation)

As packages become more complex and the materials change, the use of laser decapsulation is likely to grow. Laser decapsulation does allow for more precision in the x- and y-directions, as well as reasonable control in the z-dimension. The big drawback to laser decapsulation is damage to the chip, which can render it non-operational. As scientists study this problem and develop new laser techniques, the impact on functional circuits should go down. Look for more development in this area in the future.

Technical Tidbit

HAST Chamber Operation

The general concepts for Highly Accelerated Stress Testing (HAST) are straightforward to understand. The idea is to stress devices at temperatures between 110 – 130°C for JEDEC tests, and possibly as high as 156°C for device characterization. The relative humidity level should be maintained at 85% for this testing. However, during warm-up and cool-down, the thermal load from the devices and boards can affect this behavior. For example, incorrect airflow can lead to condensation on the components, as they warm more slowly than the environment. In order to avoid this problem, the wet-bulb temperature needs to remain below that of the electronics. These graphs show a full-load ramp-up to 156 degrees centigrade, 85% relative humidity. The top graph shows an example before optimization of the fan behavior, and the bottom graph shows it after optimization. After optimization, the wet-bulb temperature is always below the temperature at any point during the cycle.

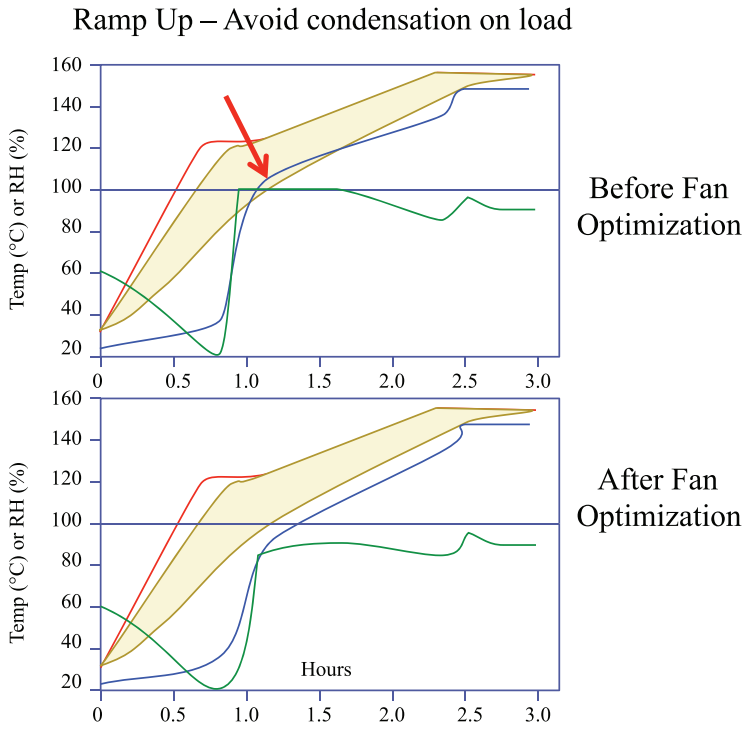

Figure 1. Example showing ramp up behavior of a HAST chamber before fan optimization and after fan optimization. Red arrow indicate region where humidity reaches 100% and condensation may occur.

There can be a different set of problems during the cool-down period. For instance, the mechanical pressure relief must be slow, on the order of three hours, to allow for the units to cool correctly without resulting in pressure issues. One should not vent the system until the pressure reaches one atmosphere. Also, one must hold the relative humidity at the test value to ensure correct results as the units must retain the moisture they acquired during the test.

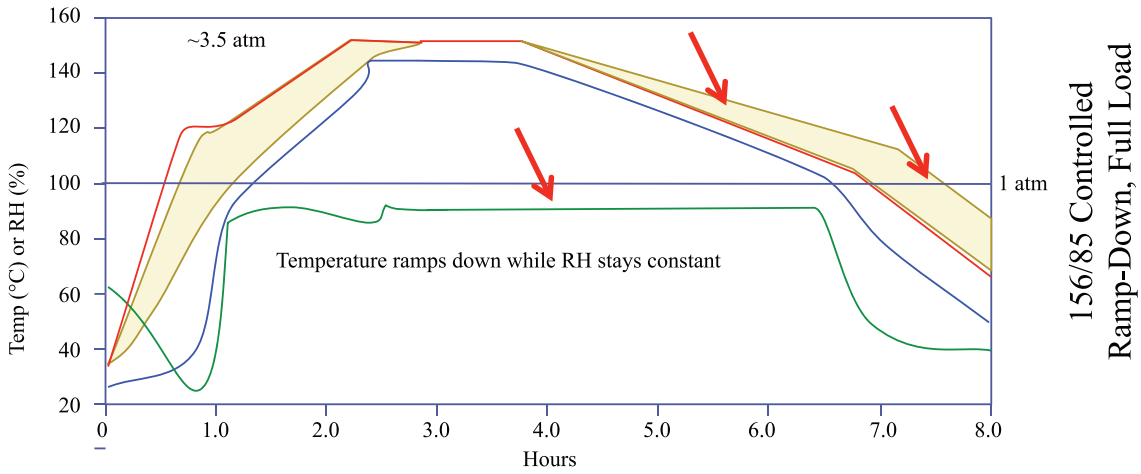

Figure 2 showing full cycle. The top arrow indicates that mechanical pressure relief must be slow, the right-most arrow indicates that one should not vent until you reach one atmosphere, and the left-most arrow indicates that the relative humidity should remain constant.

This can require some experimentation, so engineers should plan time in the schedule to characterize this behavior should they begin performing HAST testing, if they begin using new equipment, or even if they design new boards to stress new components.

Ask the Experts

Q: I hear a lot of discussion about NBTI (Negative Bias Temperature Instability). Is PBTI (Positive Temperature Instability) a problem as well??

A: It can be in High-K Metal Gate technologies, but it is not a big issue in circuits with oxide or oxynitride-based gate dielectrics. Mikael Denais and a team from ST Microelectronics did a nice study on this issue back in 2004, and determined that while PMOS NBTI can lead to changes in threshold voltages of as much as 8%, NMOS PBTI, NMOS NBTI, and PMOS PBTI normally exhibit changes of less than 1%. Researchers do see bigger shifts in PBTI with High-K Metal Gate transistors, and they are actively studying this phenomenon.

Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a one-day course that offers an overview look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we summarize the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an overview of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

5. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
6. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

1. Raw Silicon Wafers
2. Ion Implantation
3. Thermal Processing
4. Contamination Monitoring and Control
5. Wafer Cleaning and Surface Preparation
6. Chemical Vapor Deposition
7. Physical Vapor Deposition
8. Lithography
9. Etch
10. Chemical Mechanical Polishing
11. Cu Interconnect and low-k Dielectrics
12. Leading Edge Technologies and Techniques
    a. ALD
    b. high-k gate and capacitor dielectrics
    c. metal gates
    d. SOI
    e. strained silicon
    f. plasma doping

For each of these modules, the following topics will be addressed:

1 fundamentals necessary for a basic understanding of the technique
2 its role(s) and importance in contemporary wafer fab processes
3 type of equipment used
4 challenges
5 trends

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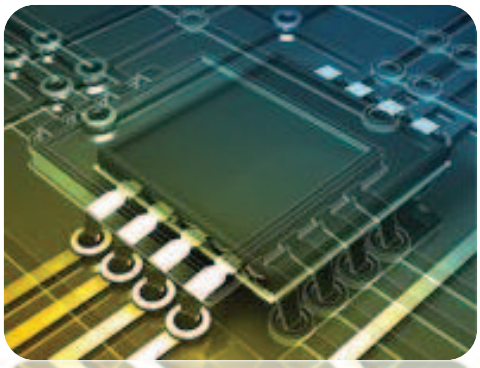

Upcoming Courses

(Click on each item for details)

Advanced Semiconductor Metallurgy and Challenges
October 23 – 25, 2013 (Wed – Fri)
Malaysia

Wafer Fab Processing
November 7, 2013 (Thur)
San Jose, California, USA

Advanced Thermal Management and Packaging Materials
November 19 – 20, 2013 (Tue – Wed)
Philadelphia, Pennsylvania, USA

Copper Pillar Technology and Challenges
December 19 – 20 2013 (Thur – Fri)
Malaysia

Microelectronic Defect, Fault Isolation and Failure Analysis
February 19 – 21, 2014 (Wed – Fri)
Malaysia

Microelectronic Defect, Fault Isolation and Failure Analysis
February 24 – 26, 2014 (Mon – Wed)
Singapore

Feedback

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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