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Bipolar Junction Technologies Part 2

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In this document, we'll continue to cover bipolar junction technologies. Although bipolar devices were very common for many years, their use in the 1980s and 1990s fell off due to the rise of CMOS. However, there are still some useful properties of bipolar devices, and we will discuss them here.

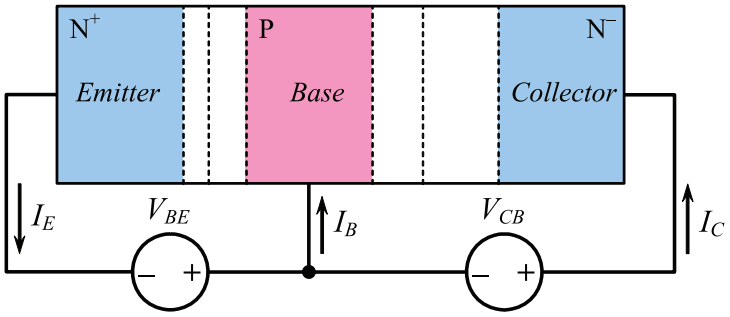

Figure 4. Illustration of NPN transistor.

Let's move on to a description of the bipolar junction transistor's operation. An NPN transistor consists of a P-type base region sandwiched between N-type emitter and collector regions. Let's imagine that a voltage source VBE is applied from base to emitter, and a voltage source VCB is applied from collector to base. It's important to note that we often use alternative biasing configurations. For this diagram in Figure 4 we chose VCB, but some engineers would use VBC. And of course some engineers use VCE rather than VBC.

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Furthermore, many books use PNP transistors rather than NPN because the conventional current patterns are simpler. Some manufacturers prefer to use NPN transistors because they are often favored over PNPs for various reasons (typically, because NPN transistors benefit from higher electron mobility, and therefore process engineers usually optimize NPN devices over PNP transistors).

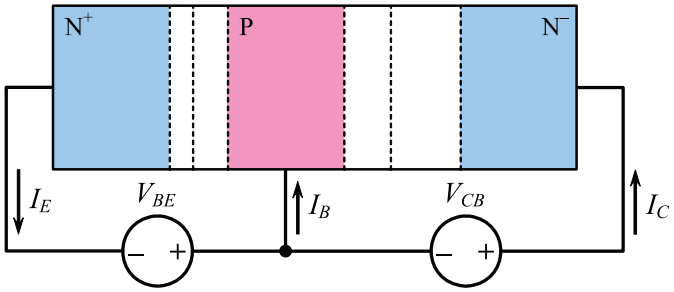


Figure 5. NPN transistor regions of operation.

NPN transistors have four regions of operation:

- Cutoff: $V_{BE} < 0V, V_{CB} > 0V$
- Forward active: $V_{BE} > 0V, V_{CB} > 0V$
- Reverse active: $V_{BE} < 0V, V_{CB} < 0V$
- Saturation: $V_{BE} > 0V, V_{CB} < 0V$

A few comments are in order concerning these regions of operation. The forward active behaves better than reverse active because the doping is not symmetrical. Saturation can be useful, but many SPICE simulators don't handle it correctly. Reverse active is still used for some special purposes. A famous one is the use of reverse active NPN transistors in standard bipolar for current mirrors because the larger collector-base (CB) junction actually matches better than the much smaller emitter-base (EB) junction. The original transistor-transistor logic (TTL) logic family also used reverse active devices. Saturation can lead to serious problems in junction-isolated processes if the designer doesn't understand the problems that it can cause, but again there are useful applications for saturated transistors; for example, power switches. SPICE stands for Simulation Program with Integrated Circuit Emphasis.

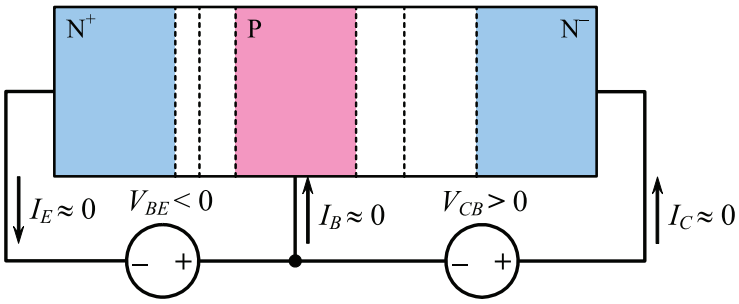


Figure 6. Regions of operation: cutoff mode.

Let's begin with the cutoff mode. When an NPN operates in cutoff, the base-emitter depletion region is reverse-biased ($V_{BE} < 0V$) and the base-collector depletion region is reverse-biased ($V_{CB} > 0V$). Each of these junctions behaves as it does in a PN diode, so the terminal currents I_E, I_B, and I_C are all very small. In this condition, we do not want to avalanche the base-emitter junction, since that action typically destroys the transistor. Furthermore, avalanching the BE junction of a planar NPN usually kills the transistor gain (β) because the avalanche process occurs at the surface and hot carriers desorb hydrogen that passivated dangling bonds. The regenerated dangling bonds become traps that cause a drastic degradation of β. Also, in this configuration we can expect more IC than IE since the thicker depletion layer (base to collector) allows for more recombination.

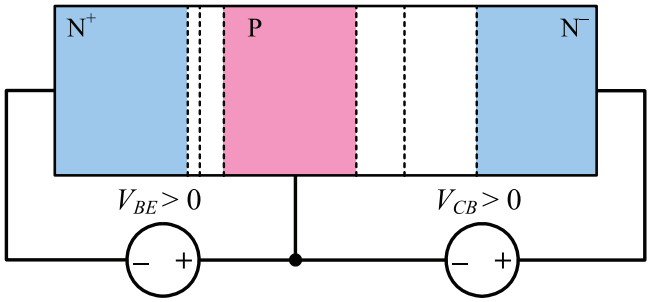


Figure 7. Regions of operation: forward active.

The next region is the forward active region. When an NPN operates in the forward active region, the base-emitter depletion region is forward-biased ($V_{BE} > 0V$) and the base-collector depletion region is reverse-biased ($V_{CB} > 0V$). Although each of the two PN junctions acts like a PN diode, they are located so close to one another that they begin to interact.

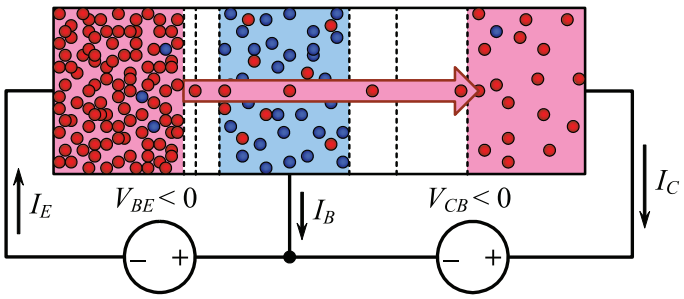


Figure 8. Illustration of PNP transistor.

So far, we have discussed bipolar transistors by using the NPN transistor as the example. Even though PNP transistors do not have as good a gain, they do have their uses. While NPN transistors have better mobility, engineers can adjust their properties down to be more in sync with the PNP transistor. The PNP

transistor can also be useful in certain circuits; for example, one can make better bandgap references with PNP transistors in the technology. The main reason that PNP transistors are good in bandgaps is that the mismatch of these transistors generates a ΔV_{BE} term that can be cancelled by trimming one of the resistors in the circuit. The mismatch of MOS transistors is mostly in threshold voltage, and the transconductance's variation with temperature causes an unpredictable temperature coefficient to appear that can't be trimmed out. Generally, simulations seem to underestimate the magnitude of this problem by a factor of two or three. The PNP transistor behaves much like an NPN transistor. The PNP uses a P-type emitter, an N-type base, and a P-type collector. During forward-active operation, holes injected from the emitter diffuse across the base to reach the collector. The forward-biased PNP exhibits $V_{BE} < 0V$, $V_{CB} < 0V$.

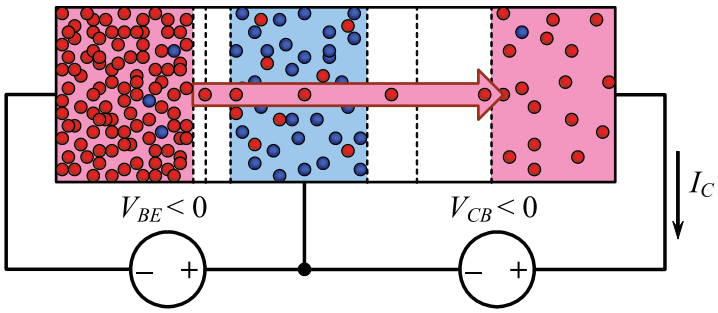


Figure 9. Illustration of PNP transistor (cont.).

PNP transistors generally do not perform as well as NPN transistors. Holes are less mobile than electrons, PNP transistors tend to switch more slowly than NPN transistors, so most processes optimize the NPN transistor at the expense of the PNP transistor. To summarize, the main reasons we use bipolar transistors are:

1) The exponential I_C-vs.-V_{BE} function allows some very useful circuits to be created; for example, Gilbert translinear circuits that can multiply and divide currents.
2) The bandgap circuit allows the creation of cheap and relatively accurate voltage references.
3) Voltage-proportional-to-absolute temperature circuits allow construction of current limits using metal resistors that have low inherent temperature coefficients.
4) High pulse-power handling capability allows bipolars to make excellent ESD devices.

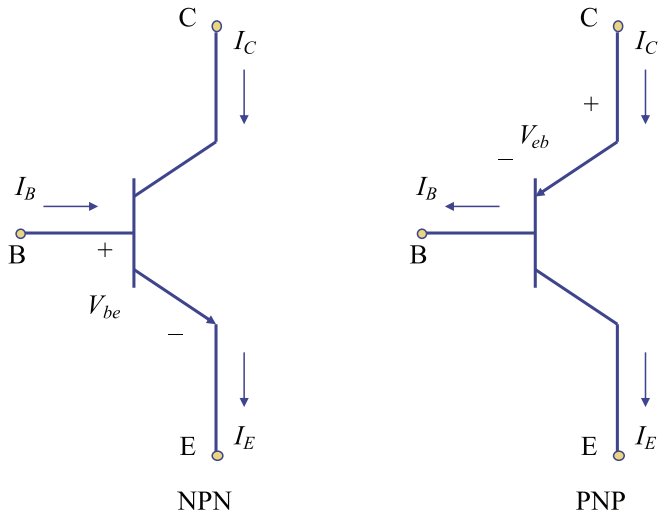


Figure 10. NPN and PNP bipolar transistors: engineering symbols.

In Figure 10 we show the engineering symbols for the NPN and PNP bipolar transistors. The bipolar transistor is used as a discrete device, and as an element of a larger circuit. The bipolar circuit is a current-controlled current device. To summarize, the current flowing through the emitter junction, labeled E in this drawing, is proportional to the current flowing into the base junction, labeled B in this drawing. There are two types of bipolar transistors: NPN and PNP. An NPN transistor has an n-doped collector, a p-doped base, and an n-doped emitter. The PNP transistor has the opposite configuration.

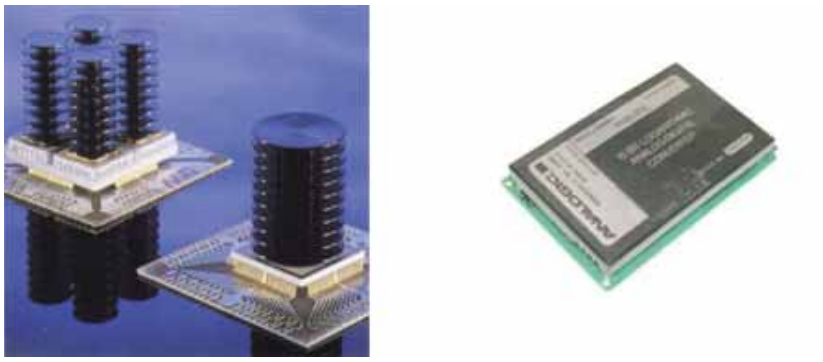


Figure 11. Illustration of emitter-coupled logic cell (left) and logarithmic converter (right).

The BJT remains a device that excels in some applications—such as discrete circuit design—due to the very wide selection of BJT types available, and because of its high transconductance and output resistance compared to MOSFETs. The BJT is also the choice for demanding analog circuits, especially for very-high-frequency applications such as radio-frequency circuits for wireless systems. It works in high speed digital logic such as emitter-coupled logic-use BJTs. Bipolar transistors can be combined with MOSFETs in an integrated circuit by using a BiCMOS process of wafer fabrication to create circuits that take advantage of the application strengths of both types of transistor. The transistor parameters α and β characterize the current gain of the BJT. It is this gain that allows BJTs to be used as the building blocks of electronic amplifiers. The three main BJT amplifier topologies are: common emitter, common base, and common collector. Another use for the Bipolar circuit is the silicon bandgap temperature sensor. Because of the known temperature and current dependence of the forward-biased base–emitter junction voltage, the BJT can be used to measure temperature by subtracting two voltages at two different bias currents in a known ratio. Finally, BJT circuits can be used for logarithmic converters. Because base–emitter voltage varies as the logarithm of the base–emitter and collector–emitter currents, a BJT can also be used to compute logarithms and anti-logarithms. A diode can also perform these nonlinear functions, but the transistor provides more circuit flexibility.

In conclusion, the bipolar junction transistor was a common transistor type in the early years of the semiconductor industry. In fact, the bulk properties of the transistor made it much easier to implement in the beginning of the semiconductor era rather than the MOS transistor, which relies on a near-perfect surface interface. However, engineers overcame the surface interface problems through cleanliness and process control, and the electronics industry largely adapted to using CMOS rather than bipolar circuits. There are still some important applications for bipolar circuits. They include Emitter Coupled Logic (ECL), many types of amplifiers, a variety of sensor types, and circuits that require fast logarithmic applications.

Technical Tidbit

Sputtering Targets

In this month's technical tidbit, we will discuss sputtering targets. Sputtering targets are used during physical vapor deposition to deposit metals, metal alloys, and some types of insulators.

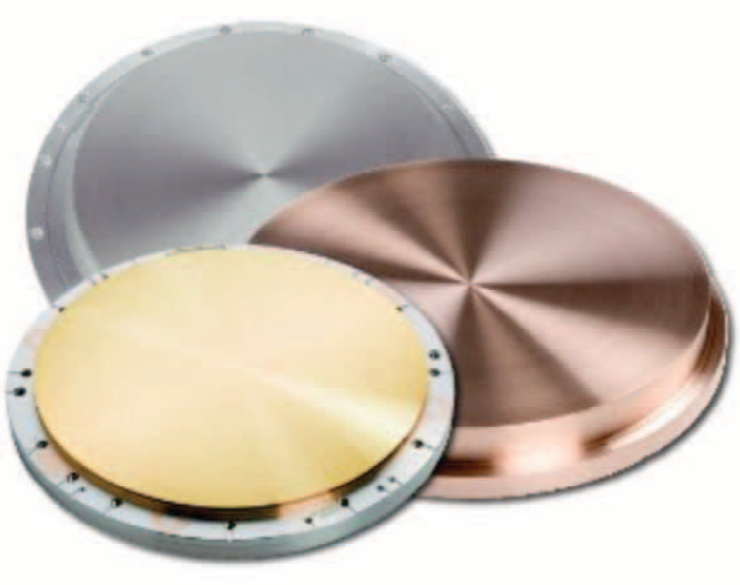


Figure 1.

These targets are formed from the metal to be deposited and must be of very high purity. Six nines purity is common for these materials. Manufacturers fabricate these targets using two different methods: melting and hot casting, or hot pressing of metal powders. The method will depend on the metal. Refractory metals such as titanium and tungsten are too difficult to handle in a molten state, so they are usually hot pressed. The typical shape is a circular disk, like we show in Figure 1. The diameter of these targets is approximately 1.5 times the diameter of the wafers on which the sputtered material will land. Some tools will use a three-dimensional hollow cathode or other designs rather than a solid target. This disk of material is then bonded to an ultrapure water-cooled backing plate, which is necessary to prevent target warpage, delamination, or even melting.

Figure 2.

Let's now make a few more comments about the sputter targets. The target is typically a combination of the metal to be deposited and a backing plate that can be cooled. There are companies that specialize in the target materials, like Reade Advanced Materials, and other companies that act as integrators, such as Honeywell Electronic Materials, Materion, and ULVAC. The key aspect of the target material is of course its purity, which we discussed earlier. Another key with a target is to ensure uniform sputtering, which in turn creates uniform deposition. One attains high uniformity by adjusting the metal microstructure. Utilizing a fine metal microstructure having a high degree of uniformity for example, allows uniform the magnetic flux leakage on the target surface of high purity cobalt targets. Also, process manufacturing should take product characteristics and contours into account during production. Sophisticated analysis/evaluation system such as Glow Discharge Mass Spectrometry ensure purity along with a high level of quality. Another key element of the target design is to avoid flaking or peeling, due to thermal coefficient of expansion mismatches. This means the target material and the backing plates need to be well matched. Gaseous elements are one factor in causing particle emissions especially in aluminum targets and suppliers are working to lower emissions by utilizing vacuum melting methods in the refining and ingot purification processes. Furthermore, the targets need to be effectively cooled in order to avoid problems like melting or warpage. Proper circulation of deionized water is therefore critical.

Ask the Experts

Q: Is 450mm processing likely to occur?

A: That depends on who you talk to. From our perspective at Semitracks, there are several important reasons to believe it may never occur:

1. Only a few companies are interested in pursuing the 450mm format.

2. In order for 450mm to be a success, we need a lithography tool at 450mm. ASML is very focused on making EUVL work and is not likely to devote significant resources to this until they have worked out the issues with EUVL. That is likely to take many years.

3. A fab can output a LOT of circuits using 300mm wafers. Therefore, very few applications can really take advantage of the larger wafer format.

4. It is unclear how much savings can result at 450mm, given the challenges with processing uniformity on that scale.

Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

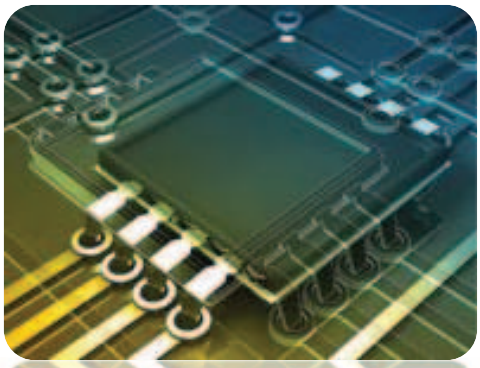
1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.
3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials

3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills
   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless
   f. Thermal Interface Materials (TIMs) and Lids
   g. Fine Pitch Warpage Reduction
   h. Stacked Die and Stacked Packages
   i. Material Selection for Board Level Temperature Cycling and Drop Reliability
4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic

7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Introduction to Processing
March 2 – 3, 2020 (Mon – Tue)
Portland, Oregon, USA

Failure and Yield Analysis
March 2 – 5, 2020 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
March 4, 2020 (Wed)
Portland, Oregon, USA

IC Packaging Technology
March 5 – 6, 2020 (Thur – Fri)
Portland, Oregon, USA

Semiconductor Reliability / Product Qualification
March 9 – 12, 2020 (Mon – Thur)
Portland, Oregon, USA

Wafer Fab Processing
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 30, 2020 (Thur)
Munich, Germany