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# InfoTracks

Semitracks Monthly Newsletter

## Latch-Up Overview Part 2

By Christopher Henderson

In this section, we will continue to discuss the topic of latch-up. We will discuss latch-up testing. We perform latch-up testing to determine the robustness of the device to latch-up, much like we perform ESD testing to determine the robustness of the device to ESD.

Latch-up testing can be accomplished with a latch-up test system. These systems are sometimes configured to do both ESD and latch-up. The standard for latch-up testing is JEDEC standard number 78. To perform latch-up testing, one must initialize the device with vectors to place the pins in appropriate conditions. Some pins may be more sensitive to positive transients than negative transients. The pins might also be more sensitive to latch-up when in a high state or a low state. There are two classes for latch-up testing: Class I, or room temperature, and Class II. For Class II testing at the maximum operating ambient temperature or case temperature, the value needs to be set at the required test value. For Class II testing at the maximum operating junction temperature, the ambient temperature or the case temperature should be selected to achieve a temperature characteristic of the junction temperature for a given device operating mode(s) during latch-up testing. The maximum operating ambient or case temperature during stress may be calculated based on the methods detailed in the appendix in the standard.

## In this Issue:



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| Test | Trigger | |
|---|---|---|
| | Force current/voltage | Voltage/current limits |
| Positive I-Test | <50 mA | See comments in next table |
| | 50 – 100 mA | |
| | 100 – 150 mA | |
| | 150 – 200 mA | |
| | > 200 mA | |
| Negative I-Test | >-50 mA | See comments in next table |
| | -50 – -100 mA | |
| | -100 – -150 mA | |
| | -150 – -200 mA | |
| | < -200 mA | |
| Over-voltage Test | 1.5×VDD or MSV, whichever is less | See comments in next table |

The operator pulses the device on non-supply pins with currents that are a certain number of milliamps above and below the normal current. The operator then pulses the device with voltage pulses on the supply pins that exceed the normal supply voltage by some amount. In most cases, we use 150% of the normal supply voltage. If the normal supply voltage is 2.5 volts, one would use voltage pulses of 3.75 volts. In some cases, it may be more appropriate to use the maximum stress voltage, MSV.

| Test Type | Trigger Polarity | Condition of untested pins | Test temp. classification | $V_{supply}$ conditions | Trigger test conditions for pin or supply group under test | Latch-up detection criteria |
|---|---|---|---|---|---|---|
| I-Test | Positive | Max Logic High | Temp. Class I Room Temp | Max. operating voltage for each $V_{supply}$ pin group per device spec. | See previous table for stress current range and clamp voltage | If absolute Inom is <25mA, then absolute Inom+10mA is used<br><br>or<br><br>If absolute Inom is >25mA, then 1.4× absolute Inom is used |
| | | Min Logic Low | | | | |
| | Negative | Max Logic High | Temp. Class II Max. ambient operating temp. | | | |
| | | Min Logic Low | | | | |
| $V_{supply}$ Over-voltage test | See latch-up waveforms voltage | Max Logic High | | | See previous table for stress voltage range and clamp current | |
| | | Min Logic Low | | | | |

The table above shows the test matrix. This includes four combinations of current testing, and two combinations of voltage testing. After the pulses are applied and while the device is still biased, the operator checks the supply current. The device is considered to be in latch-up if the supply current is 25 milliamps above the nominal operating current for low current devices, or 140% of the nominal current for high current devices.

Below are some comments regarding the test matrix.

1. Maximum logic high and minimum logic low shall be per the device specification. When logic levels are used with respect to non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specification.
2. During supply over-voltage latch-up tests, it is common to combine several IC supply pins of the same voltage into one supply group. It is necessary to combine supply pins into one group if they are connected internally. The current clamp for the supply group is set according to the total nominal supply current of the group.

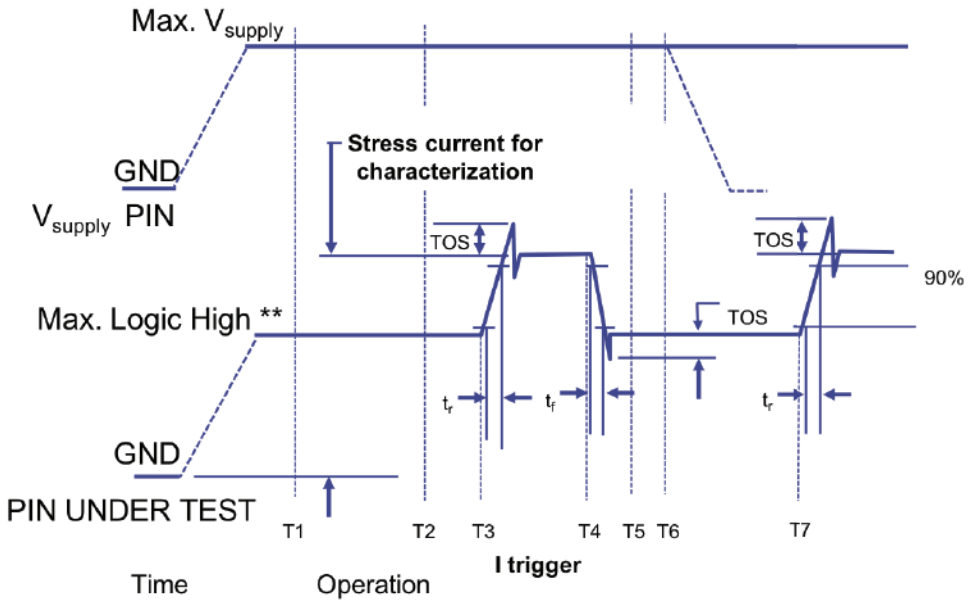
$$I_{Clampj} = 100mA + I_{nomj} = 100mA + \sum_{\text{All supplies in supply group j}} I_{nomi}$$

$$I_{Clampj} = 1.5 \times I_{nomj} = 1.5 \times \sum_{\text{All supplies in supply group j}} I_{nomi}$$

3. The pin clamping voltage for positive current-test is given by $V_{clamp}$ equal to $V_{max}$ + 0.5 ($V_{max}$ – $V_{min}$), with an upper limit of 1.5 x $V_{max}$ , where $V_{max}$, the logic high value, and $V_{min}$, the logic low value, are defined in the standard. If the Maximum Stress Voltage (MSV) for the pin is less than $V_{max}$ + 0.5 x the quantity $V_{max}$ – $V_{min}$, or 1.5 x $V_{max}$, then the pin clamping voltage is given by $V_{clamp}$ equal to the MSV. In some instances the forcing current required and the voltage limit may have opposite polarities. Two-quadrant power supplies are not capable of providing negative injection current with positive clamping voltage. Four-quadrant power supplies do not share this limitation.
   The pin clamping voltage for negative current-test is given by $V_{clamp}$ equal to $V_{min}$ – 0.5 x the quantity $V_{max}$ – $V_{min}$, with a lower limit of -0.5 x $V_{max}$, where $V_{max}$ the logic high value, and $V_{min}$ the logic low value, are defined in the standard. If the MSV for the pin is greater than $V_{min}$ – 0.5 x the quantity $V_{max}$ – $V_{min}$, or -0.5 x $V_{max}$, then the pin clamping voltage is given by $V_{clamp}$ equal to the MSV. In some instances the forcing current required and the voltage limit may have opposite polarities. Two-quadrant power supplies are not capable of providing negative injection current with positive clamping voltage. Four-quadrant power supplies do not share this limitation.
4. If the trigger test condition reaches the voltage of current clamp limit and latch-up has not occurred, the pin passes the latch-up test.
5. During the current test or supply overvoltage test, the supply currents for all supply groups are monitored for latch-up occurrence. Failure occurs if any supply current exceeds the limit in the table.
6. The trigger conditions are not indicative of appropriate trigger conditions for all devices. Appropriate trigger conditions may be more or less stringent. When trigger conditions used in testing differ from the table, the trigger conditions used must be defined in the test results.

| Symbol | Time Interval | Parameter | Limits | |
|---|---|---|---|---|
| | | | Min | Max |
| $t_r$ | | Trigger rise time | 5µs | 5ms |
| $t_f$ | | Trigger fall time | 5µs | 5ms |
| $T_{width}$ | T3 to T4 | Trigger duration (width) | $2 \times T_r$ | 1s |
| TOS | | Trigger over-shoot | +/- 5% of pulse voltage | |
| $T_{cool}$ | T4 to T7 | Cool down time | $> T_{width}$ | |
| $T_{measure}$* | T4 to T5 | Waiting time before measuring $I_{supply}$ | 3ms | 5s |
| *Wait time shall be sufficient to allow for power supply ramp down/stabilization of $I_{supply}$ | | | | |

The table above shows the timing specifications for the current and voltage waveforms. Notice that there is a trigger rise time, trigger fall time, trigger duration width, trigger over-shoot, cool down time, and wait time. Some of the timing limits are fairly wide, but they do need to be followed in order for the latch-up test to be a valid test.




In the illustration above we show a timing diagram for the positive current pulse test:

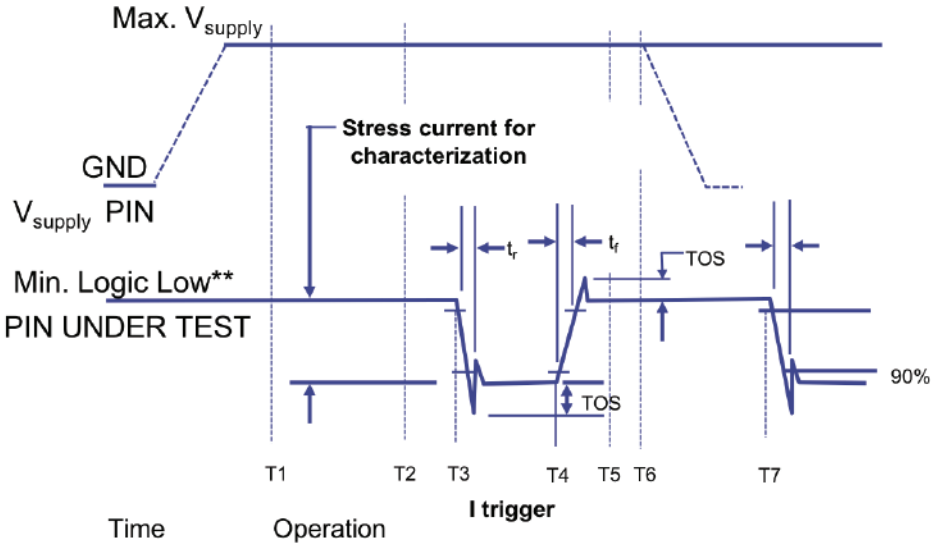
T1 to T2 - Measure nominal $I_{supply}$ (Inom).

T4 to T7 - Cool down time (T cool).

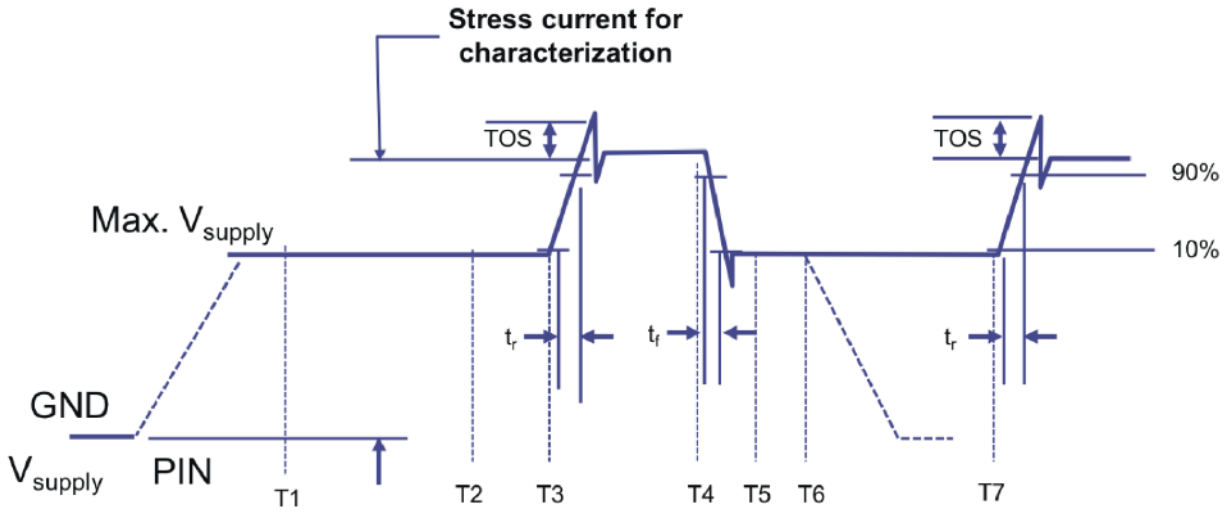
T4 to T5 - Wait time prior to $I_{supply}$ measurement.

T5 - Measure $I_{supply}$.

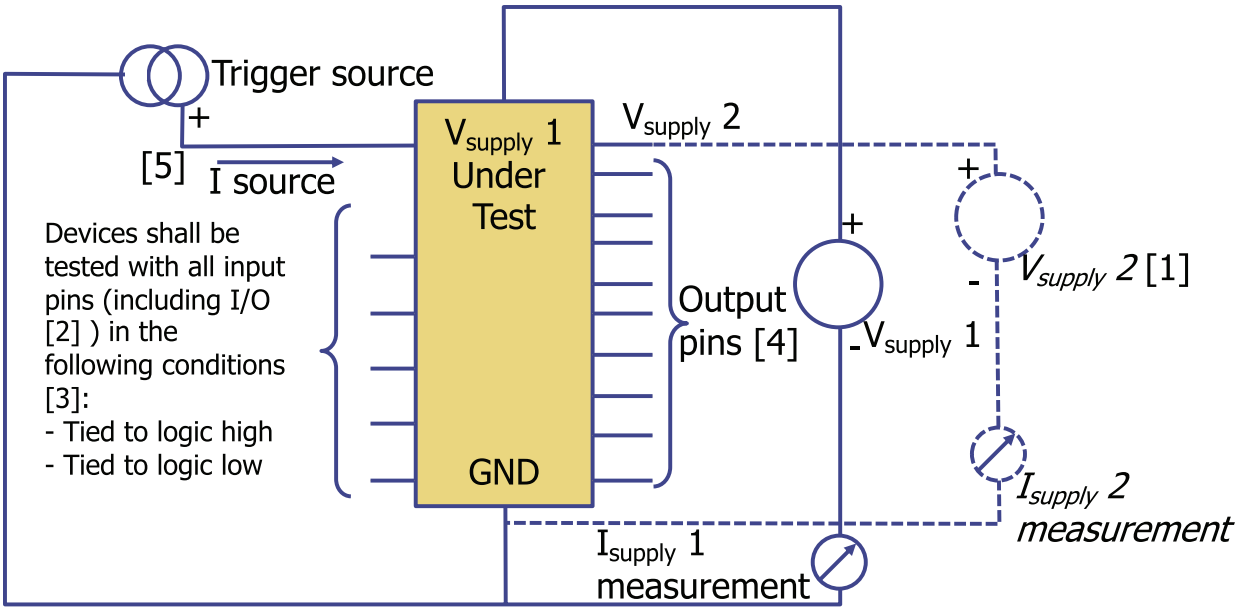
T6 - If any $I_{supply}$ value exceeds the failure criteria defined in the standard, latch-up has occurred and power must be removed from DUT.




In the illustration above we show a timing diagram for the negative current pulse test. It is similar to the positive test with just a few differences in the waveforms. As with the previous test, if any $I_{supply}$ exceeds the failure criteria defined in the standard, latch-up has occurred and power must be removed from DUT.

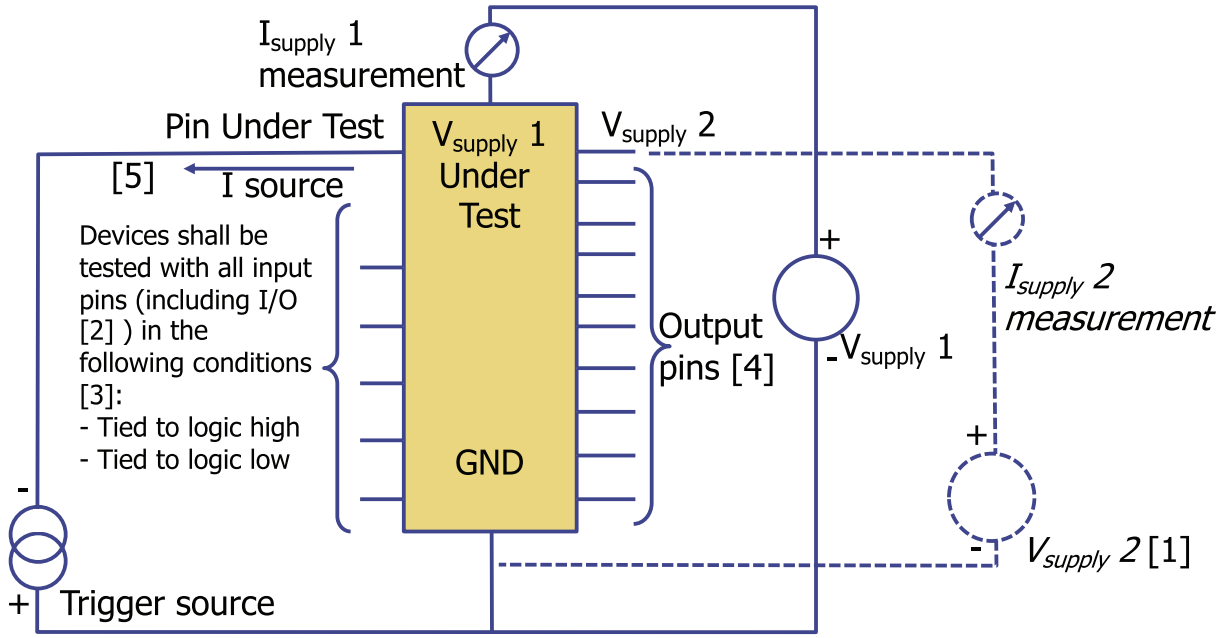



In the illustration above we show a timing diagram for the voltage pulse test. Like before, if any $I_{supply}$ exceeds the failure criteria defined in the standard, latch-up has occurred and power must be removed from DUT.

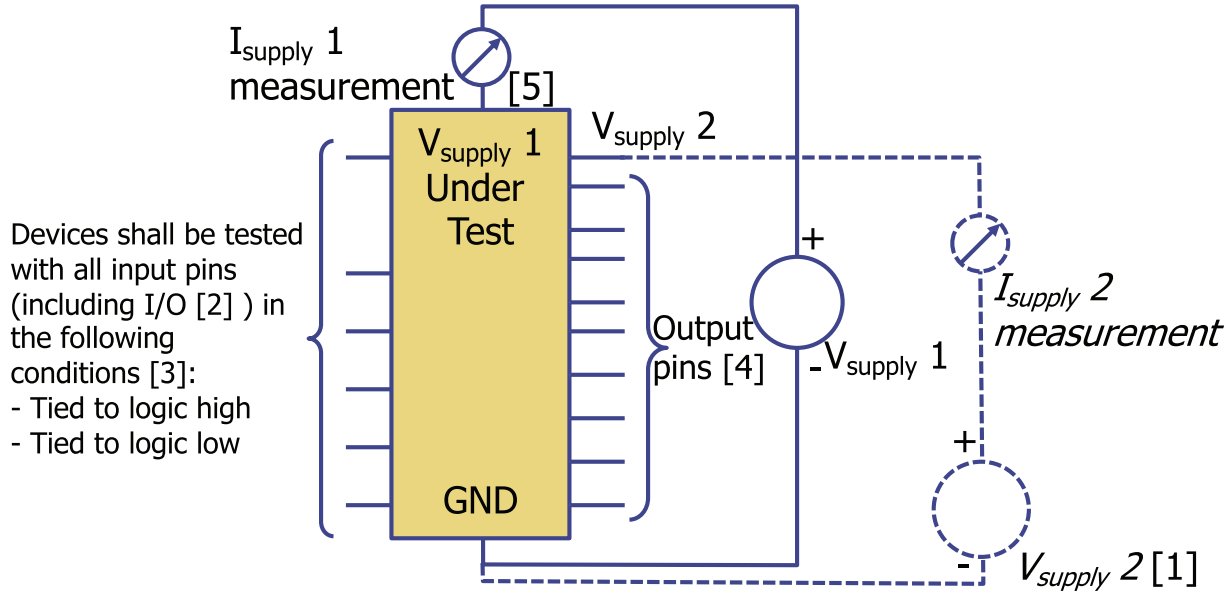



In the illustration above we show the circuit for positive current testing. The standard makes a few comments about the circuit:

1. The DUT biasing should include additional V supplies as required.
2. The DUT should be preconditioned so that all I/O pins are placed in a valid state per the standard. I/O pins in the output state should be open circuit.
3. The logic high and logic low values should be assigned per the device specification. When logic levels are used with respect to a non-digital device, it means the maximum high or minimum low voltage that can be supplied to the pin per the device specifications, unless these conditions violate the device setup condition requirements.
4. The output pins should be open circuit except when tested for latch-up.
5. The trigger test condition is defined in the standard. We should also note that dynamic devices may have timing signals applied per the standard.




And here in the illustration above we show the circuit for negative current testing.



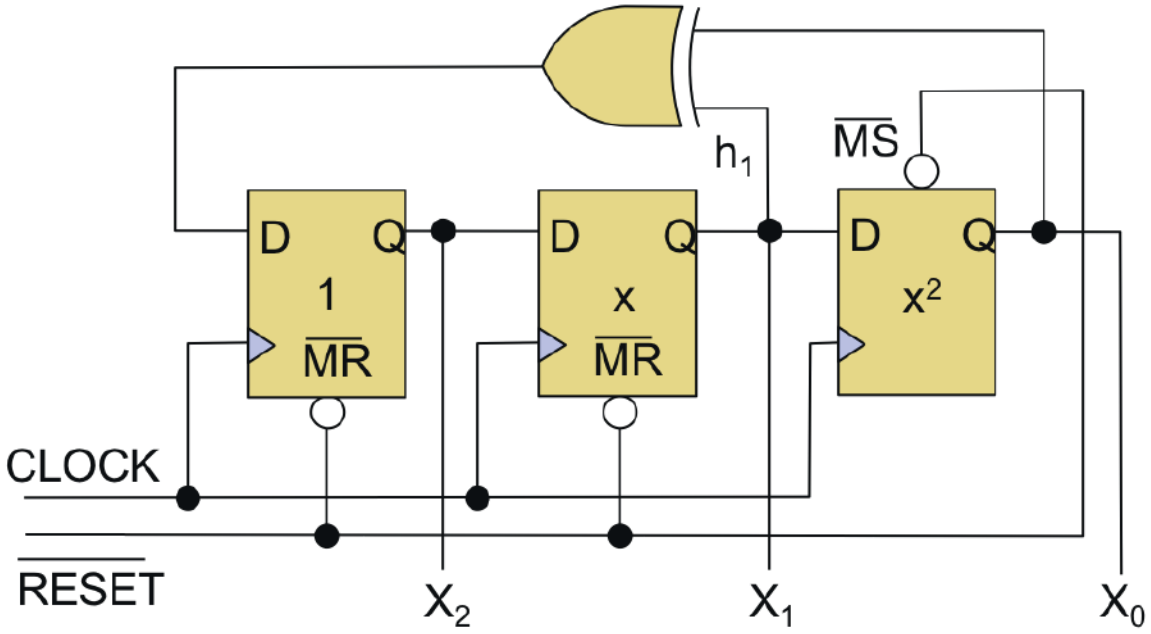

Finally, we show the circuit for over-voltage testing in the illustration above.

In conclusion, latch-up is a less common failure mechanism, but is still important to consider, as it can affect many CMOS circuits and potentially other circuits when PNPN subcircuits occur. The trigger modes are well understood, but the process, layout, and interactions between the two can make the problem quite complex to understand. As such, one may need simulation to predict results accurately. We discussed some basic protection techniques. Like ESD, there is a significant body of knowledge on latch-up protection in the literature. Finally, we discuss the JEDEC standard for latch-up testing, which is commonly used across most qualification documents.

## Technical Tidbit

### Linear Feedback Shift Registers

In this month's technical tidbit we will discuss an important building block for Built-In Self Test, the Linear Feedback Shift Register, or LFSR.




The most basic form of hardware generation circuit is the Linear Feedback Shift Register, or LFSR, like we show here. It consists of a number of D-flip-flops with a reset pin. In this example, we show a three-stage LFSR. To implement a characteristic polynomial, we can use feedback. In this example, to implement the function f (x) = 1 + x + x2, we insert an exclusive-OR gate in the feedback path, receiving one input from the 1's D-flip-flop and the X's D-flip-flop. This creates the polynomial value we wish to inject into the circuit. We should note that you read the taps from right to left in this schematic, rather than left to right. LFSRs can also be created using exclusive-NOR gates as well.

Next, we show the pattern sequence from the LFSR above.

$$\begin{array}{c|ccccccccc} X_0 & 1 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 \\ X_1 & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 \\ X_2 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \end{array} \quad \ldots$$

$$\begin{bmatrix} X_0 & (t+1) \\ X_1 & (t+1) \\ X_2 & (t+1) \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \begin{bmatrix} X_0 & t \\ X_1 & t \\ X_2 & t \end{bmatrix}$$

Note that we always have 1 and $x_n$ terms in the polynomial expression. When using an LFSR for Built-In Self Test, be sure to never repeat the LFSR pattern more than one time; otherwise, it repeats the same error vector and will cancel the fault effect.

## Ask the Experts

**Q: Do you offer any courses for Quality Engineers?**

**A:** Several people have asked about this. We are currently working on several Quality-related courses that will be added into our Online Training System within the next 3 – 6 months. Once everything is up and running for these courses, we will make an announcement.

# Spotlight: Failure and Yield Analysis

## OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

## COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

## INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

## THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

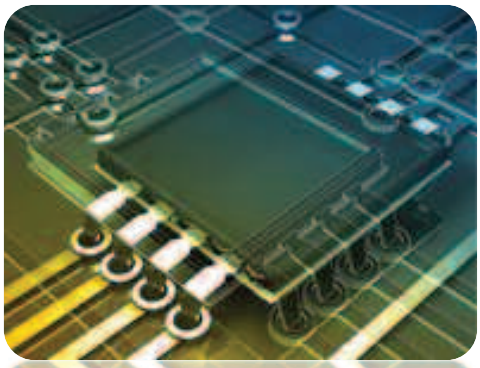
One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

## COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques

7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy
8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS

14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories



# Upcoming Courses

(Click on each item for details)

**Failure and Yield Analysis**
October 29 – November 1, 2018 (Mon – Thur)
Singapore

**Failure and Yield Analysis**
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

**Wafer Fab Processing**
April 23 – 26, 2019 (Tue – Fri)
Munich, Germany

**EOS, ESD and How to Differentiate**
April 29 – 30, 2019 (Mon – Tue)
Munich, Germany

**Semiconductor Reliability / Product Qualification**
May 6 – 9, 2019 (Mon – Thur)
Munich, Germany

**Semiconductor Reliability / Product Qualification**
May 13 – 16, 2019 (Mon – Thur)
Tel Aviv, Israel

**Introduction to Processing**
June 3 – 4, 2019 (Mon – Tue)
San Jose, California, USA

**Failure and Yield Analysis**
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA

**Advanced CMOS/FinFET Fabrication**
June 5, 2019 (Wed)
San Jose, California, USA

# Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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http://www.semitracks.com

*To post, read, or answer a question, visit our forums.*
*We look forward to hearing from you!*