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Optical Pyrometry Part 1

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In this section, we will discuss a technique used to measure surfaces at high temperatures known as Optical Pyrometry. Semiconductor equipment manufacturers will use this technique to measure high temperatures in such applications as Chemical Vapor Deposition, Rapid Thermal Processing, Thermal Diffusion, and other high-temperature processing techniques.

The outline is shown here. First, we'll discuss the basics of optical pyrometry, followed by the equipment used for the technique. We'll then discuss techniques to improve the range and sensitivity of the technique, along with issues associated with the technique. Finally, we'll provide a conclusion for this technique.

Optical pyrometry takes advantage of the fact that a hot surface will emit infrared energy that can be detected. The peak wavelength and energy density allow the user to determine the temperature of the object fairly precisely. Optical pyrometry is a non-contact technique, and its major strength is being able to measure high temperatures (above 500°C). Engineers use this technique to measure temperatures during wafer fabrication processes like Chemical Vapor Deposition, Rapid Thermal Annealing, Atomic Layer Deposition, and others.

Optical pyrometry is based on black body radiation physics, so let's briefly review blackbody physics. In classical physics, the spectral radiancy, R sub T of nu, is the spectral distribution of energy emitted by a blackbody. It is defined so that R sub T of nu d nu is the energy

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emitted per unit time in the frequency range of nu to nu plus d nu from a unit area on a surface at a temperature T. If one integrates over all of the frequencies, one gets the radiancy given by the equation shown here.

$$R_T = \int_0^\infty R_T(\nu)d\nu$$

The radiancy is related to the temperature of an object by a property called Stefan's Law.

$$R(T) = \sigma T^4$$

It states that the radiancy is proportional to the temperature raised to the fourth power. The proportionality constant, sigma, is the Stefan-Boltzmann constant, which is equal to 5.67×10^{-8} watts per meter squared, degrees kelvin to the fourth power.

$$\sigma = 5.67\times10^{-8}\frac{W}{m^2K^4}$$

Most objects are not blackbodies, therefore one needs to take into account the emissivity of the object. The emissivity, e, can be factored into Stefan's Law as follows. The radiancy is equal to the emissivity times the Stefan-Boltzmann constant times T to the fourth power.

$$R(T) = e\cdot\sigma T^4$$

Another important factor required for infrared thermography is Wein's displacement law. Wein's displacement law relates the temperature to the wavelength peak.

$$\lambda_{MAX} = \frac{2.898\times10^{-3}}{T}$$

The maximum in the spectrum is inversely proportional to the temperature. The higher the temperature, the shorter the peak in the wavelength, and the finer the resolution that is possible.

If one assigns an average energy kT to each mode of the spectral radiancy, one gets the classical solution called the Rayleigh-Jeans formula for blackbody radiation.

$$\rho(\nu)d\nu = \frac{8\pi\nu^2kT}{c^2}d\nu$$

This assumes that the Equipartition Theorem holds true. The Equipartition Theorem is a principle of classical statistical mechanics which states that the internal energy of a system composed of a large number of particles will distribute itself evenly among each of the degrees of freedom allowed to the particles of the system. Unfortunately, this solution does not work for shorter wavelengths because it would assume an infinite energy density. This led to what is known as the ultraviolet catastrophe. Several years later, Max Planck examined the Rayleigh-Jeans formula in light of quantum mechanics. Planck derived a new equation based on quantized energy units, shown here.

$$\rho_T(\nu)d\nu = \frac{8\pi\nu^2}{c^3}\cdot\frac{h\nu}{e^{h\nu/kT}-1}d\nu$$

This equation works over the entire spectrum.

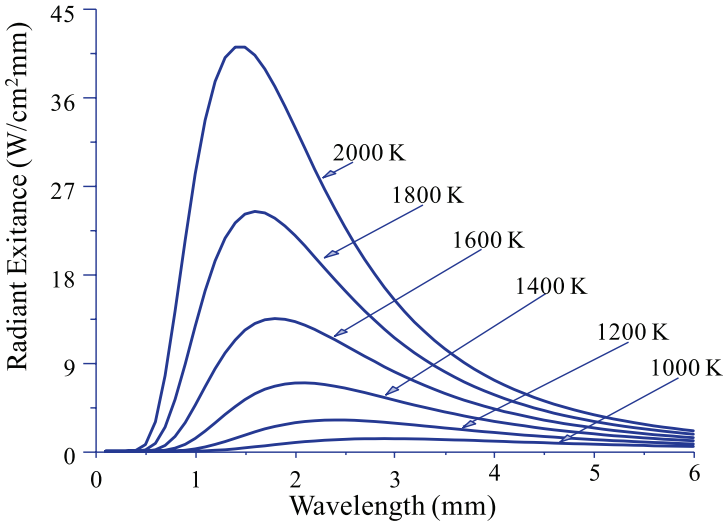


Figure 1. Blackbody radiation: 1000°K to 2000°K.

If one plots the radiancy versus wavelength, the relationship can be seen (Figure 1). Notice that as the temperature increases, the peak in the radiancy moves toward shorter wavelengths.

As we discussed earlier, the radiancy therefore of a body is related to the radiancy of a blackbody by the emissivity.

$$R_T = e \cdot R_{TBB}$$

In order to obtain a correct temperature reading, the radiance reflected by the sample must be taken into account.

$$R_{Total} = R_T + (1 - e)R_0$$

If we combine the two equations shown here, we can obtain an equation that gives an accurate measurement of any particular body.

$$R_{Total} = e \cdot R_{TBB} + (1 - e)R_0$$

Material	Emissivity
Ideal black body	1.00
Lampblack	.95
Asbestos paper	.95
White Lacquer	.95
Bronze paint	.80
Carbon, rough plate	.76
Oxidized steel	.70
Polished brass, oxidized copper	.60
Aluminum paint	.55
Oxidized monel metal	.43
Cast iron - polished	.25
Copper - polished	.15
Silicon (lightly doped)	.12
Aluminum - highly polished	.08
Platinum - highly polished	.05
Silver - highly polished	.02

Figure 2. Emissivities of common materials.

Emissivities can vary quite widely for various materials. This chart shows some common materials and their emissivities. An object that absorbs light has a high emissivity, like lampblack, while an object that reflects light has a low emissivity, like highly polished silver. Notice that materials used in semiconductor devices, like aluminum and copper, have low emissivities. One needs to take this into account when examining these devices. Lightly doped silicon has an emissivity of around .12 at room temperature.

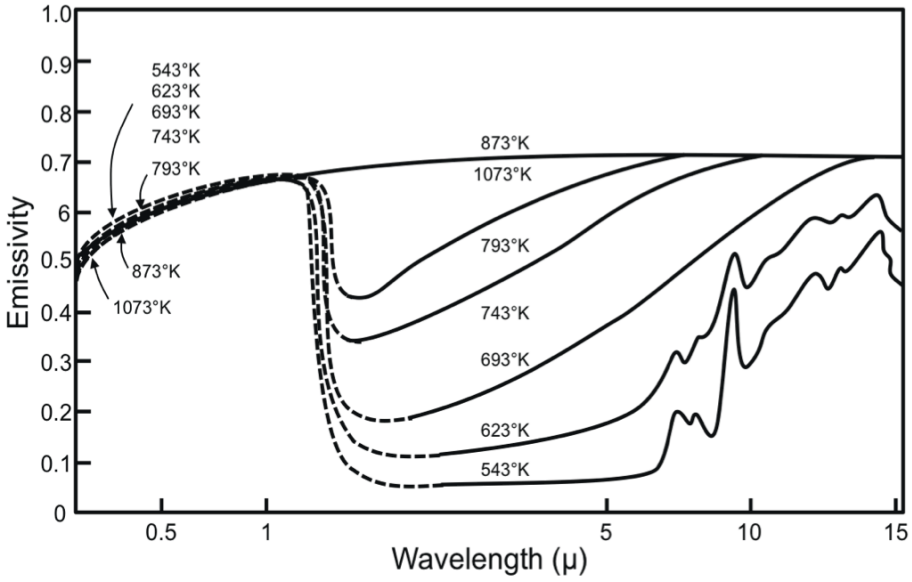


Figure 3. Silicon emissivity.

However, silicon emissivity is not just a single number. Here we show a plot of silicon emissivity as a function of wavelength and temperature. Notice that the emissivity of silicon changes with temperature, and it also changes with frequency, so depending on what temperature the wafer is and what wavelength you're examining, you will get different results. Furthermore, this will also be the case with other thin films like silicon dioxide, silicon nitride, aluminum, copper, and so forth. Further complicating matters is the fact that the strength of the emissivity increases strongly with temperature.

To be continued in the November 2017 issue.

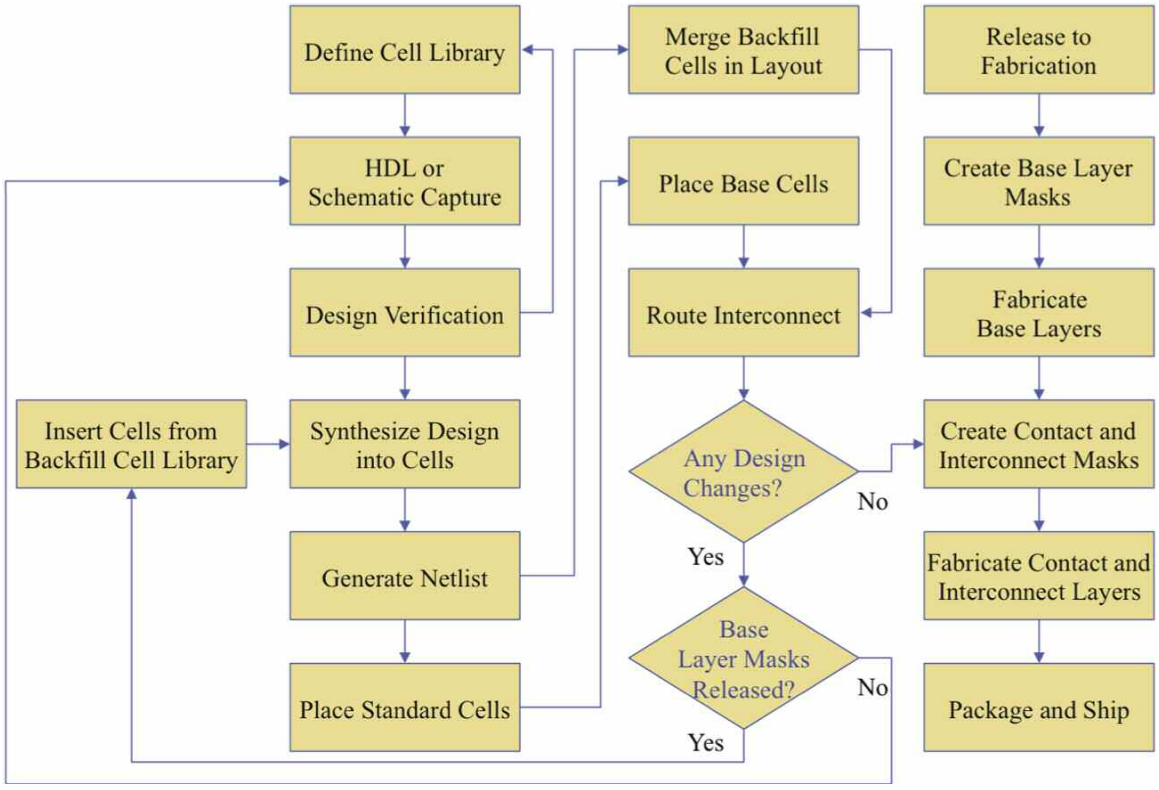
Technical Tidbit

Extra Cells in Design

One design concept that has some appeal is to add additional unused gates or standard cells into a layout to permit easy modification, should changes be necessary.

One method of minimizing the effect of design changes in the fabrication process is to add extra standard cells into the initial layout definition, which could then be used if the design engineers believe a change is necessary. One could add extra NOR or NAND gates for example, throughout the standard cell layout. There are some issues with this approach though. First, these gates will only perform the functions of the gates themselves, not necessarily what is needed to fix the design. Second, these extra cells add area to the chip, which in theory reduces the yield. Third, this reduces the placement and routing optimization of the rest of the circuit. And fourth, this concept will not work well for analog circuits, since most analog circuits will require custom layout and placement in order to provide the proper performance and precision.

The gate array is perhaps the oldest example of a chip technology where one can make modifications easily. In a gate array approach, the manufacturer creates a regular array of transistors and fabricates them up through the contact or metal-1 portion of the process. Customers can then create a design, and this design can be personalized onto the base wafer through the interconnects and the vias. This



approach has the advantage that the chip can be fabricated more quickly (provided the base layers are already present), and the mask costs are lower because the customer only has to pay for the masks that create the interconnect layers. In theory, this type of technology would also be useful to make FIB modifications more easily, since unused transistors would be available for wiring. However, there are issues with this technology. It is a non-optimized technology; transistor performance is uniform, but gate and analog circuit performance cannot be easily optimized. Second, from the perspective of FIB circuit modifications, one would have to drill down to metal-1 or polysilicon in order to make the connections, which can be difficult in a chip with many interconnect levels. And third, this technology is not widely available as an option. Most designers instead use the Field Programmable Gate Array, which is highly configurable and easy to modify.

On the previous page is the basic process flow for adding in extra gates and utilizing them. This flow assumes a base wafer fabrication step, followed by a “personalization” step using contacts, vias, and metal. This approach can also be used in conjunction with a focused ion beam system, where the engineer could test the fix more easily before correcting the problem in the design.

Ask the Experts

Q: What are some common causes of CVD non-uniformities?

A: CVD non-uniformities can be due to several causes. Here are the main ones.

1. Temperature non-uniformities in the chamber can create problems if the CVD reaction is in the reaction-rate limited regime. CVD reactions typically increase exponentially with temperature, so a temperature gradient or change can create a problem. This might be caused by non-uniform heating in the chamber, or non-uniform heating of the chuck, or convection within the chamber.
2. Gas flow non-uniformities in the chamber can create problems. The gas flow across the surface will be a function of the chamber shape, the location of the gas flow injectors, the topography on the wafer, and even subtle features like the notch on the wafer.
3. Batch processing non-uniformities can also create problems. The gas flow and temperature profiles around a batch of wafers is even more complex. Many times, the scientists and engineers at the equipment manufacturing companies will do a computational fluid dynamics study to understand the gas flow and temperature properties within the system.

Spotlight: EOS, ESD, and How to Differentiate

OVERVIEW

Electrical Overstress (EOS) and Electrostatic Discharge (ESD) account for most of the field failures observed in the electronics industry. Although EOS and ESD damage can at times look quite similar to each other, the source each and the solution can be quite different. Therefore, it is important to be able to distinguish between the two mechanisms. The semiconductor industry needs knowledgeable engineers and scientists to understand these issues. ***EOS, ESD, and How to Differentiate*** is a two-day course that offers detailed instruction on EOS, ESD and how to distinguish between them. This course is designed for every manager, engineer, and technician concerned with EOS, ESD, analyzing field returns, determining impact, and developing mitigation techniques.

Participants learn to develop the skills to determine what constitutes a good ESD design, how to recognize devices that can reduce ESD susceptibility, and how to design new ESD structures for a variety of technologies.

1. **Overview of the EOS Failure Mechanism.** Participants learn the fundamentals of EOS, the physics behind overstress conditions, test equipment, sources of EOS, and the results of failure.
2. **Overview of the ESD Failure Mechanism.** Participants learn the fundamentals of ESD, the physics behind overstress conditions, test equipment, test protocols, and the results of failure.
3. **ESD Circuit Design Issues.** Participants learn how designers develop circuits to protect against ESD damage. This includes MOSFETs, diodes, off-chip driver circuits, receiver circuits, and power clamps.
4. **How to Differentiate.** Participants learn how to tell the difference between EOS and ESD. They learn how to simulate damage and interpret pulse widths, amplitudes and polarity.
5. **Resolving EOS/ESD on the Manufacturing Floor.** Participants see a number of common problems and their origins.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of electrical overstress, the models used for EOS, and the manifestation of the mechanism.
2. Participants will understand the ESD failure mechanism, test structures, equipment, and testing methods used to achieve robust ESD resistance in today's components.
3. The seminar will identify the major issues associated with ESD, and explain how they occur, how they are modeled, and how they are mitigated.
4. Participants will be able to identify basic ESD structures and how they are used to help reduce ESD susceptibility on semiconductor devices.
5. Participants will be able to distinguish between EOS and ESD when performing a failure analysis.
6. Participants will be able to estimate a pulse width, pulse amplitude, and determine the polarity of an EOS or ESD event.
7. Participants will see examples of common problems that result in EOS and ESD in the manufacturing environment.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, written text material, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The course notes offer dozens of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Introduction
   a. Terms and Definitions
   b. ESD Fundamentals
   c. EOS Fundamentals
2. Electrical Overstress Device Physics
   a. Sources of EOS
   b. EOS Models
   c. Electrothermal Physics
3. Electrostatic Discharge Device Physics
   a. ESD Models
   b. ESD Testing and Qualification
   c. ESD Failure Criteria
   d. Electrothermal Physics
   e. Electrostatic Discharge Failure Models
   f. Semiconductor Devices and ESD Models
   g. Latchup
4. EOS Issues in Manufacturing
   a. Charging Associated with Equipment
      i. Testers
      ii. Automated Handling Equipment
      iii. Soldering Irons
   b. Charge Board Events
   c. Cable Discharge Events
   d. Ground Loops/Faulty Wiring
   e. Voltage Differentials due to High Current
   f. Event Detection

Day 2

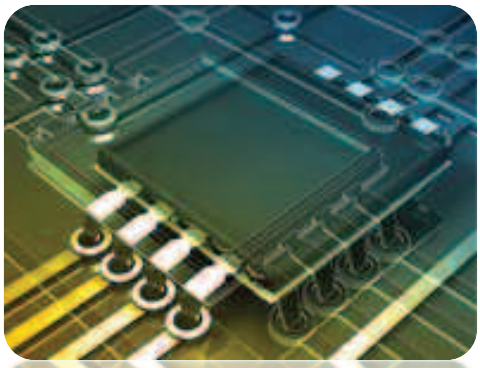
5. ESD Protection Methods
   a. Semiconductor Process Methods
   b. MOSFET Design
   c. Diode Design
   d. Off-Chip Drivers
   e. Receiver Networks
   f. Power Clamps
6. Differentiating Between EOS and ESD
   a. EOS Manifestation
   b. ESD Manifestation
   c. Circuit considerations
      i. Chip level
      ii. System level
   d. Simulating ESD
   e. Simulating EOS
7. EOS/ESD Design and Modeling Tools
   a. Electrothermal Circuit Design
   b. Electrothermal Device Design
   c. ESD CAD Design

ISTFA/2017

International Symposium for Testing and Failure Analysis

November 5-9, 2017
Pasadena Convention Center
Pasadena, CA, USA

Registration is available at
https://register.rcsreg.com/r2/istfa2017/ga/top.html



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Upcoming Courses

(Click on each item for details)

Failure and Yield Analysis
March 19 – 22, 2018 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
March 26 – 29, 2018 (Mon – Thur)
Portland, Oregon, USA

Failure and Yield Analysis
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Wafer Fab Processing
April 9 – 12, 2018 (Mon – Thur)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 16 – 19, 2018 (Mon – Thur)
Munich, Germany