Issue 137 November 2020

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Semitracks Monthly Newsletter

Photonics Device Fundamentals

By Christopher Henderson

In this month's feature article, we will conclude our series on photonics device fundamentals. This is the fourth in a series of four articles. This month we discuss the behavior of several detectors and modulators.

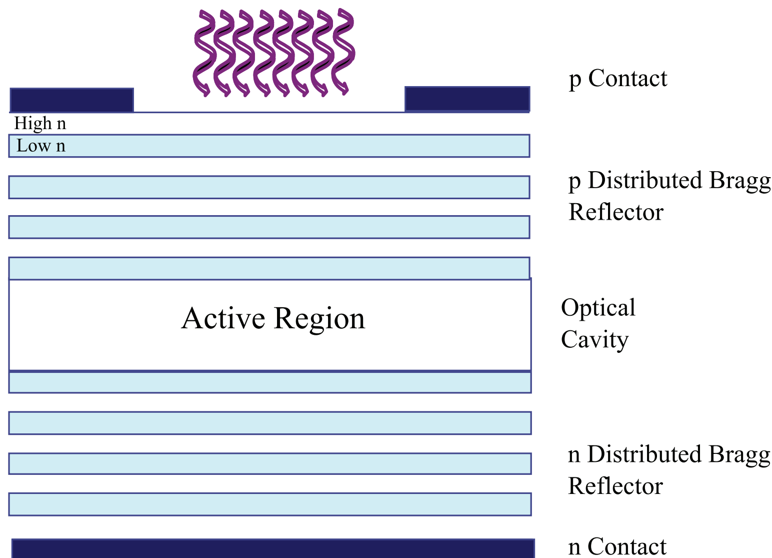

Figure 24. Resonant cavity photodiode.

Next, let's discuss the resonant cavity photodiode. We showed Figure 24 previously as Figure 15, but now let's talk about a second

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aspect of this structure. The active region acts as an optical cavity to create a resonant frequency that generates a specific wavelength of light. The Distributed Bragg Reflector (DBR) structure reflects the light to help create the resonant frequency and amplify the intensity.

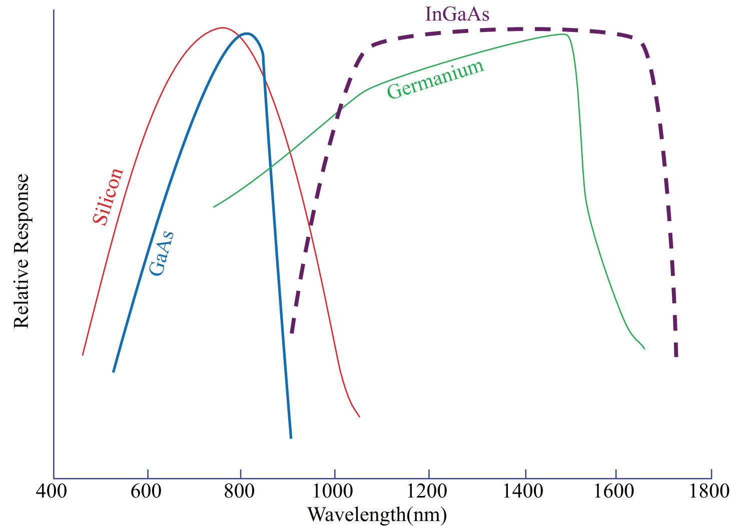


Figure 25. Spectral response of a few detector materials.

Here in Figure 25, we show the spectral response of several detector materials. We show Si in red, GaAs in blue, Ge in green, and InGaAs in magenta. The response of these detector materials is related to the bandgap of the materials.

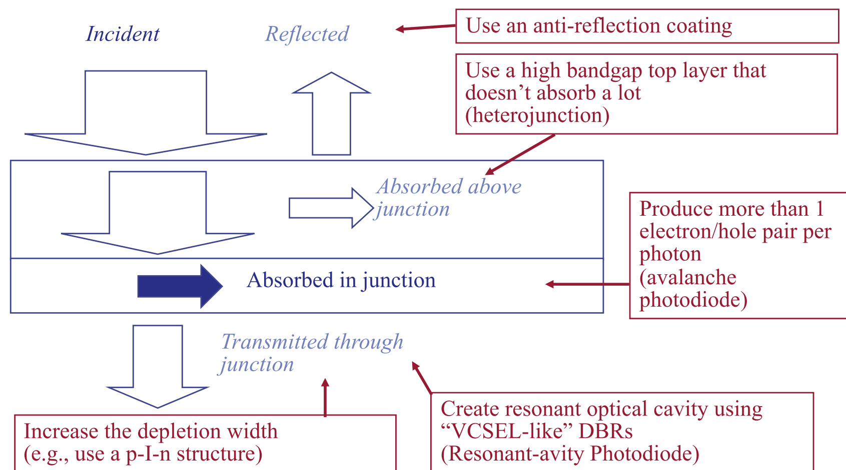
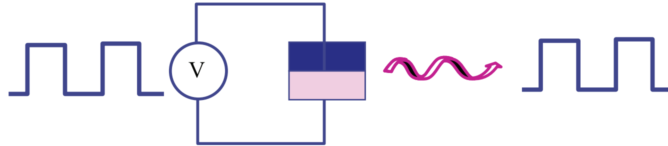


Figure 26. How to improve detector efficiency.

The challenge with detectors is how do we improve the detector efficiency. As illustrated by Figure 26, there are five important factors to help improve efficiency. The first is to increase the depletion width. We already discussed an important method to do this, which is the p-i-n structure. The second is to create a resonant optical cavity structure using Distributed Bragg Reflection. In this case, we use the approach in

the detector rather than in the laser diode. The third is to produce more than one electron-hole pair per photon. The avalanche photodiode can enable this possibility. The fourth is to use a high bandgap top layer that doesn't absorb photons to the degree that the detector material does. Finally, the fifth is to use an anti-reflection coating to prevent the photons from reflecting off of the interface and never reaching the semiconductor junction.



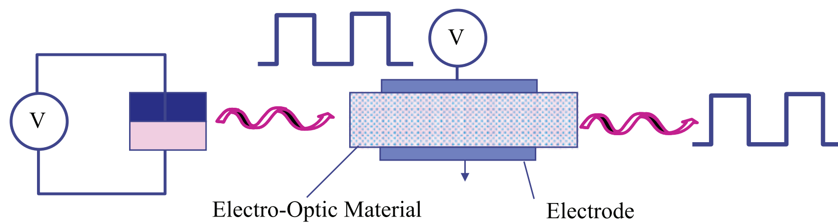


Figure 27. Direct vs. optical modulation.

Next, let's discuss modulation. There are two forms of modulation: direct and optical. In direct modulations, we vary the voltage to the laser diode, like we show here at the top of Figure 27. In optical modulation (as illustrated at the bottom of Figure 27), we vary the voltage to the electro-optical materials. The change in the electric field changes the index of refraction or the absorption coefficient, or potentially both parameters.

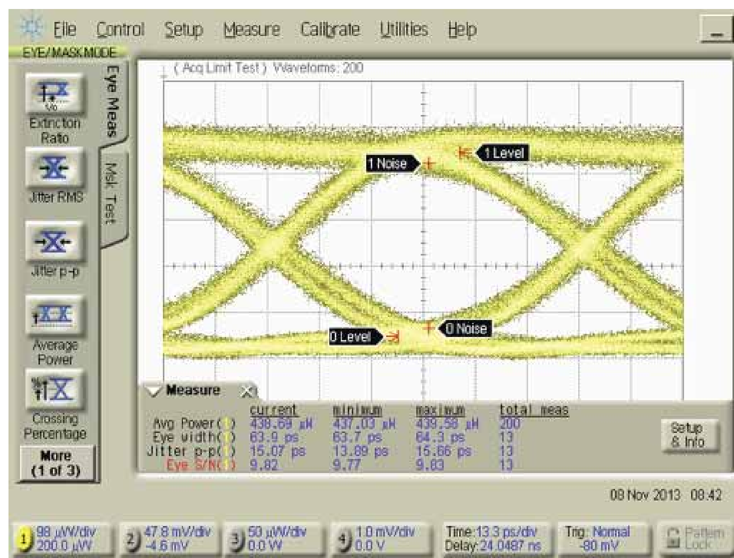


Figure 28. Example of optical data eye diagram (15Gb/s).

One can examine the behavior of modulation by looking at an eye diagram. This is an example of an optical data eye diagram in Figure 28.

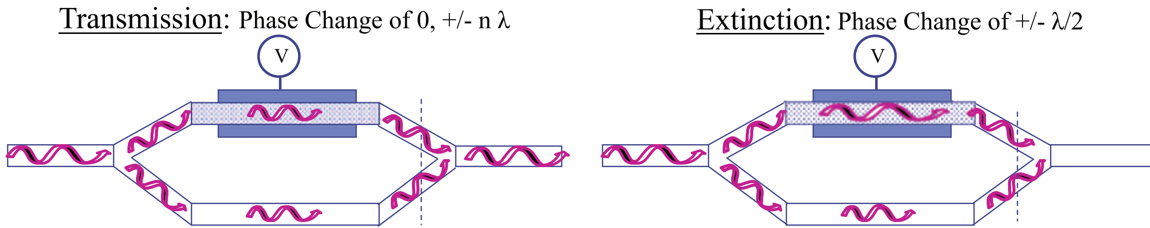


Figure 29. Mach-Zehnder modulators (MZM).

One common modulator used in optical communications is the Mach-Zehnder modulator. Mach-Zehnder modulators can operate in either a transmission or an extinction mode, as shown in Figure 29. In the transmission mode, one can modulate the signal by producing a phase change of 0 or plus or minus integer units of the wavelength of the light. The waves physically add to one another. In the extinction mode, one can modulate the signal by producing a phase change of plus or minus half-integer units of the wavelength of the light. This causes destructive interference, which reduces the amplitude of the signal. In the case of equal amplitudes in both paths, the signal is cancelled.

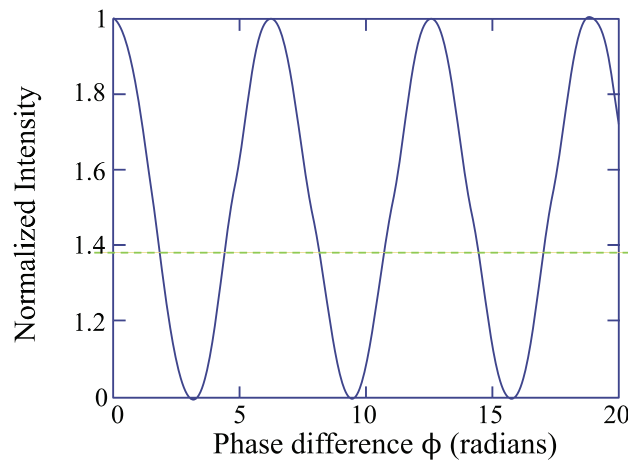


Figure 30. The normalized transfer function of a Mach-Zehnder interferometer.

One can more broadly consider the Mach-Zehnder modulator in terms of a transfer function, like we show here in Figure 30. Clearly if the two arms of the interferometer have identical propagation constants, the transfer function will be a maximum when the path length difference, the absolute value of L_2 minus L_1, results in a phase difference of a multiple of 2π radians. Similarly, the transfer function will have a minimum when the phase difference is a multiple of π radians.

Next, let's discuss some important electro-optical effects. The index of refraction changes with the electric field. This can be expressed by the equation shown here,

$$\Delta\left(\frac{1}{n^2}\right) = rE_{field} + sE_{field}^2 + \ldots$$

where there is a linear term, a squared term, a cubic term, and so on. The linear term is known as the Pockels effect. This factor is strong in certain optoelectronic materials such as $LiNbO_3$, a dielectric

material, and semiconductors such as GaAs and InP. The squared term is known as the Kerr effect. It is strong in polar liquids like nitro-benzene, and in silicon non-crystals.

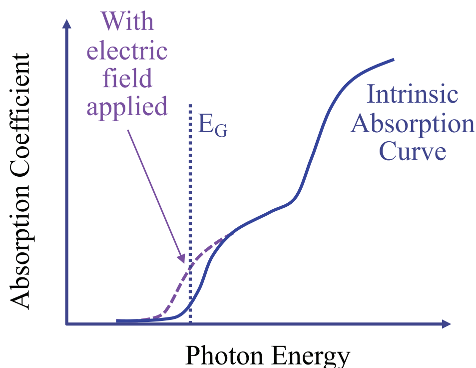


Figure 31. llustration of Franz-Keldysh effect.

Another electro-optical effect is the Franz-Keldysh effect. The band bending under an electric field allows absorption at photon energies slightly below the bandgap energy, like we show in Figure 31. It also changes the index of refraction. Engineers can use this effect in crystalline silicon to enable electro-optical probing of circuits as well.

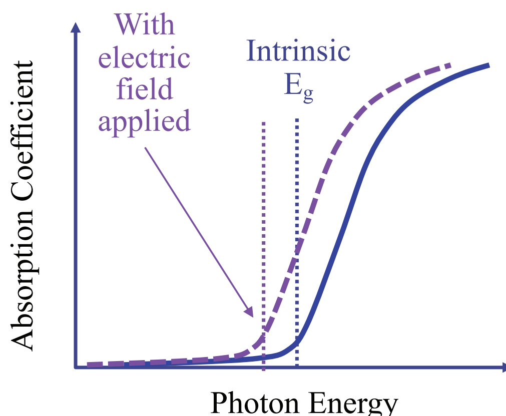


Figure 32. Illustration of Stark effect.

Yet another effect is the Stark effect. The electric field will distort the shape of the electron orbitals. This decreases the effective bandgap energy, which changes the index of refraction and the absorption coefficient, like we show in Figure 32. This effect is strongest in quantum well structures.

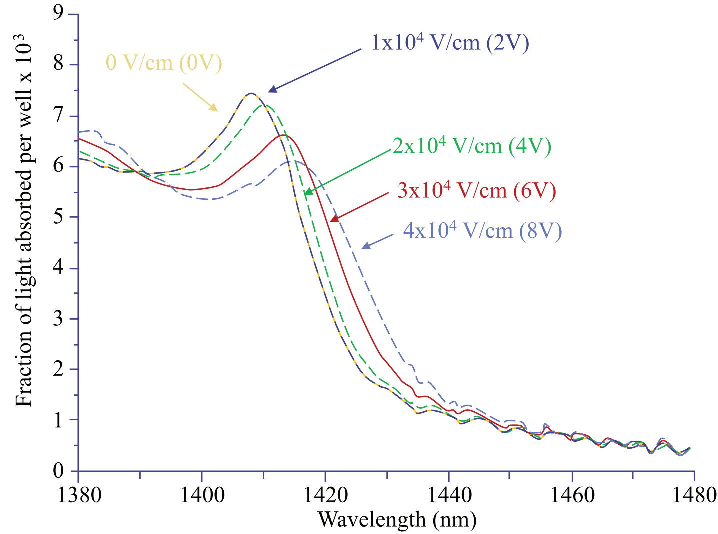


Figure 33. Examples of Stark effect in quantum well structure.

These curves in Figure 33 show examples of the Stark effect in a quantum well structure. Notice that the fraction of the absorbed light lowers significantly with an increase in electric field.

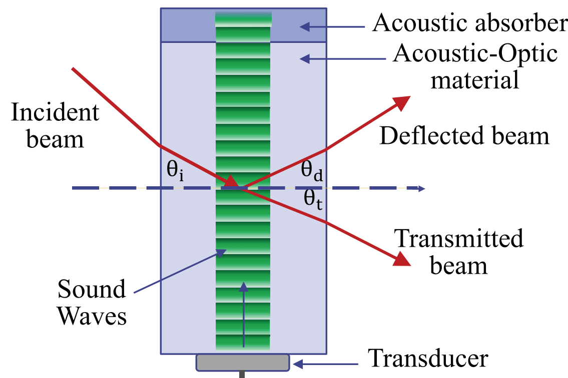


Figure 34. Illustration of acousto-optic effect.

The final effect is the acousto-optic effect. When an oscillating electric signal drives a transducer, it creates sound waves or a periodic expansion and compression in a transparent material or medium. The strain produced in the medium will alter the index of refraction. The incoming light will then scatter off the resulting periodic index modulation that occurs due to the acousto-optic effect, and interference occurs that is similar to Bragg diffraction.

Technical Tidbit

Wafer Thinning

This month's Technical Tidbit covers wafer thinning. This is an important technology for many ICs sold today that go into small spaces, like smart phones, memory modules, smart watches, and other portable electronics systems.

Wafer thinning technology became important as the demand for ultra-thin die used in stacked die packages, IC cards, and other applications increased. Early on, the two major drivers were stacked die packages where die on the order of 25-50 microns were used, and IC cards, or Smart Cards as they're sometimes called, where the target thickness of the die was between 30 and 80 microns.

Figure 1. Smart Card (left) and Stacked Die Structure (right).

Die thinning is essential in stacked die packaging because it reduces the package height and enables the addition of dice without increasing overall height within packages that contain stacked die systems. Smart cards and RFID cards are very thin single-die applications that represent an important electronics application with thin wafer requirements. A typical wafer is approximately 750µm thick and can be mounted in a lead frame or on a BGA substrate with half that thickness. Therefore, in order to maintain an overall molded package height of less than 1.2 mm, smart cards require thinning, and stacked die applications require significant thinning. Figure 1 shows an example of a smart card on the left, and a stacked die structure on the right.

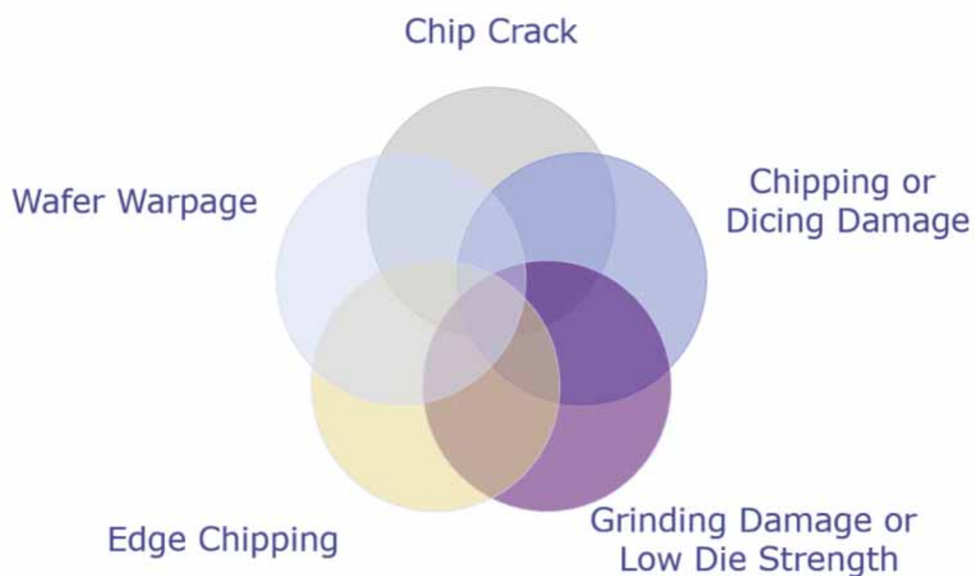


Figure 2. Issues with Wafer Thinning.

Figure 2 shows the challenges associated with wafer thinning. They include chip cracking from handling, chipping or damage associated with the dicing process from the wafer saw, damage from grinding, or loss of die strength from thinning, edge chipping, and wafer warpage. We will concentrate on wafer warpage and grinding damage, since they cannot easily be avoided through improved process control.

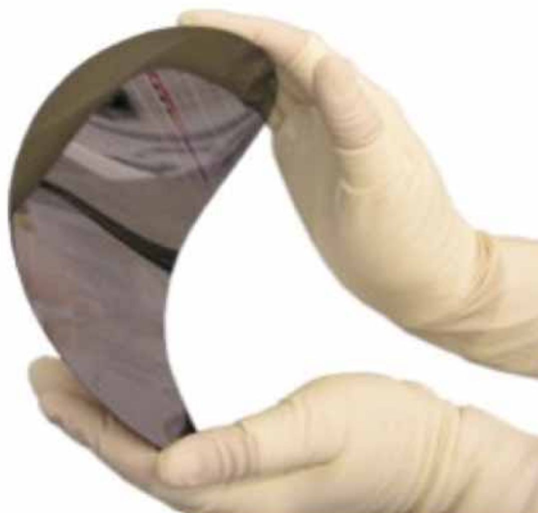


Figure 3. Image of Wafer after Back-Grinding.

The most common method of wafer thinning is back-grinding. It is traditionally used to remove excess silicon from the wafer backside. This wafer thinning method offers high throughput and a working wafer thickness down to 50µm. The most aggressive techniques in grinding and polishing today can achieve a thickness of ~30µm without etch or plasma processing. However, it generally leaves small surface defects. It is essentially a dry CMP process, employing a fibrous pad with oxide. Figure 3 shows an example of a wafer after the back-grinding process.

Figure 4. Chemical Etch System for Wafer Thinning (left) and Plasma Etch System for Wafer Thinning (right).

If the application requires a wafer thickness below 50µm, then wet etching or plasma processes are used. Although they are slower and more expensive, these processes exert much less stress and damage to the wafer. As of this writing, dice with a thickness of 50µm are in limited production, and dice with thicknesses of 25 or even 15µm are in development. A typical process would first use back-grinding, followed by a wet etch for the last 15 – 30µm of silicon removal. The typical methods of wafer thinning include mechanical grinding, chemical etching, or an atmospheric downstream plasma (ADP) etch. Figure 4 shows the equipment used for the final thinning steps.

Figure 5. High Volume Manufacturing Wafer Thinning System.

In the past, engineers used full thickness dice in packages. Today, semiconductor wafers are routinely thinned prior to dicing to aid in the sawing operation and to allow final package thickness to be reduced. Figure 5 shows an example of such a system. For high-power devices, wafer thinning improves ability to dissipate heat by lowering thermal resistance of die. However, as final thickness is decreased, the wafer progressively bends and weakens, causing problems for subsequent assembly processes. Therefore, it is important to reduce damage caused by back-grinding.

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Ask the Experts

Q: Why does STI (Shallow Trench Isolation) saturation stress reduce with increasing temperature?

A: This is caused by the fact that the viscosity of the dielectric reduces with increasing temperature and because the stress level (above which the dielectric viscosity decreases abruptly) is lower at higher temperatures.

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Spotlight: Wafer Fab Processing

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. The industry as a whole has gotten to this point of incredible complexity through the process of countless breakthroughs and developments in wafer fab processing. Today's wafer fab contains some of the most complex and intricate procedures ever developed by mankind. ***Wafer Fab Processing*** is a 4-day course that offers an in-depth look into the semiconductor manufacturing process, and the individual processing technologies required to make them. We place special emphasis on the basics surrounding each technique, and we delve into the current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By focusing on the basics of each processing step and the issues surrounding them, participants will learn why certain techniques are preferred over others. Our instructors work hard to explain how semiconductor processing works without delving heavily into the complex physics and mathematical expressions that normally accompany this discipline.

Participants learn basic but powerful aspects about the semiconductor industry. This skill-building series is divided into three segments:

1. **Basic Processing Steps.** Each processing step addresses a specific need in IC creation. Participants learn the fundamentals of each processing step and why they are used in the industry today.
2. **The Evolution of Each Processing Step.** It is important to understand how wafer fab processing came to the point where it is today. Participants learn how each technique has evolved for use in previous and current generation ICs.
3. **Current Issues in Wafer Fab Processing.** Participants learn how many processing steps are increasingly constrained by physics and materials science. They also learn about the impact of using new materials in the fabrication process and how those materials may create problems for the manufacturers in the future.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the semiconductor industry and its technical issues.
2. Participants will understand the basic concepts behind the fundamental wafer fab processing steps.
3. The seminar will identify the key issues related to each of the processing techniques and their impact on the continued scaling of the semiconductor industry.
4. The seminar offers a wide variety of sample problems that participants work to help them gain knowledge of the fundamentals of wafer fab processing.
5. Participants will be able to identify the basic features and principles associated with each major processing step. These include processes like chemical vapor deposition, ion implantation, lithography, and etching.

6. Participants will understand how processing, reliability, power consumption and device performance are interrelated.
7. Participants will be able to make decisions about how to construct and evaluate processing steps for CMOS, BiCMOS, and bipolar technologies.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, participants will learn practical information on semiconductor processing and the operation of this industry. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The accompanying textbook offers hundreds of pages of additional reference material participants can use back at their daily activities.

COURSE OUTLINE

Day 1

1. Module 1: Basics & Fundamentals; Semiconductor Devices and ICs
    a. Acronyms
    b. Common Terminology
    c. Brief History
    d. Semiconductor Materials
    e. Electrical Conductivity
    f. Semiconductor Devices
    g. Classification of ICs & IC Processes
    h. Integrated Circuit Types
2. Module 2: Crystallinity, Crystal Defects, Crystal Growth
    a. Crystallinity
    b. Crystal Defects
    c. Crystal Growth
    d. Controlling Crystal Defects
3. Module 3: Basic CMOS Process Flow
    a. Transistors and Isolation
    b. Contacts/Vias Formation
    c. Interconnects
    d. Parametric Testing
4. Module 4: Ion Implantation 1 (The Science)
    a. Doping Basics
    b. Ion Implantation Basics
    c. Dopant Profiles
    d. Crystal Damage & Annealing

5. Module 5: Ion Implantation 2 (Equipment, Process Issues)
    a. Equipment
    b. Process Challenges
    c. Process Monitoring & Characterization
    d. New Techniques

Day 2

6. Module 6: Thermal Processing
    a. Overview of Thermal Processing
    b. Process Applications of SiO2
    c. Thermal Oxidation
    d. Thermal Oxidation Reaction Kinetics
    e. Oxide Quality
    f. Atomistic Models of Thermal Diffusion
    g. Thermal Diffusion Kinetics
    h. Thermal Annealing
    i. Thermal Processing Hardware
    j. Process Control
7. Module 7: Contamination Monitoring and Control
    a. Contamination Forms & Effects
    b. Contamination Sources & Control
    c. Contamination Characterization & Measurement
8. Module 8: Wafer Cleaning
    a. Wafer Cleaning Strategies
    b. Chemical Cleaning
    c. Mechanical Cleaning
9. Module 9: Vacuum, Thin Film, & Plasma Basics
    a. Vacuum Basics
    b. Thin Film Basics
    c. Plasma Basics
10. Module 10: CVD 1 (Basics, LPCVD, Epitaxy)
    a. CVD Basics
    b. LPCVD Films
    c. LPCVD Equipment
    d. Epi Basics
    e. Epi Process Applications
    f. Epi Deposition Process
    g. Epi Deposition Equipment

Day 3

11. Module 11: PVD
    a. PVD (Physical Vapor Deposition) Basics
    b. Sputter Deposition Process
    c. Sputter Deposition Equipment
    d. Al-Based Films
    e. Step Coverage and Contact/Via Hole Filling
    f. Metal Film Evaluation
12. Module 12: Lithography 1 (Photoresist Processing)
    a. Basic Lithography Process
    b. Photoresist Materials
    c. Photoresist Process Flow
    d. Photoresist Processing Systems
13. Module 13: Lithography 2 (Image Formation)
    a. Basic Optics
    b. Imaging
    c. Equipment Overview
    d. Actinic Illumination
    e. Exposure Tools
14. Module 14: Lithgroaphy 3 (Registration, Photomasks, RETs)
    a. Registration
    b. Photomasks
    c. Resolution Enhancement Techniques
    d. The Evolution of Optical Lithography
15. Module 15: Etch 1 (Basics, Wet Etch, Dry Etch)
    a. Etch Basics
    b. Etch Terminology
    c. Wet Etch Overview
    d. Wet Etch Chemistries
    e. Types of Dry Etch Processes
    f. Physics & Chemistry of Plasma Etching

Day 4

16. Module 16: Etch 2 (Dry Etch Applications and Equipment)
    a. Dry Etch Applications
    b. SiO2
    c. Polysilicon
    d. Al & Al Alloys
    e. Photoresist Strip
    f. Silicon Nitride
    g. Dry Etch Equipment
    h. Batch Etchers
    i. Single Wafer Etchers
    j. Endpoint Detection
    k. Wafer Chucks
17. Module 17: CVD 2 (PECVD)
    a. CVD Basics
    b. PECVD Equipment
    c. CVD Films
    d. Step Coverage
18. Module 18: Chemical Mechanical Polishing
    a. Planarization Basics
    b. CMP Basics
    c. CMP Processes
    d. Process Challenges
    e. Equipment
    f. Process Control
19. Module 19: Copper Interconnect, Low-k Dielectrics
    a. Limitations of “Conventional” Interconnect
    b. Copper Interconnect
    c. Cu Electroplating
    d. Damascene Structures
    e. Low-k IMDs
    f. Cleaning Cu and low-k IMDs

20. Module 20: Leading Edge Technologies & Techniques
    a. Process Evolution
    b. Atomic Layer Deposition (ALD)
    c. High-k Gate and Capacitor Dielectrics
    d. Ni Silicide Contacts
    e. Metal Gates
    f. Silicon on Insulator (SOI) Technology
    g. Strained Silicon
    h. Hard Mask Trim Etch
    i. New Doping Techniques
    j. New Annealing Techniques
    k. Other New Techniques
    l. Summary of Industry Trends

References:

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Doering & Nishi, Semiconductor Manufacturing Technology, 2nd ed.
Wolf, Silicon Processing, Vol. 4
Wolf, Silicon Processing, Vol. 1, 2nd ed.

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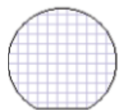

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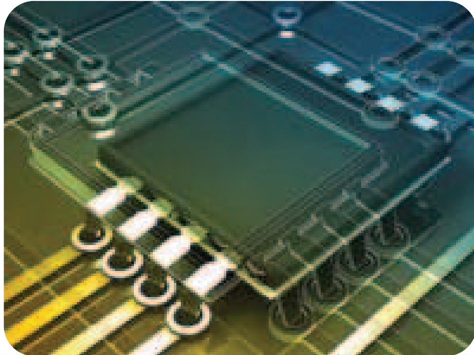

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