Issue 125 November 2019

InfoTracks

Semitracks Monthly Newsletter

Electronic Design Automation Tools Part 1

By Christopher Henderson

This article provides an overview of the Electronic Design Automation (EDA) design tools. The EDA industry is an interesting ecosystem and bears discussing, so that the design engineer can understand the environment.

Here is the outline. In Part I we will discuss the three major EDA tool suppliers: Cadence Design Systems, Synopsys, and Mentor Graphics, which is now owned by Siemens. In Part II we will briefly discuss interoperability issues between the three major platforms. We'll also discuss other suppliers developing tools in this area. Finally, we'll discuss the use case and the strengths and weaknesses of the tool suites.

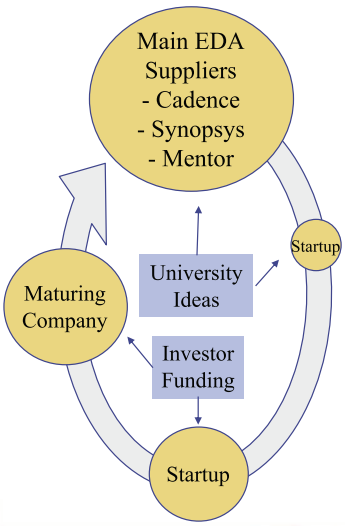


Figure 1. Illustration of EDA ecosystem.

In this Issue:

The EDA ecosystem is an interesting environment. There are three large suppliers within an industry that is no longer rapidly expanding. This creates an interesting dynamic. New ideas typically come from engineers working at one of the existing three large EDA suppliers. These engineers might leave and form a spinout or startup. These startups then gain some investor funding, and develop the idea into a working product. Sometimes the large EDA suppliers snap up companies early on, or in other instances, those startups can grow quite large before being bought (*e.g.,* Magma Design Automation grew quite large before being bought by Synopsys). This cycle then repeats itself. In fact, a number of engineers have left and joined startups, been acquired by a large EDA supplier, only to leave again at a later date with another new idea.

Figure 2. Cadence Design Systems.

Let's now briefly cover the three major EDA suppliers. The first one is Cadence Design Systems. They were founded in 1988 and employ around 6,800 employees, generating around $1.7B in revenue each year. They are currently the second largest of the three major EDA suppliers. They have strengths in full custom design, and some firms use Cadence as a "one-stop-shop" for their design tool needs.

We show a list of the main tools that Cadence provides here. They include:

- Virtuoso Platform—Tools for designing full-custom integrated circuits
- Encounter Platform—Tools for implementation of digital integrated circuits; this includes floorplanning, test, place and route and clock tree synthesis
- Incisive Platform—Tools for simulation and functional verification of RTL including Verilog, VHDL and SystemC based models; includes formal verification, formal equivalence checking, hardware acceleration, and emulation
- Palladium—Accelerators and emulators for hardware/software co-verification
- Design IP—Cadence provides design IP for memory, storage, high-performance interface protocols such as PCI Express Gen3, 40/100G Ethernet, and USB 2, 3
- Verification IP (VIP)—AMBA, PCI Express, USB, SATA, OCP, SAS, MIPI, others
- Integration Optimized IP (Design IP)—Vertically Integrated IP, inclusive of Digital Controller, Serdes Layer, and Device Driver; protocols supported include USB, DDR, PCI-Express, 10G-40G Ethernet, and On Chip Bus Fabric
- Allegro Platform—Tools for co-design of integrated circuits, packages, and PCBs
- OrCAD/PSpice—Tools for smaller design teams and individual PCB designers
- Sigrity technologies—Tools for signal and power verification for system-level signoff verification and interface compliance

Figure 3. Synopsys.

The next major EDA supplier to discuss is Synopsys. Synopsys was founded in 1986 by Aart de Geus, a well-known figure for many years in the EDA industry. Synopsys employs about 10,300 people and generates around $2.42B in revenue, as of this writing. They are currently the largest of the three major EDA suppliers. They have strengths in verification, synthesis and HDL. Synopsys is popular with fabless semiconductor firms and embedded systems companies.

We show a list of the main tools that Synopsys provides here. They include tools for:

- Software Integrity—Coverity, Defensics, Protecode, Sekker, Test Advisor, AbuseSA
- Semiconductor IP—Interface IP (USD, PCI DDR, Bluetooth, ethernet, etc.), Analog IP (data converters, audio codecs), Processors (ARC processors, embedded vision processors, software), IP Subsystems, SoC Infrastructure IP, Security IP Memories and Libraries
- Verification—Verification Continuum Platform, Simulation (VCS), AMS Verification (HSPICE), Static and Formal Verification (VC, SpyGlass), Debug and Coverage (Verdi), Verification IP, Emulation, Virtual Prototyping (Platform Architect), Physical Prototyping (HAPS Proto Compiler)
- Design—Galaxy Design Platform, RTL Synthesis (Design Compiler), Synthesis-based Test (DFTMax), Physical Implementation (ID Compiler), Custom Implementation (Custom Compiler), Signoff (PrimeTime), Physical Verification, FPGA Design, Power Electronic Systems, Optical Solutions
- Silicon Implementation—TCAD, Mask Synthesis (Proteus), Yield Management (Yield Manager)

Figure 4. Mentor Graphics (Siemens).

The third major EDA supplier is Mentor Graphics. Mentor was founded in 1981 by three engineers from Tektronix Corporation. Mentor Graphics employs around 5,200 employees and generates around $1.09B in revenue, as of this writing. They are currently the third largest EDA supplier and the smallest of

the big 3 EDA companies. They have strengths in test and yield. They are also quite popular with engineers, as this firm has had more of an engineering focus in its day-to-day operations over the years. Mentor Graphics was purchased by Siemens in 2016. Siemens has stated that they plan to allow Mentor to operate as a stand-alone operation, so we'll see if that direction holds into the future.

We show a list of the main tools that Mentor Graphics provides here. They include:

- Electronic design automation—full-custom layout (IC Station), place/route (Olympus-SoC), IC Verification tools (Calibre nmDRC, Calibre nmLVS, Calibre xRC, Calibre xACT 3D), IC Design for Manufacturing tools (Calibre LFD, Calibre YieldEnhancer and Calibre YieldAnalyzer), Schematic editors (Design Architect IC, DxDesigner), PCB Layout/design tools (PADS, Xpedition Enterprise and Board Station), IP cores for ASIC and FPGA designs
- Embedded systems—Mentor Embedded Linux, Real-time operating systems (Nucleus OS), VRTX, AUTOSAR, Confiig. Tooling (Volcano Vehicle Systems Builder), Dev. Tools (Sourcery CodeBench, Sourcery GNU toolchains), Inflexion UI, xtUML Design Tools (BridgePoint), VPN Solutions (Nucleus tool suite)
- FPGA synthesis tools—RTL & physical synthesis for FPGAs
- Electrical systems, cabling and harness design—Capital and VeSys
- Simulation tools for analog mixed-signal design—ModelSim, QuestaSim (Simulator with additional Debug capabilities targeted at complex FPGA's and SoC's), Questa Verification IP, Eldo and ADIT (SPICE simulators), SystemVision
- Fluid dynamics and heat transfer tools—FloTHERM (Computational Fluid Dynamics tool), FloEFD, T3Ster (JEDEC JESD51-1 standard modeling), TeraLED, Flowmaster (fluid mechanics in complex pipe flow systems), CADRA Design Drafting (mechanical drafting and documentation package)

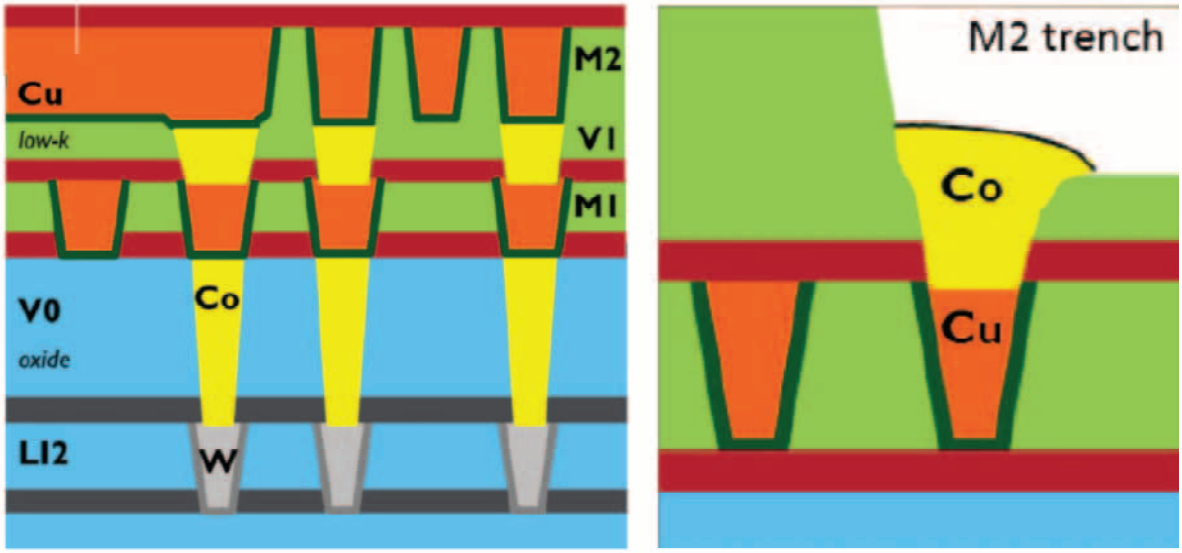
(to be concluded in next month's newsletter)

Technical Tidbit

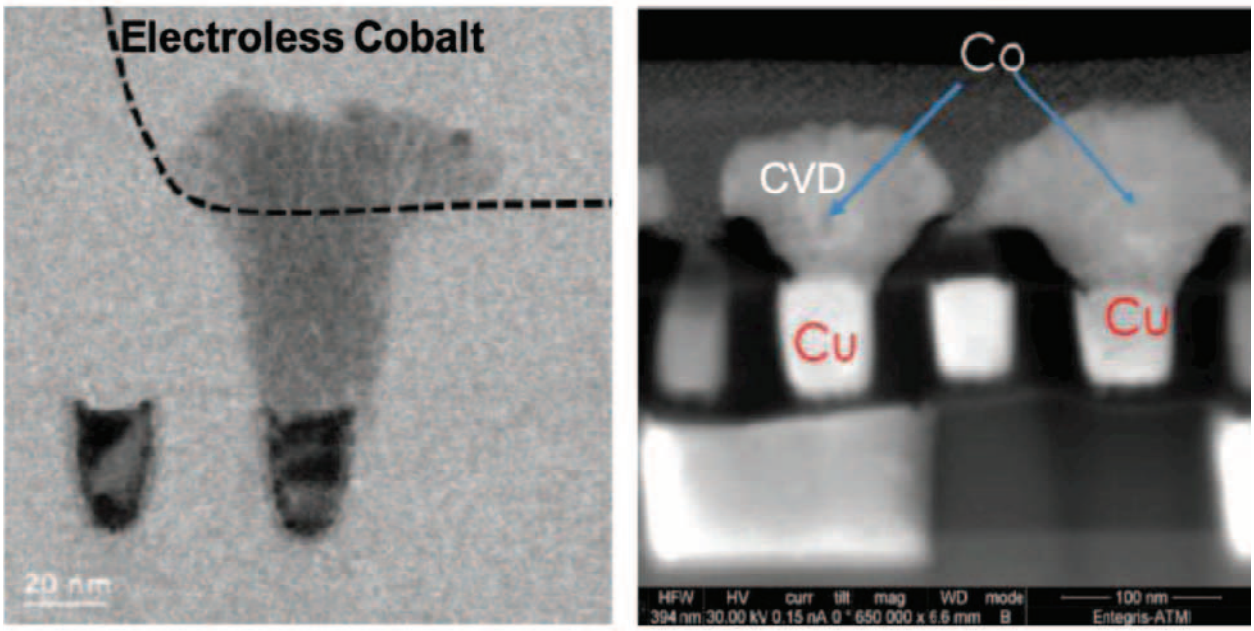
Cobalt Interconnect

In this month's technical tidbit, we will discuss the use of cobalt for interconnects.

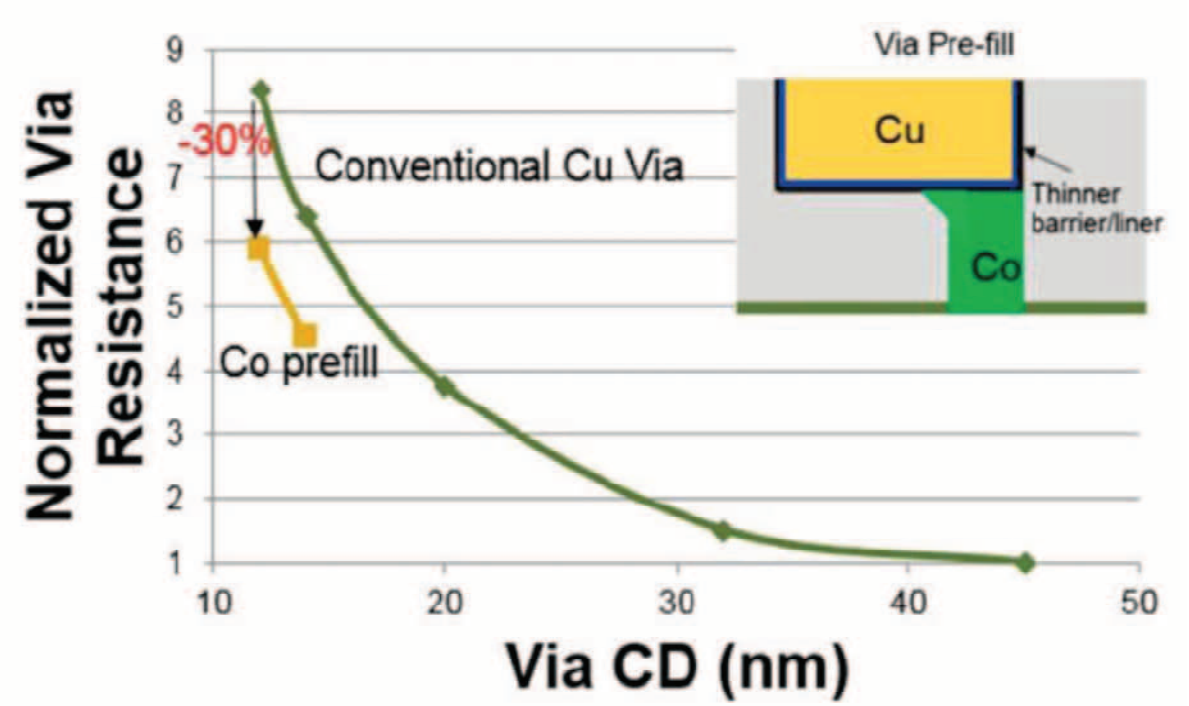
In terms of process integration for copper interconnect, one new material that is beginning to be used for vias is cobalt. As we scale down the contacts, we run into increased problems with resistance due to scaling, liner limitations, and scattering. One possibility to address this problem is to use a different material. In recent years, scientists have been investigating the use of cobalt at this layer. In fact, tools are now available to deposit cobalt , and Intel has demonstrated cobalt-filled contacts in their 10nm FinFET technology. Cobalt can be deposited using Physical Vapor Deposition or Chemical Vapor Deposition.



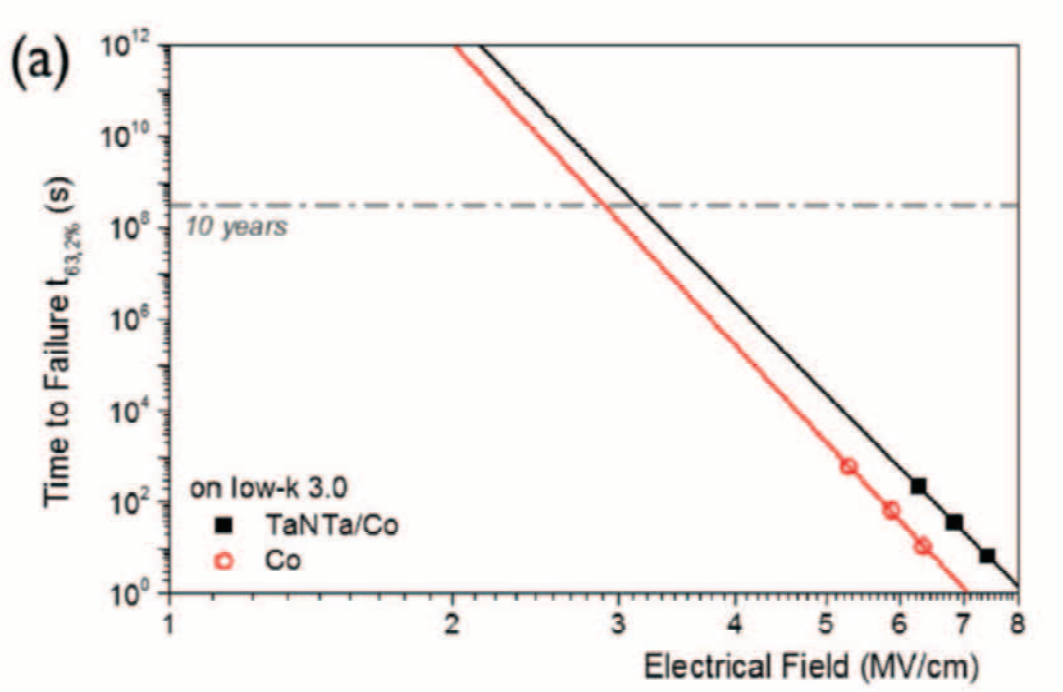
These images show examples of chemical vapor deposited cobalt vias in a semiconductor process. These are results from IMEC.



Cobalt exhibits lower via resistance than copper, and doesn't require a barrier layer, like copper does. Cobalt can also be deposited selectively. The graph here shows the improvement in via resistance.



Furthermore, cobalt deposited directly on low-k dielectrics shows adequate time dependent dielectric breakdown robustness, as the data in the graph at the lower left indicates. There isn't as much information on cobalt electromigration. However, we would expect cobalt to perform better due to its higher melting temperature.



Ask the Experts

Q: What was the smallest channel length before the industry switched to FinFETs?

A: Around 25nm. The 28nm technology node was the last major node to be a planar node. The effective channel length of a 28nm node transistor is approximately 25nm. Interestingly, the effective gate length has been around this value from around the 90nm technology node. Furthermore, it is not too much smaller, even with the advent of FinFETs.

Spotlight: Semiconductor Reliability and Qualification

OVERVIEW

Package reliability and qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.

5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.
6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms

4. Interfacial Fatigue
    1. Low-K fracture
5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

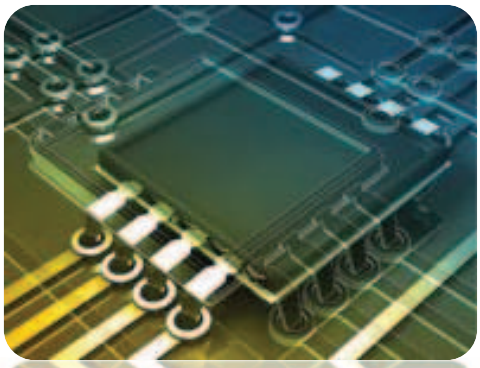
1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.



Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).

To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!

Upcoming Courses

(Click on each item for details)

Introduction to Processing
March 2 – 3, 2020 (Mon – Tue)
Portland, Oregon, USA

Failure and Yield Analysis
March 2 – 5, 2020 (Mon – Thur)
Portland, Oregon, USA

Advanced CMOS/FinFET Fabrication
March 4, 2020 (Wed)
Portland, Oregon, USA

IC Packaging Technology
March 5 – 6, 2020 (Thur – Fri)
Portland, Oregon, USA

Semiconductor Reliability / Product Qualification
March 9 – 12, 2020 (Mon – Thur)
Portland, Oregon, USA

Wafer Fab Processing
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Semiconductor Reliability / Product Qualification
April 14 – 17, 2020 (Tue – Fri)
Munich, Germany

Failure and Yield Analysis
April 20 – 23, 2020 (Mon – Thur)
Munich, Germany

IC Packaging Technology
April 27 – 28, 2020 (Mon – Tue)
Munich, Germany

Advanced CMOS/FinFET Fabrication
April 30, 2020 (Thur)
Munich, Germany