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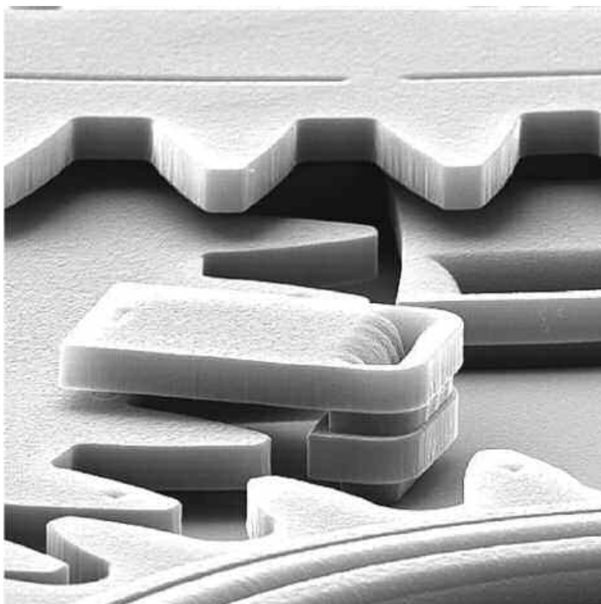
CVD Part I

By Christopher Henderson

Let's begin by discussing the chemistries used for silicon. Both epitaxial and polycrystalline silicon can be deposited using chemical vapor deposition. Silicon is deposited using silane or a chlorosilane gas. Both gases are highly reactive and must be treated carefully. Both gases produce excellent step coverage and good gap fill properties. These properties, while not as important in today's world of chemical mechanical planarization, are very worthwhile in the fabrication of surface micromachined structures, like the one shown here.



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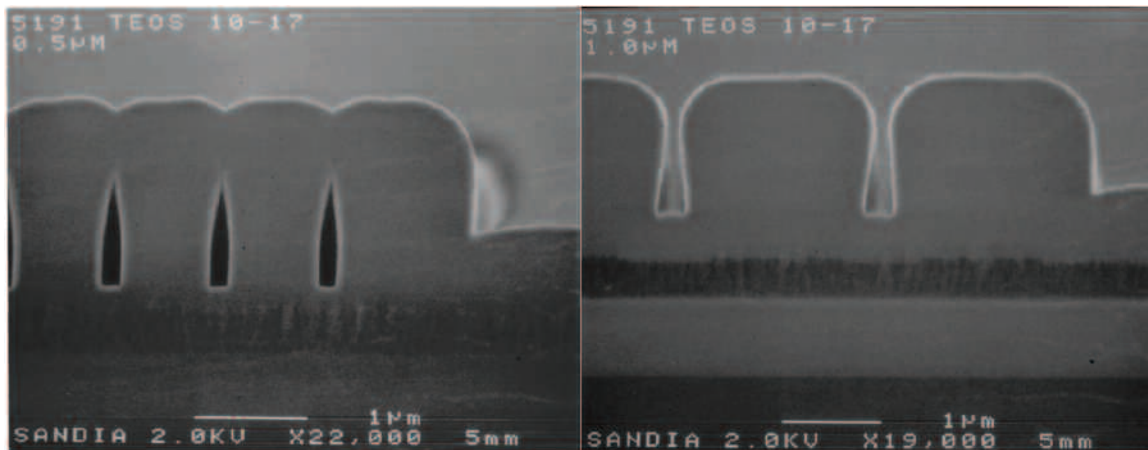
Polysilicon is formed by the thermal decomposition of silane. It is deposited by low pressure CVD. It is normally done at temperatures between 580 and 650ºC. Below 580ºC the polysilicon film is amorphous. Amorphous polysilicon tends to have higher resistance. Above 650ºC, the grains are large, but the film becomes rough and does not adhere well to the gate oxide regions.

There are two common chemistries for depositing CVD silicon oxide. One is silane-based while the other is TEOS-based. While silane plus oxygen will produce silicon dioxide, it is very reactive and causes gas-phase reactions. The temperatures associated with this reaction also result in poor step coverage and "bread-loafing". These effects can be reduced somewhat by using plasma enhanced CVD. TEOS (pronounced tee-os) or tetra-ethyl-ortho-silicate is very commonly used for depositing silicon dioxide. It has the advantages of a single source precursor, which means no gas phase reactions. A purely thermal TEOS CVD reaction around 700ºC will produce some bread-loafing, so plasma enhanced TEOS CVD is normally performed. There is some risk of carbon contamination when one uses TEOS.

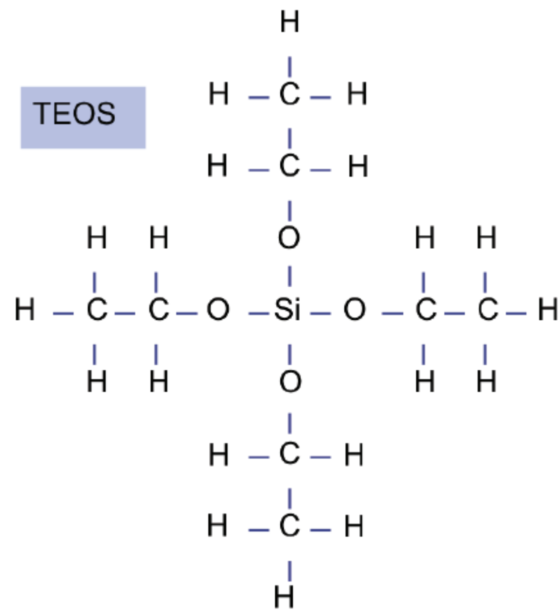


Process engineers use CVD when they cannot grow thermal silicon dioxide layers, which means they use this approach extensively. The process applications include interlevel and intermetal dielectrics, capping layers on materials like copper to prevent outdiffusion, ion implantation masks, and the final protective passivation layer on the chip. The properties between thermal silicon dioxide and CVD-deposited oxide differ substantially. We'll discuss those differences on the following slide. Also, the deposition conditions control the properties of the oxide. The comments on the following slide apply to both low pressure CVD and plasma-enhanced CVD, unless we state otherwise.

Parameter	Thermal	CVD
Stoichiometry	2.0	< 2.0
Density	Higher	Lower
Etch rate	Lower	Higher
Stress	Lower	Higher
Dielectric strength	Higher	Lower
Dielectric breakdown voltage	Higher	Lower

If we compare the qualities of thermally-growth silicon oxides to CVD-deposited oxides, we see there are several differences. Note that a thermally-grown oxide has a silicon to oxygen ratio of 2, whereas a CVD-deposited oxide is greater than 2. Thermal oxides have a higher density, lower etch rate, lower stress, higher dielectric strength and higher breakdown voltages. However, thermally-grown oxides can only be grown on silicon surfaces, and require extremely high temperatures, making them useful only in limited situations.

One can produce an oxide with properties more similar to a thermal silicon dioxide by raising the temperature during the deposition. Another technique is to perform a thermal densification after deposition. Process engineers do this at temperatures between 700 and 1000°C. As such, this process cannot be used after depositing aluminum metal. There are three common chemistries for this approach: silane, tetraethyl orthosilicate or TEOS, and TEOS plus ozone. This is the chemical structure for TEOS.



This table shows the three CVD deposition techniques for silicon oxide. In general silane provides a simple deposition method, but it is the most dangerous because silane gas is not only toxic, but highly explosive. It also suffers from problems with step coverage.

Parameter	Silane Chemistry	TEOS Chemistry	Ozone/TEOS Chem.
Process complexity	Simple	More complex	Even more complex
Main reactants	SiH_4 or SiH_2Cl_2 + N_2O	$Si(OC_2H_5)_4$	$Si(OC_2H_5)_4$, O_3
Step coverage	Poor for sub µm gaps	Very good	Excellent
Process safety	Concern	Good	Good
Dep. By LPCVD?	Not anymore	Yes	Yes
LPCVD dep. T	300-450°C	600-700°C	300-600°C
Dep. By PECVD?	Yes	Yes	Yes
PECVD dep. T	200-400°C	250-400°C	250-400°C
In-situ doping?	Yes	Yes	Yes

If we look at the chemistries in more detail, we see the reactions for silane, TEOS and ozone plus TEOS here. There are separate chemistries for TEOS depending on whether or not the reaction uses LPCVD or PECVD. The PECVD reaction requires the addition of oxygen to the reaction. LPCVD gives the best performance in terms of conformality, so it works well from trench fills like one needs for shallow trench isolation. In addition to silane and TEOS, there are a number of other possible precursor gases that one can use for PECVD-deposited oxides.

There are three common types of doped oxides: phosphosilicate glass, borosilicate glass, and borophosphosilicate glass. Most process engineers use the acronyms PSG, BSG, and BPSG. The typical doping range is 1 to 4% by weight. The advantages of doped silicon dioxide include: lower stress, better step coverage, lower reflow temperatures, and the ability to getter contaminants. Reflowed glass layers can round sharp corners, creating a smoother surface topography, while PSG getters highly-mobile alkali metals like sodium and potassium. Process engineers can dope the film in-situ by adding dopant gases. These include phosphine or trimethylphosphite for n-type doping, and diborane or trimethylborate for p-type doping.

An important application of PECVD is the deposition of silicon nitride. The specific applications include the formation of side wall spacers for transistors, the damascene etch stop layer, and the top passivation layer for the chip. We show the basic equation here. We react silane and ammonia to form a solid silicon hydrogen nitride on the chip. By using an RF plasma, we can lower the deposition temperature to between 200 and 400°C. Unfortunately, hydrogen content is a concern. At around 300°C, the hydrogen content can reach 20% or greater, which impacts film etching. Also, the hydrogen content in the sidewall spacer can lead to transistor threshold voltage shifts. Overall, this results in a lower quality film, but it is also a lower stress film.

Parameter	LPCVD	PECVD
Deposition temperature	700-800°C	200-400°C
Density	Higher	Lower
Composition	Stoichiometric	Non-stoichiometric
Step coverage	Excellent	Fair
Stress	High tensile	Low compressive
Hydrogen content	Low	High
Relative etch rate	Low	High

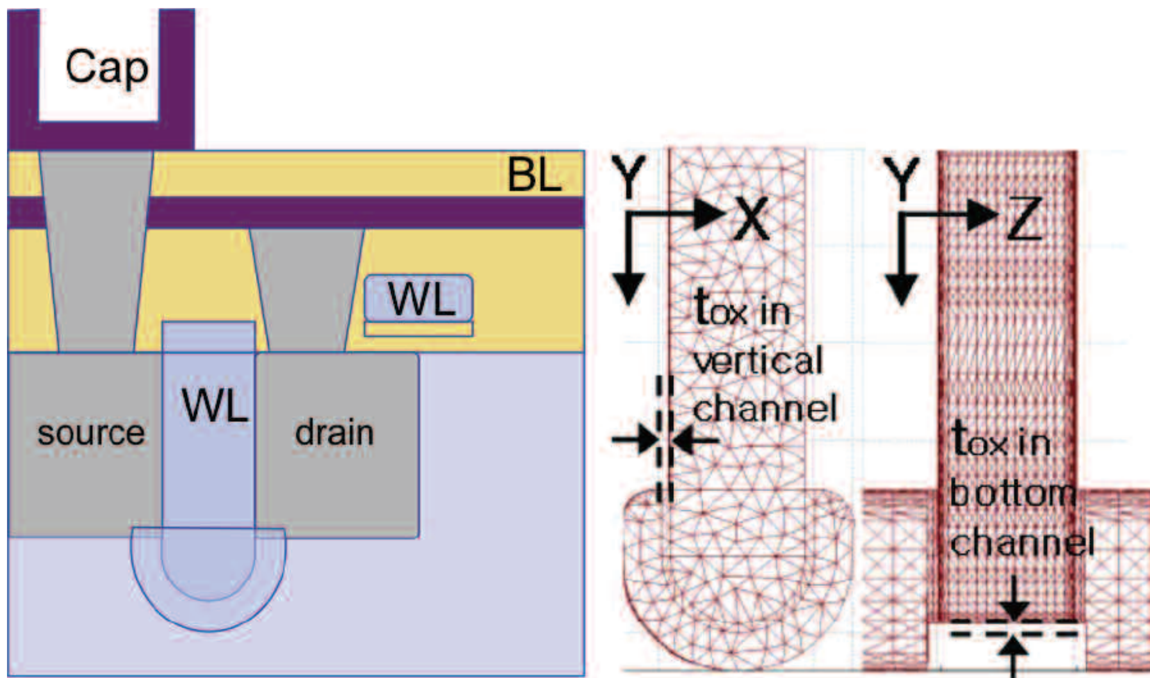
Another major material group deposited by PECVD is the oxynitride group. The process applications for silicon oxynitrides include: the liner films for shallow trench isolation, the interlevel and intermetal dielectrics, the final passivation layer, the gate and capacitor dielectrics, and dielectric antireflective coatings. We show the basic equation here. We react silane, ammonia, and nitrous oxide to form a solid silicon oxynitride layer on the chip. We can control the composition of this film by controlling the nitrous oxide flow.

There are two main CVD chemistries for silicon nitride deposition: silane-ammonia and chlorosilane-ammonia. Silane plus ammonia is very reactive in a thermal CVD reaction. Essentially, the reaction rains silicon nitride particles on the wafer surface. The silane-ammonia chemistry has been used in plasma enhanced CVD reactions with moderate success. The chlorosilane-ammonia chemistry is a better choice for CVD silicon nitride. It is less reactive, and produces excellent step coverage in a thermal CVD reaction. The chlorosilane-ammonia chemistry produces a silicon-rich silicon nitride. This has the advantage of producing a lower stress nitride layer, which can help reduce problems with dislocations in the silicon. CVD silicon nitride is commonly used for masking the silicon for ion implantation, and creating the nitride spacer on the side of the polysilicon gate.

Technical Tidbit

Saddle FinFET

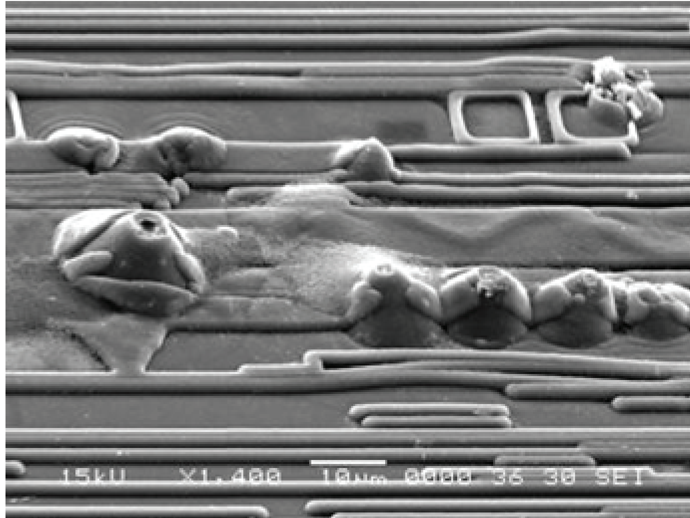
Although DRAM architectures have not evolved significantly over the last 15 years, there have been some incremental developments in the front end of line processing to improve the transistors. One such improvement is the saddle FinFET structure.



The Saddle FinFET or S-Fin is a variant of the buried wordline architecture. In addition to improved short channel effects, it also exhibits improved drive current and subthreshold slope, since the saddle structure provides a tri-gate type of effect that helps to control the channel better. This structure does have problems with gate-drain leakage and threshold voltage, and is therefore less effective at reducing the off-state leakage. Engineers at Samsung have been able to mitigate these effects somewhat by using a recessed fin structure or RFinFET. This structure just employs the saddle structure in the bottom of the recessed structure, which lowers the gate capacitance and the off-current. This in turn, helps to improve retention time.

Ask the Experts

Q: What do you think might be causing this problem seen here?



Energy Dispersive X-Ray Analysis shows that there are high levels of carbon in and near the anomalies.

A: Our best guess is that there was some type of contaminant in the PECVD chamber that fell onto the wafer during the dielectric deposition process right before top metal was deposited. This contaminant is a hydrocarbon material of some type (possibly a polymer from the CVD machine somewhere). During subsequent processing, it vaporized and created the "bubbling volcano" look that you see in the SEM images.

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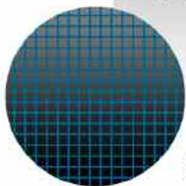

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Spotlight: Failure and Yield Analysis

OVERVIEW

Failure and Yield Analysis is an increasingly difficult and complex process. Today, engineers are required to locate defects on complex integrated circuits. In many ways, this is akin to locating a needle in a haystack, where the needles get smaller and the haystack gets bigger every year. Engineers are required to understand a variety of disciplines in order to effectively perform failure analysis. This requires knowledge of subjects like: design, testing, technology, processing, materials science, chemistry, and even optics! Failed devices and low yields can lead to customer returns and idle manufacturing lines that can cost a company millions of dollars a day. Your industry needs competent analysts to help solve these problems. ***Advanced Failure and Yield Analysis*** is a four-day course that offers detailed instruction on a variety of effective tools, as well as the overall process flow for locating and characterizing the defect responsible for the failure. This course is designed for every manager, engineer, and technician working in the semiconductor field, using semiconductor components or supplying tools to the industry.

By focusing on a ***Do It Right the First Time*** approach to the analysis, participants will learn the appropriate methodology to successfully locate defects, characterize them, and determine the root cause of failure.

Participants learn to develop the skills to determine what tools and techniques should be applied, and when they should be applied. This skill-building series is divided into three segments:

1. **The Process of Failure and Yield Analysis.**Participants learn to recognize correct philosophical principles that lead to a successful analysis. This includes concepts like destructive vs. non-destructive techniques, fast techniques vs. brute force techniques, and correct verification.
2. **The Tools and Techniques.** Participants learn the strengths and weaknesses of a variety of tools used for analysis, including electrical testing techniques, package analysis tools, light emission, electron beam tools, optical beam tools, decapping and sample preparation, and surface science tools.
3. **Case Histories.** Participants identify how to use their knowledge through the case histories. They learn to identify key pieces of information that allow them to determine the possible cause of failure and how to proceed.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the tools, techniques and processes used in failure and yield analysis.
2. Participants will be able to determine how to proceed with a submitted request for analysis, ensuring that the analysis is done with the greatest probability of success.
3. The seminar will identify the advantages and disadvantages of a wide variety of tools and techniques that are used for failure and yield analysis.
4. The seminar offers a wide variety of video demonstrations of analysis techniques, so the analyst can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify basic technology features on semiconductor devices.
6. Participants will be able to identify a variety of different failure mechanisms and how they manifest themselves.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

THE SEMITRACKS ANALYSIS INSTRUCTIONAL VIDEOS™

One unique feature of this workshop is the video segments used to help train the students. Failure and Yield Analysis is a visual discipline. The ability to identify nuances and subtleties in images is critical to locating and understanding the defect. Many tools output video images that must be interpreted by analysts. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.

COURSE OUTLINE

1. Introduction
2. Failure Analysis Principles/Procedures
    a. Philosophy of Failure Analysis
    b. Flowcharts
3. Gathering Information
4. Package Level Testing
    a. Optical Microscopy
    b. Acoustic Microscopy
    c. X-Ray Radiography
    d. Hermetic Seal Testing
    e. Residual Gas Analysis
5. Electrical Testing
    a. Basics of Circuit Operation
    b. Curve Tracer/Parameter Analyzer Operation
    c. Quiescent Power Supply Current
    d. Parametric Tests (Input Leakage, Output voltage levels, Output current levels, etc.)
    e. Timing Tests (Propagation Delay, Rise/Fall Times, etc.)
    f. Automatic Test Equipment
    g. Basics of Digital Circuit Troubleshooting
    h. Basics of Analog Circuit Troubleshooting
6. Decapsulation/Backside Sample Preparation
    a. Mechanical Delidding Techniques
    b. Chemical Delidding Techniques
    c. Backside Sample Preparation Techniques
7. Die Inspection
    a. Optical Microscopy
    b. Scanning Electron Microscopy

8. Photon Emission Microscopy
    a. Mechanisms for Photon Emission
    b. Instrumentation
    c. Frontside
    d. Backside
    e. Interpretation
9. Electron Beam Tools
    a. Voltage Contrast
        i. Passive Voltage Contrast
        ii. Static Voltage Contrast
        iii. Capacitive Coupled Voltage Contrast
        iv. Introduction to Electron Beam Probing
    b. Electron Beam Induced Current
    c. Resistive Contrast Imaging
    d. Charge-Induced Voltage Alteration
10. Optical Beam Tools
    a. Optical Beam Induced Current
    b. Light-Induced Voltage Alteration
    c. Thermally-Induced Voltage Alteration
    d. Seebeck Effect Imaging
    e. Electro-optical Probing
11. Thermal Detection Techniques
    a. Infrared Thermal Imaging
    b. Liquid Crystal Hot Spot Detection
    c. Fluorescent Microthermal Imaging
12. Chemical Unlayering
    a. Wet Chemical Etching
    b. Reactive Ion Etching
    c. Parallel Polishing
13. Analytical Techniques
    a. TEM
    b. SIMS
    c. Auger
    d. ESCA/XPS
14. Focused Ion Beam Technology
    a. Physics of Operation
    b. Instrumentation
    c. Examples
    d. Gas-Assisted Etching
    e. Insulator Deposition
    f. Electrical Circuit Effects
15. Case Histories

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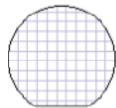

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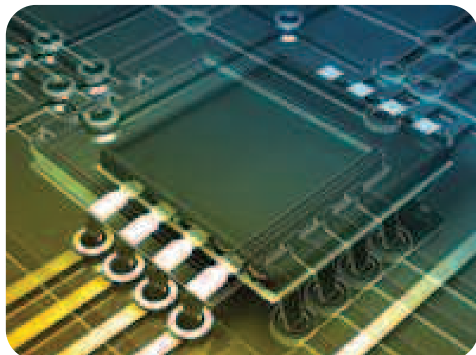

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).

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Failure and Yield Analysis
January 18 – 21, 2016 (Mon – Thur)
San Jose, California, USA

Failure and Yield Analysis
May 17 – 20, 2016 (Tue – Fri)
Munich, Germany

EOS, ESD and How to Differentiate
May 23 – 24, 2016 (Mon – Tue)
Munich, Germany

Semiconductor Reliability / Product Qualification
May 30 – June 2, 2016 (Mon – Thur)
Munich, Germany