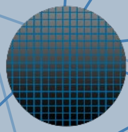

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INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

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Semiconductor Cleanroom Technology

By Christopher Henderson

In October's Feature Article, we continued our series on Cleanroom Technology by discussing Contamination Control. In this Feature Article, we will continue our discussion on Cleanroom Technology by discussing Cleanroom Construction. The construction of the cleanroom is a critical activity.

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UPCOMING COURSES:

EOS, ESD & How to Differentiate

Wafer Fab Processing

And more! See page 14 for more details

Not only does the cleanroom need to be constructed in such a way as to keep contamination out, it must also be able to minimize vibrations, prevent damage to the surrounding environment, and provide flexibility for various types of semiconductor processing tools.

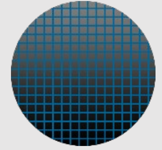
All the elements of a cleanroom project are typically developed by a team of project designers, engineers, construction managers, project managers, and some sort of management team. This can range from CEOs to directors of engineering or operations to mid-range facility managers. When the thought of building a cleanroom comes to fruition, some questions to prepare for are:

- What is this cleanroom going to be used for? (Product development, packaging, research & development etc.)
- What process systems are going into the space?
- Is there a rough estimate on dimensions?
- What are the ISO classification requirements?

Determining an ISO classification and process requirements are important, but selecting a site location is just as important. Some variables that need to be considered are:

- The load-bearing capacity of the ground
- The ground water and soil toxicity
- The ambient air quality and airborne pollutants around the site
- The availability of utilities and services at the site versus the required utilities and services to determine if additional services or remote connections from adjacent facilities are necessary
- Any environmental issues
- The site ambient vibration and noise levels, and a determination of their acceptability for the process technologies being considered at the site with or without special treatments
- Any ambient electromagnetic fields

Finally, one must consider local zoning ordinances and regulations. Figure 1 shows a typical zoning map associated with a cleanroom site construction plan.



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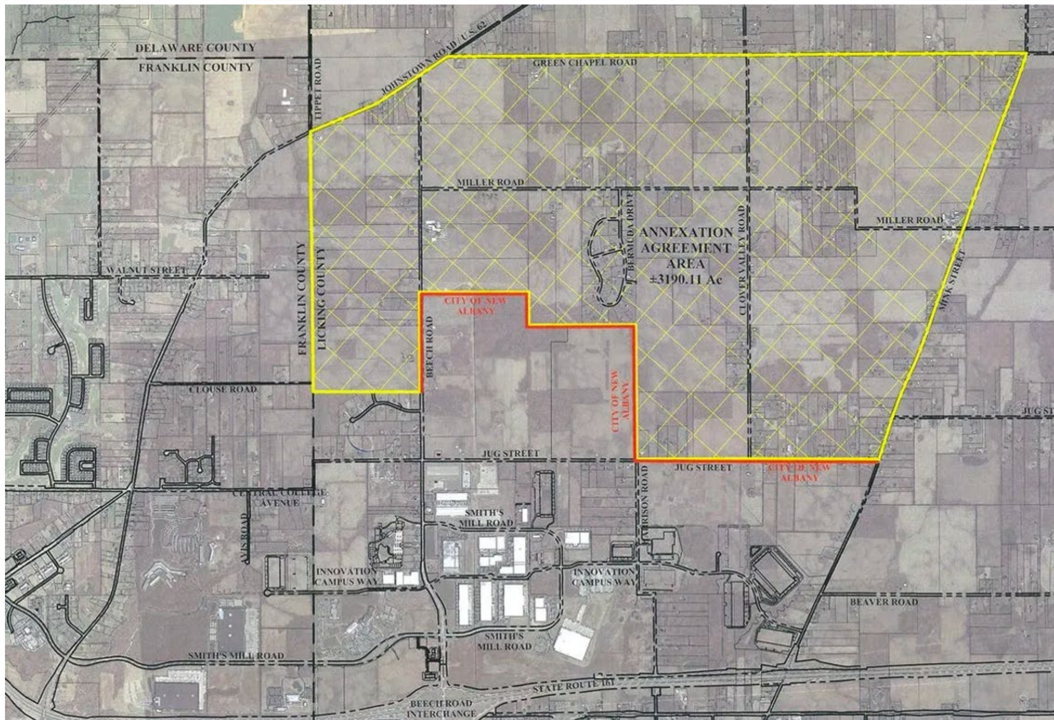


Figure 1- Example of a zoning map associated with a cleanroom site construction plan

Everything from operations, maintenances, and quality personnel to flow of air in the cleanroom need to be consulted throughout the entire design process. An efficient cleanroom operation is a systemic design effort that determines functional interdependences and efficient flow to minimize the migration of contaminants and to optimize process flow; this means design flow arrangements in and out of the cleanroom. If your cleanroom has equipment and materials entering it, these items must be precleaned and moved through either an airlock or a pass through.

Let’s discuss ancillary buildings on the fab site. The primary building or buildings of interest are the ones associated with central utilities. Quite often, ultrapure water and bulk gasses, like oxygen, hydrogen and argon, are generated on site in a central utilities building or plant. Figure 2 shows an example of a central utilities building attached to a wafer fabrication facility.

Figure 2- Example of a central utilities building attached to a wafer fabrication facility

A typical approach to placing the fab and the central utilities plant on a site would be based on how the last fab developed by the manufacturer was configured and would consider outside constraints such as property lines, where utilities are entering the site and surrounding traffic patterns. Another common tactic is to put all the facilities equipment that are not in the fab building into one large central utilities plant.

An alternative approach is to design things from the "inside-out." In this approach, one would start by defining where the fab processing functional areas will be located within the cleanroom. One would then note which of these functional areas are the largest consumers of a given facility system. For example, the deposition and dry etch areas use by far the most specialty gases, but use relatively low levels of ultrapure water; whereas, the wet clean/etch area uses the vast majority of ultrapure water and wet chemicals, and also a significant amount of the exhaust totals. To improve on this, one can pair this information with data-driven design tools to digitally model different possible facility system placements within the building and on the site to quickly identify the top few options which have the lowest cost of conveying the utility system between the source and the major use point in the fab. These options, by definition, would also have the simplest utility space plan and would require the

lowest amount of field labor to erect. While the cost of conveyance should not be the ONLY consideration for site placement with this alternate approach, it should be a key consideration. This approach provides valuable data to help better understand that cost. Another interesting issue is that the location where a given utility service would ideally enter and/or leave the fab building can be different from the other services. For example, construction costs might be reduced if the chilled and hot water supply and return lines entered the fab building on its short end, but the ultrapure water and drains entered/left the wafer fab in the middle of one of its long sides. This logically leads to proposing that the boiler/chiller central utilities building be different than the ultrapure water makeup building which is also different from the wastewater treatment building. Each building can then be tailored (column spacing, ceiling heights, etc.) to the facility equipment's needs.

Next, let's briefly discuss the topics of site preparation, building structure, and materials used in construction.

We need to control vibration, so fabs need to be placed away from significant road traffic, and the concrete flooring material must be able to handle the load of the building and equipment without transferring vibration into the facility. We need to address settling of the soil. We also need to address moisture and drainage. The soil materials must have the ability to handle the load of the building and the equipment. As such, there will likely need to be significant effort in preparing the site, including removal of existing soil, the deposition of a proper base course material, and shaping the land for proper drainage. Figure 3 shows a photograph of the Texas Instruments fab complex in Sherman, Texas, during the site preparation process.

Figure 3- Texas Instruments Sherman fab complex during site preparation process.

The structure must be able to handle the HVAC and other cleaning units in the region above the cleanroom. Because this is necessary, the construction of the support beams and joists will be significantly more robust than a typical warehouse. Figure 4 shows a photograph of the inside of a cleanroom area during the construction phase.

Figure 4- Photograph of the inside of a cleanroom area during the construction phase

The materials used in the construction of the cleanroom, especially those that are exposed on the inside of the cleanroom, need to be made of materials that will not generate particles. As such, construction materials typically include tile, ceramics, glass, metals and plastics. Figure 5 shows a photograph of a cleanroom after completion.

Figure 5- Photograph of a cleanroom after completion

Fab construction usually takes about 12 to 18 months, depending on the complexity of the site. Figure 6 shows a photo of the TSMC fab in north Phoenix during its construction phase.

Figure 6- Photo of the TSMC fab in north Phoenix during its construction phase

This concludes the first part of our discussion on cleanroom construction. In next month's Feature Article, we will cover the second part of our discussion of cleanroom construction.

Technical Tidbit: Sputtering Yield

This month's Technical Tidbit covers Sputtering Yield. We define the sputter yield as the number of atoms ejected divided by the number of incident atoms.

Figure 1- effect of the mass and energy on sputtering yield

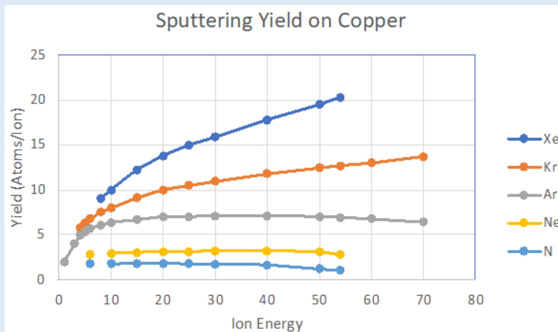


Figure 2- sputtering yield as a function of the ion angle of incidence

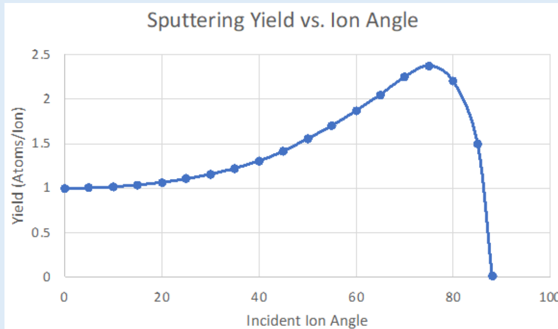
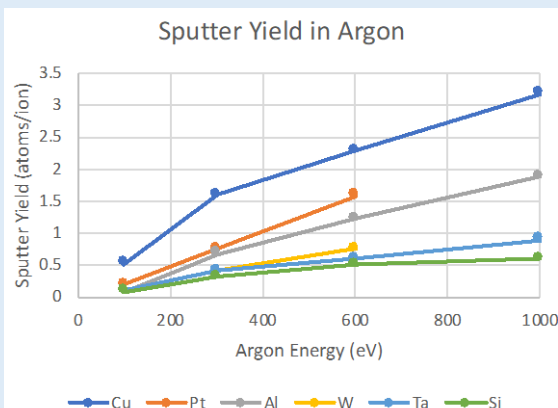


Figure 3- sputtering yield as a function of the target material and energy



This is a key factor in determining the deposition rate. It is a function of several variables: the ion angle of incidence, the atomic mass of the incident ion, the energy of the incident ion, and the target material. In general, the yield is higher for oblique angles, as there is less chance of ion implantation; higher for higher mass atoms, as they are able to dislodge target material atoms more easily through momentum transfer; and higher for higher energy ions for the same reason.

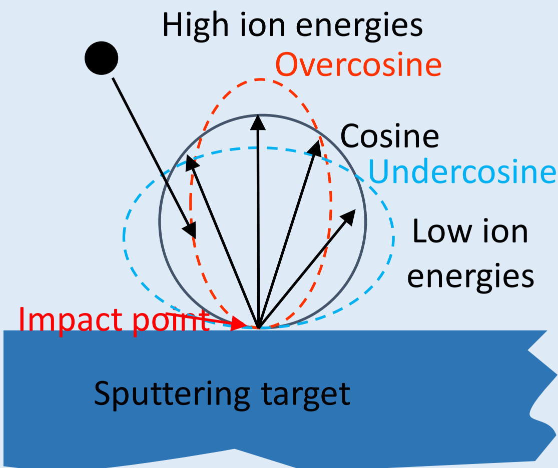
Sputtering yield is typically in the range of 1 to 3 atoms per incoming ion, and will determine the deposition rate. The yield depends on the target material, the mass and energy of the bombarding ions, the angle of incidence, and the pressure inside the chamber, which determines the mean free path of the ions. Below, we show several graphs to gain some perspective on the variables involved. First, the graph in Figure 1 shows the effect of the mass and energy of the bombarding ions. Notice that heavier elements provide better sputtering yield. Also, notice that, in general, higher ion energies provide better sputtering yield. However, this is not true for lighter elements, such as nitrogen and neon. The overwhelming choice for sputtering in a physical vapor deposition system is argon. It is inert, since it is a noble gas, and will not react with the target material. Furthermore, it is more readily available than the heavier noble gases, like krypton and xenon. Argon provides a decent sputter yield, and is easy to pump with vacuum pumping systems.

The graph in Figure 2 shows the sputtering yield as a function of the ion angle of incidence. Low angles mean that the ions arrive closer to perpendicular to the target surface, and are therefore less likely to cause the target material to scatter. As the angle increases, the incident ions become more likely to scatter target atoms away from the target.

Figure 4- emission flux equation

$$j_{\Omega}(\theta) = Y\phi\left(\frac{cos\theta}{\pi}\right)$$

Figure 5- diagram depicting the cosine law of sputtering



However, if the angle is too large, then the incident ions will simply scatter off of the target material, causing the sputtering yield to fall toward zero.

The sputter yield is also a function of the target material. We show data for several commonly-deposited metals in Figure 3. The graph shows sputter yield as a function of argon energy. Notice that the sputter yield increases with argon energy.

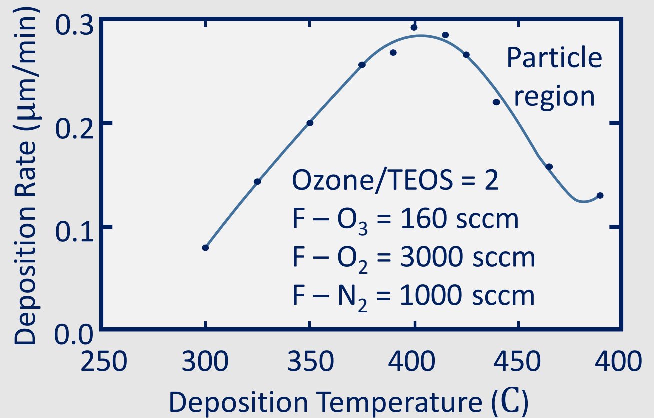
In general, the yield will go up as the bonding energy between the atoms in the target material go down. This means that materials with weaker bonding configurations, like gold, sputter more easily than materials with strong bonding configurations, like tungsten or titanium. A typical semiconductor sputtering system will operate at approximately 500 electron-volts.

Let's look more closely at the angle of incidence associated with the sputtering yield. The sputtering yield follows a cosine law. The sputtering yield, also known as emission flux, follows the equation shown in figure 4.

Emission flux is a function of the sputter yield (Y), the incident flux (ϕ), and the cosine of the emission angle (θ). For near normal incidence of sputtering gas ions onto the target surface, the angular distribution of the sputtered species emitted from a target surface can be approximated by a cosine distribution. One factor that does affect the cosine law is the energy of the incoming ions. If they are high, the function is classified as an "Overcosine" function, and if they are low, then the function is classified as an "Undercosine" function. We show that in Figure 5.

Ask The Experts

Q: When depositing Thermal TEOS-O_3, why does the deposition rate decrease with temperature?



A: The primary reason for the decrease in deposition rate with increasing temperature is because there is an increase in parasitic gas-phase reactions. In other words, the gas molecules are more energetic, and colliding and reacting with each other in the plasma, rather than arriving at the surface of the wafer to react on the surface. This leads to the depletion of deposition precursors. It also leads to the formation of silicon dioxide “dust”, which then rains down onto the surface of the wafer, rather than incorporating into the thin film. The graph in Figure 1 shows this decrease that occurs above 400°C, where particles begin to form.

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Course Spotlight:
Semiconductor Reliability & Product Qualification

This is one of our public courses we are planning to hold in 2023. Stay tuned on our website for course announcements!

COURSE OBJECTIVES

With focused guidance from your instructor, you will gain insight into the following:

1. failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components
2. how to gather, plot and make inferences from relevant data
3. major failure mechanisms, how they're observed, modeled, and eliminated
4. video demonstrations of analysis techniques covering the expected results seen with equipment
5. identifying the steps that make up a basic qualification process for semiconductor devices
6. how to implement appropriate screens that will assure component reliability
7. identifying appropriate tools to purchase when starting or expanding a laboratory

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, classroom exercises, and question/answer sessions, you will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of current, relevant experience in this field. The course notes offer dozens of pages of additional reference material you can use day to day.

OVERVIEW

Package reliability and qualification evolves with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability involves tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins and adapting to many new package types. This requires information on statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

You'll develop the skills to determine what failure mechanisms might occur, how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics:** learn the fundamentals of statistics, sample sizes, distributions and their parameters.

2. **Failure Mechanisms:** learn the nature and manifestation of many types of failure mechanisms at both the die and package level. Including time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.

3. **Qualification Principles:** learn how test structures are designed to test for a particular failure mechanism.

4. **Test Strategies:** learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OUTLINE

Day 1

1. Introduction to Reliability
    a. Basic Concepts
    b. Definitions
    c. Historical Information
2. Statistics and Distributions
    a. Basic Statistics
    b. Distributions (normal, lognormal, exponent, Weibull)
    c. Which distribution should I use?
    d. Acceleration
    e. Number of failures

Day 2

3. Overview of Die-Level Failure Mechanisms
    a. Time Dependant Dielectric Breakdown
    b. Hot Carrier Damage
    c. Bias Temperature Instability
    d. Electromigration
    e. Stress Induced Voiding
    f. BEOL Dielectric Reliability
4. Package Level Mechanisms
    a. Moisture/Corrosion
        i. Failure Mechanisms
        ii. Models for Humidity
        iii. T_{ja} Considerations
        iv. Static and Periodic stresses
        v. Exercises
    b. Thermo-Mechanical Stress
        i. Models
        ii. Failure Mechanisms
    c. Chip-Package Interactions
        i. Low-K fracture
    d. Through Silicon Via Reliability
    e. Thermal Degradation/Oxidation

Day 3

5. Board Level
    a. Package Attach (Solder) Reliability
        i. Creep/Sheer/Strain
        ii. Lead-Free Issues
        iii. Electromigration/Thermo migration
        iv. MSL Testing
    b. Board Level Reliability Mechanisms
        i. Interposer
        ii. Substrate
6. Use Condition Failure Mechanisms
    a. Electrical Overstress/ESD
    b. Radiation Effects
7. Test Structures and Test Equipment
8. Developing Screens, Stress Tests and Life Tests
    a. Burn-In
    b. Life Testing
    c. HAST
    d. JEDEC-based Tests
    e. Exercises

Day Four

9. Calculating Chip and System Level Reliability
10. Developing a Qualification Program
    a. Process
    b. Standards-Based Qualification
    c. Knowledge-Based Qualification
    d. MIL-STD Qualification
    e. JEDEC Documents (JESD47H, JESD94, JEP148)
    f. AEC-Q100 Qualification
11. JEDEC Tests
12. Exercises and Discussion

Upcoming Courses

EOS, ESD and How to Differentiate
March 6-7, 2023 (Mon.-Tues.) | Munich, Germany

Semiconductor Reliability and Product Qualification
March 13-16, 2023 (Mon.-Thurs.) | Munich, Germany

Wafer Fab Processing
March 13-16, 2023 (Mon.-Thurs.) | Munich, Germany

Failure and Yield Analysis
March 20-23, 2023 (Mon.-Thurs.) | Munich, Germany

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