ISSUE #166
May 2023

SEMITRACKS, INC.

INFOTRACKS

YOUR MONTHLY LOOK INSIDE SEMICONDUCTOR TECHNOLOGY

Semiconductor Cleanroom Technology

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In last month's Feature Article, we continued our series on Semiconductor Cleanroom Technology by discussing Power Usage as it pertains to the Heating, Ventilation and Air Conditioning (HVAC). In this month's Feature Article, we continue our discussion of Cleanroom Technology, by covering HVAC, as it applies to the technology of Cleanrooms. Semiconductor cleanrooms require tightly controlled temperature and humidity levels, so the air conditioning requirements are quite stringent.

The Heating, Ventilation and Air Conditioning system plays a large role in creating the contamination-free properties of the cleanroom environment as compared to the outside ambient environment. The HVAC system requirements include:

- Supplying airflow in sufficient volume and cleanliness to support the cleanliness rating of the room.
- Introducing air in a manner to prevent stagnant areas where particles could accumulate.
- Filtering the outside and re-circulated air across high efficiency particulate air (HEPA) filters.
- Conditioning the air to meet the cleanroom temperature and humidity requirements.
- Ensuring enough conditioned make-up air, or the replacement of air lost to the outside environment, to maintain the specified positive pressurization.

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Cleanroom design encompasses much more than conventional temperature and humidity control. A typical office building environment contains from 500,000 to 1,000,000 particles, at 0.5 microns or larger, per cubic foot of air, whereas a Class 100 cleanroom is designed to never allow more than 100 particles, at 0.5 microns or larger, per cubic foot of air. Class 1000 and Class 10,000 cleanrooms are designed to limit particles to 1000 and 10,000 respectively. A cleanroom differs from a normal comfort air-conditioned space in the following three ways. First, there is increased air supply. Whereas typical home or office building air conditioning requires about 2-10 air changes per hour, a cleanroom would typically require 20 to 60 air changes per hour, and could be as high as 600 changes for absolute cleanliness. The large air supply is mainly provided to eliminate the settling of the particulate, and to dilute the contamination produced in the room to an acceptable concentration level. Second, there is use of high efficiency filters. The use of high efficiency particulate air, or HEPA, filters is another distinguishing feature of cleanrooms. The HEPA filters for stringent cleanrooms are normally located at the terminal end, and in most cases, provide 100% ceiling coverage. Third is room pressurization. A cleanroom is positively pressurized to 0.05 inches of water in a water column (in-wc) with respect to the adjacent areas. This is done by supplying more air and extracting less air from the room.

Any air introduced in the controlled zone needs to be filtered. Air filtration involves the separation of particles from the air flow. The removal method is almost as diverse as the size ranges of the particulates generated. Understanding separation techniques requires an exact definition of what particles are. As particles become very small, they cease to behave as much like particles and more so like gas phase molecules. It is difficult to tell whether such small particles are actually suspended in air or instead are diffused throughout the air. The bottom boundary where particles act as true particles is about 0.01 micron. The normal theory of separation does not apply to particles below this size, and removing them from air requires techniques reserved for gaseous materials. Particles above 0.01 micron are usually considered to be filterable. All air entering a cleanroom must be treated by one or more filters. High-Efficiency Particulate Air (HEPA) and Ultra-Low Penetration Air (ULPA) filters are the most common filters used in cleanroom applications. Figure 1 shows several examples of these filters. We will have more to say about these filters in a later section of the course.

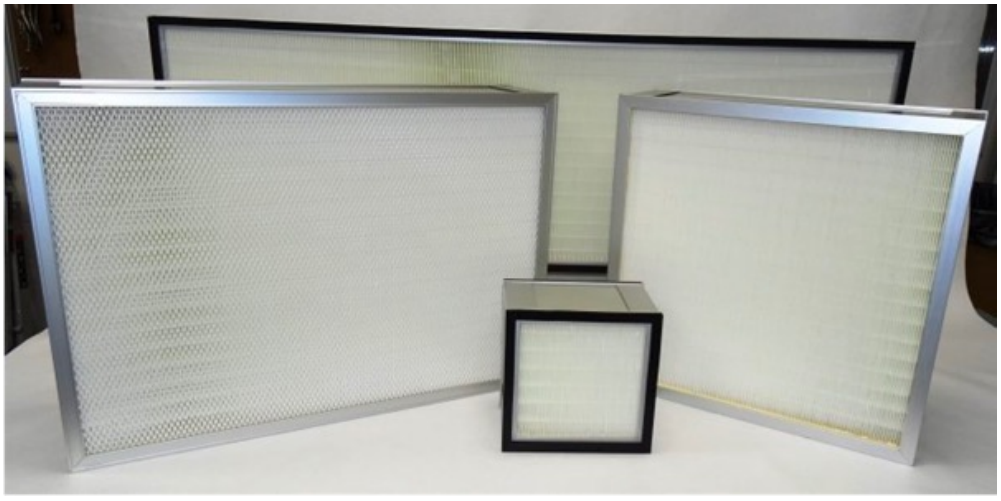

Figure 1- Examples of HEPA and ULPA filters (image courtesy APC Filtration)

HEPA & ULPA filters used in most stringent cleanrooms are generally built in the ceiling and can be installed in groups housed in a proprietary modular pressure plenum system. They can also be installed in single filter housings, individually ducted, suspended in an inverted "T" grid support system, and sealed to prevent unfiltered bypass air from entering the cleanroom. Filter design, installation, and coverage conventionally follows the guidelines shown in Table 1 for cleanroom class.

ISO Class	Fed 208	Controls	HEPA Coverage as % of Ceiling
1	-	Stringent	100
2	-	Stringent	100
3	1	Stringent	100
4	10	Stringent	100
5	100	Stringent	100
6	1,000	Intermediate	33-40
7	10,000	Intermediate	10-15
8	100,000	Less stringent	5-10

Table 1- Filter Guidelines for cleanroom coverage

Airflow is usually specified as either average air velocity within the room, or as air changes per hour, also known as Air Change Rate or ACR. These recommendations are not based on scientific findings and there is no clear consensus on an optimum ACR, or Air Velocity. Since there are no clearly defined rules, here are some rules of thumb for air flow. Table 2 shows airflow recommendations.

ISO Class	Fed 208	Controls	Air Velocity at Table Level in FPM	Air Changes per Hour
1	-	Stringent	70-130	> 750
2	-	Stringent	70-130	> 750
3	1	Stringent	70-130	> 750
4	10	Stringent	70-110	500-600
5	100	Stringent	70-90	150-400
6	1,000	Intermediate	25-40	60-100
7	10,000	Intermediate	10-15	25-40
8	100,000	Less stringent	3-5	10-15

Table 2- Airflow recommendations for air change rates and velocities

The velocity of the air is often determined by the degree of contamination control we wish to achieve. As a general rule, cleaner rooms require more air velocity than rooms that are less clean. Supply air volume is therefore highest in Class 1, or ISO 3, and decreases as the requirement for cleanliness decreases. For many years, engineers used a value of 90 feet per minute, or fpm, which is equivalent to 0.46 meters per second, with a variance of ±20%, to specify the airflow in the cleanest of cleanrooms. The primary objective is to maintain airflow in parallel flow streams that has two purposes: first, it needs to dilute particle concentrations that may have formed in the room due to personnel or process activity, and second, to carry away particles or contaminants generated within the room. Although higher air velocity is advantageous in particle removal/settlement, this may also result in over sizing of equipment that may be very energy inefficient. There is no term called optimal velocity, and there is no scientific or regulatory basis for this guideline. The 90-fpm velocity is purely derived from past practices over two decades and has become a common, widely accepted industry practice. In recent years, companies have experimented with lower velocities and have found that airflow velocity specifications ranging from 0.35 to 0.51 meters per second ± 20% could be successful, depending on the activities and equipment within the room. For example, in an empty room with no obstructions to the airflow, air velocities at 0.35 meters per second should be able to remove contamination effectively. There is no single value of average velocity or air change rate accepted by the industry for a given cleanroom classification. In general, higher values are used in rooms with a greater level of personnel activity or particle-generating process equipment. The lower value is used in rooms with fewer personnel, more stationary personnel and/or equipment with less particle-generating potential. Higher ACRs equate to higher airflows and more energy use. In most cleanrooms, human occupants are the primary source of contamination. Once a cleanroom is vacated, lower air changes per hour to maintain cleanliness are possible allowing for setback of the air handling systems. Finally, Variable Speed Drives (VSDs) should be used on all recirculation air systems allowing for air flow adjustments to optimize airflow or account for filter loading. The benefits include reduced capital costs and energy consumption.

In next month's Feature Article, we will continue our discussion of HVAC Technology for Cleanrooms.

Technical Tidbit: Hardware Cores Versus Software Cores

In this month's Technical Tidbit, we will discuss the differences between Hardware Cores and Software Cores. Engineers typically abbreviate the terms as Hard Cores and Soft Cores. Hard Cores and Soft Cores represent two options for incorporating intellectual property blocks, typically compute processing units, into a larger chip design.

Let's begin by providing a brief overview of Soft Cores. Soft Cores are provided by various chip design companies in the form of a Hardware Description Language, or HDL, file that can be synthesized. Synthesis refers to the process of turning the HDL code into a circuit schematic. The circuit schematic can then be incorporated into a larger schematic that might be implemented on a chip with standard cell libraries, or as a part of a Field Programmable Gate Array (FPGA). Soft Cores are not optimized from a layout perspective, so they are typically less compact and run more slowly. Because Soft Cores are implemented in standard cell libraries or FPGA cells, it would be difficult, and in some cases, impossible, to recognize a Soft Core in a larger chip design.

Next, let's provide a brief overview of Hard Cores. Hard Cores are typically crafted in advance by the chip design company. The design company would work with the IC manufacturer or foundry to ensure that the layout meets the requirements of the process technology, which would include simulating performance and behavior, and following the manufacturer's design rules. Because Hard Cores are laid out in advance, they are more compact than Soft Cores, and provide higher performance than Soft Cores. The performance increase can be as much as a factor of 10 to 50 times the performance of a Soft Core.

For a Soft Core circuit block, the implementation is defined by the HDL description. There are two common HDLs for chip design: the Very High-Speed Integrated Circuit (VHSIC) Hardware Description Language, known commonly as VHDL and Verilog. If the circuit is destined for an FPGA, the FPGA will need to be programmed to realize the CPU system. In Figure 1, we show an example of the HDL code on the left, and an example of a physical implementation of the HDL code on the right.

Figure 1- An excerpt from the VHDL code of a Soft Core processor (left), and the physical implementation of the Soft Core processor (right)

For a Hard Core circuit block, the implementation is defined in silicon. Design and Layout Engineers optimize the circuit block for layout compactness and performance prior to placing it into a larger design. In Figure 2, we show an example of the placement of an ARM Cortex A9 processor block within a larger Intel FPGA. As a point of reference, Intel's FPGA line of products is from the former FPGA design company, Altera, which Intel purchased near the end of 2015.

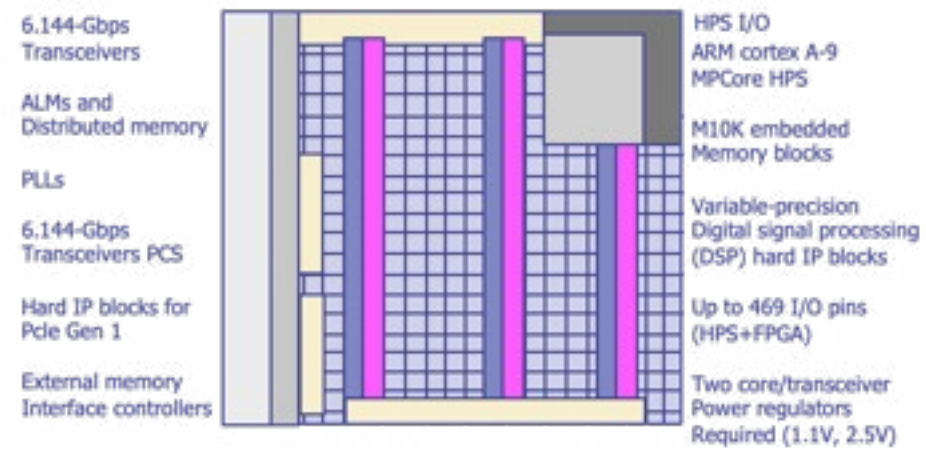

Figure 2- Placement of a Hard Core processor block within an Intel Cyclone 5 FPGA.

Although company literature might describe Soft Cores in terms of defined regions within a block diagram of a chip, like we show in Figure 3 on the left, in reality, the implementation of the Soft Core in the FPGA cells is more likely to look something like the darker blue regions in Figure 3 on the right.

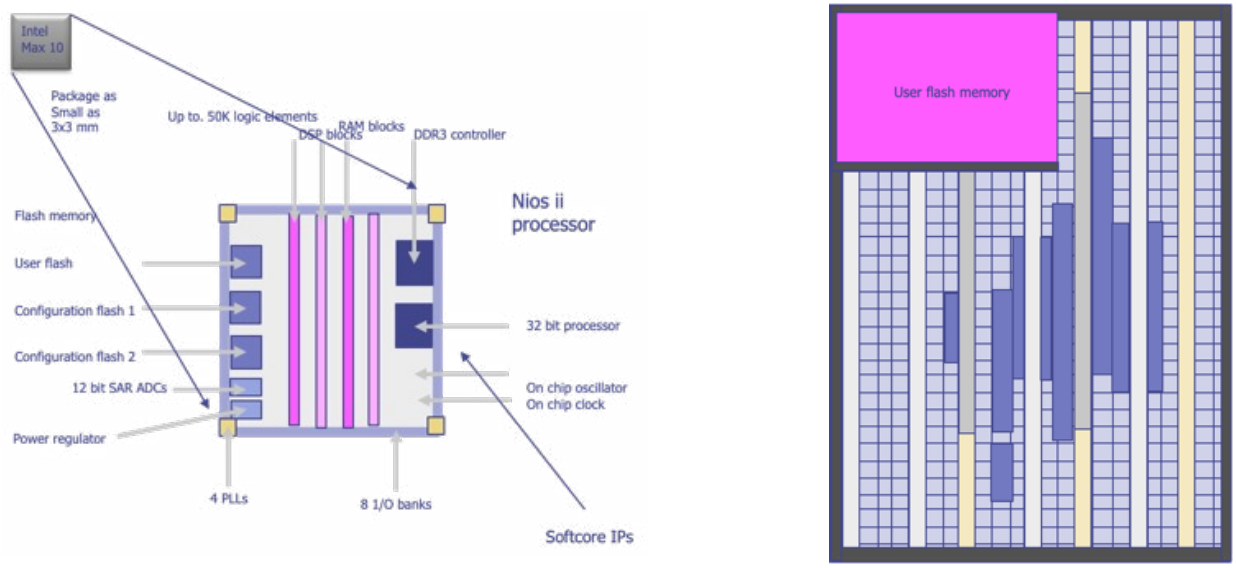

Figure 3- Block diagram of the Intel MAX 10 FPGA, highlighting the Soft Core intellectual property blocks (left), and the actual placement of the circuitry within the FPGA cells (right).

Figure 4 shows two diagrams of implementations of Hard Cores. In Figure 4, on the left, we show Intel's Cyclone 5 SoC. The Hard Core is a portion of the Hard Processor System, which is located in the upper right corner of the FPGA layout. In addition to the ARM hard core, there are other layout-defined elements like Joint Test Advisory Group (JTAG) debug and trace, Universal Serial Bus (USB) circuitry, ethernet, flash control, Synchronous DRAM (SDRAM) control, Controller Area Network (CAN) circuitry, Inter-Integrated Circuit (I2C) circuitry, Serial Peripheral Control (SPC) circuitry, General Purpose Input/Output (GPIO) circuitry, timers, and more. In Figure 4, on the right, we show the block diagram of a competitor product from Xilinx, the Zynq7000 FPGA.

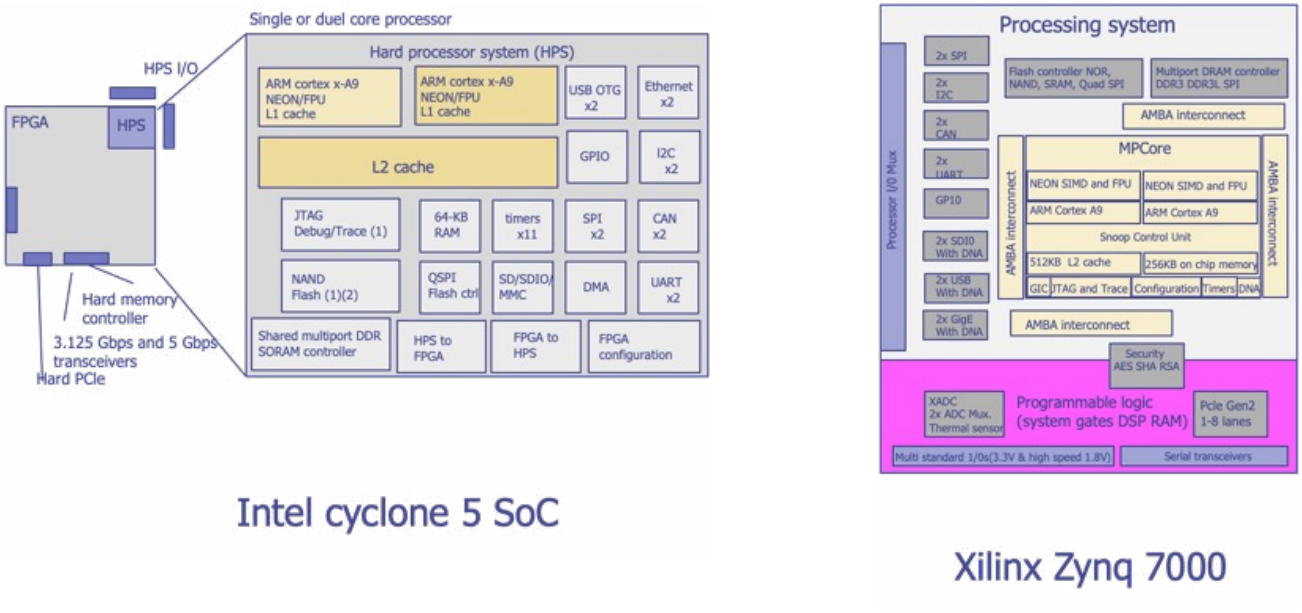

Figure 4- Intel Cyclone 5 FPGA, implemented as an SoC with Hard Core blocks in the upper right portion of the FPGA (left), and a circuit block diagram of the Xilinx Zynq7000 FPGA with Hard Core blocks (right).

Ask The Experts

Q: Why do we use a hot carrier injection (HCI) model for p-channel transistors that uses gate current (I_{gate}) for L>0.25um but uses substrate current (I_{sub}) for L<0.25um?

A: HCI-induced transistor degradation is well modeled by peak substrate current for the n-channel transistors and peak gate current for the p-channel transistors, at least for transistors for L>0.25 um. For L<0.25um p-channel transistors, the drive current tends to decrease as is the case in n-channel transistors after hot carrier stress. For L<0.25um p-channel transistors, worst-case lifetime occurs at maximum substrate current stress. The time-to-failure (TTF) model is the same as the n-channel transistor. The drive current for n-channel transistors tends to decrease after HCI stressing; however, the p-channel drive current may increase or decrease depending on the channel length and stress conditions. The off-state leakage can increase dramatically, especially for high drive current p-channel transistors.

Work from IBM back in 1997 showed that in advanced submicron technologies Hot Hole (HH) injection dominated the Channel Hot Carrier (CHC) damage in short effective channel length (L_{eff}) transistors, but not in long channel p-channel transistors where electron trapping still dominated at low gate voltage (V_g) biases equal to the threshold voltage (V_{th}) ($V_g = V_{th}$). In short channel devices, the worst CHC damage was observed when the drain voltage was equal to the gate voltage, and resulted in a decrease of the transconductance (G_{max}) and an increase in V_{th} as a function of time irrespective of the temperature and V_d applied.

Course Spotlight: ADVANCED CMOS/FINFET FABRICATION

OVERVIEW

Semiconductor and integrated circuit developments continue to proceed at an incredible pace. For example, today's microprocessor chips have one thousand times the processing power of those a decade ago. These challenges have been accomplished because of the integrated circuit industry's ability to track something known as Moore's Law. Moore's Law states that an integrated circuit's processing power will double every two years. This has been accomplished by making devices smaller and smaller. The question looming in everyone's mind is "How far into the future can this continue?" ***Advanced CMOS/FinFET Fabrication*** is a 1.5-day course that offers detailed instruction on the processing used in a modern integrated circuit, and the processing technologies required to make them. We place special emphasis on current issues related to manufacturing the next generation devices. This course is a must for every manager, engineer and technician working in the semiconductor industry, using semiconductor components or supplying tools to the industry.

By concentrating on the latest developments in CMOS and FinFET technology, participants will learn why FinFETs are fast becoming the technologies of choice at feature sizes below 20nm. Our instructors work hard to explain semiconductor processing without delving heavily into the complex physics and materials science that normally accompany this discipline.

Participants learn basic but powerful aspects about CMOS fabrication and FinFET technology. This skill-building series is divided into four segments:

1. Front End Of Line (FEOL) Overview. Participants study the major developments associated with FEOL processing, including Ion Implantation, Rapid Thermal Annealing (RTA) for implants and silicides, and Pulsed Plasma Doping. They also study alternate substrate technologies like SOI as well as High-k/Metal Gates for improved leakage control.
2. Back End Of Line (BEOL) Overview. Participants study the major developments associated with BEOL processing, including copper metallization and Low-k Dielectrics. They learn about why they're necessary for improved performance.
3. FinFET Manufacturing Overview. Participants learn how semiconductor manufacturers are currently processing FinFET devices and the difficulties associated with three-dimensional structures from a processing and metrology standpoint.
4. FinFET Reliability. They also study the failure mechanisms and techniques used for studying the reliability of these devices.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of Bulk technology, SOI technology and the technical issues.
2. Participants will understand how Hi-K/Metal Gate devices are manufactured.
3. Participants will also understand how FinFET devices are manufactured.
4. The seminar provides a look into the latest challenges with copper metallization and Low-k dielectrics.
5. Participants will understand the difficulties associated with non-planar structures and methods to alleviate the problems.
6. Participants will be able to make decisions about how to evaluate FinFET devices and what changes are likely to emerge in the coming years.
7. Participants will briefly learn about IC reliability and the failure modes associated with these devices.
8. Finally, the participants see a comparison between FinFETs and new alternatives (such as Gate All Around (GAA) structures and nanosheets).

COURSE OUTLINE

1. Advanced CMOS Fabrication – Introduction
2. Front End Of Line (FEOL) Processing
   a. SOI and FD-SOI
   b. Ion Implantation and Rapid Thermal Annealing
   c. Pulsed Plasma Doping
   d. Hi-K/Metal Gates
   e. Processing Issues
      i. Lithography
      ii. Etch
      iii. Metrology
3. Back End Of Line (BEOL) Processing
   a. Introduction and Performance Issues
   b. Copper
      i. Deposition Methods
      ii. Liners
      iii. Capping Materials
      iv. Damascene Processing Steps
   c. Lo-k Dielectrics
      i. Materials
      ii. Processing Methods
   d. Reliability Issues
4. FinFET Manufacturing Overview
   a. Substrates
      i. Bulk
      ii. SOI
   b. FinFET Types
   c. Process Sequence
   d. Processing Issues
      i. Lithography
      ii. Etch
      iii. Metrology
5. FinFET Reliability
   a. Defect density issues
   b. Gate Stack
   c. Transistor Reliability (BTI and Hot Carriers)
   d. Heat dissipation issues
   e. Failure analysis challenges
6. Future Directions for FinFETs
   a. Comparison of FinFETs and other Techniques (GAA, Nanosheets) – Are FinFETs a better choice?
   b. Scaling

Upcoming Courses:

Public Course Schedule:

Product Qualification Overview - September 11, 2023 (Mon.) | Phoenix, Arizona - $695

Advanced CMOS/FinFET Fabrication - September 25-26, 2023 (Mon.-Tues.) | Phoenix, Arizona - $995

Webinar Schedule:

IC Packaging Design and Modeling - September 18 - 21, 2023 (Mon. – Thurs.) | - $600

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To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered, please contact Jeremy Henderson at jeremy.henderson@semitracks.com

We are always looking for ways to enhance our courses and educational materials and look forward to hearing from you!