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InfoTracks

Semitracks Monthly Newsletter

Analog Building Blocks

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This month, we will continue our series of Feature Articles by discussing a class of circuits called reference circuits. These circuits are used in designs to provide a stable voltage that can be used as a reference voltage for the circuit. There are three basic types of reference circuits. The first type is the voltage divider. This is a simple circuit that can produce a reference voltage. The second type is the diode-referenced self-biasing circuit. This circuit is somewhat more complex, but yields a more stable voltage. And finally, there is the bandgap-referenced biasing circuit. This circuit is the most complex, but also provides the most stable reference voltage.

First, we will discuss the voltage divider which is a simple circuit that can provide a stable voltage. It has the advantage of being insensitive to temperature and process variations. In Figure 1, we show three circuits that are examples of voltage dividers. The first divider, shown on the left in Figure 1, is made from resistors. In order to reduce power dissipation, one must design R1 and R2 to be rather large. This can take up valuable real estate on the integrated circuit. One method for reducing the area is to use an n-channel transistor in lieu of R2, as shown at the center of Figure 1. This circuit requires much less area. Finally, one can minimize the area of the voltage divider by using the circuit shown on the right of Figure 1. In this circuit, we use a p-channel transistor in lieu of R1.

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Semiconductor, Microelectronics, Microsystems, and Nanotechnology Training

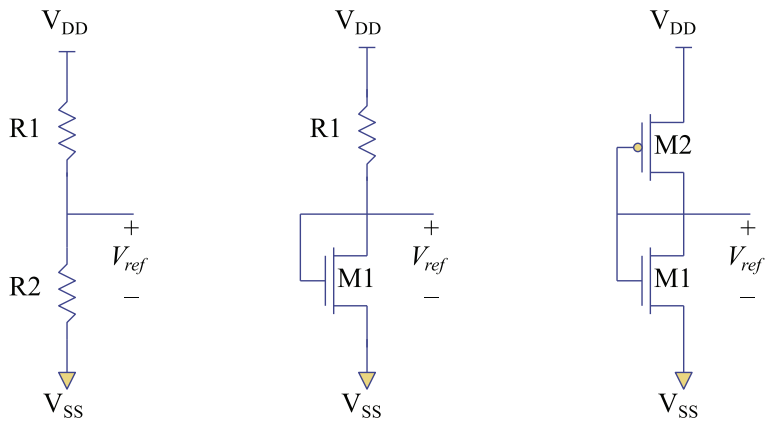


Figure 1. Voltage divider examples.

Next, we will discuss a diode-referenced self-biasing circuit (shown in Figure 2). This circuit provides a more stable voltage than the circuits shown in Figure 1. The cascode mirrors created with transistors M1 through M8 force the same current down each leg of the circuit. D2 can be sized relative to D1 such that the effect of the temperature coefficient of the thermal voltage is minimized. Because of wafer-to-wafer variations, R1 can vary by a sizable amount. If designers require more control, then they might consider using a bandgap-referenced circuit, discussed next.

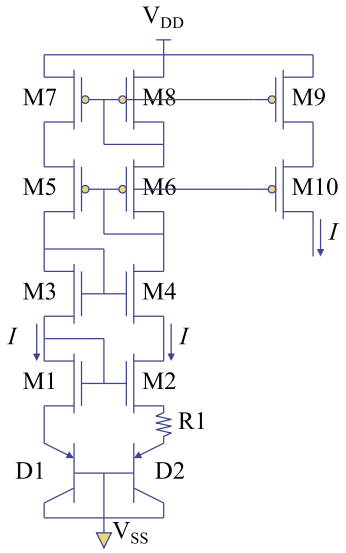
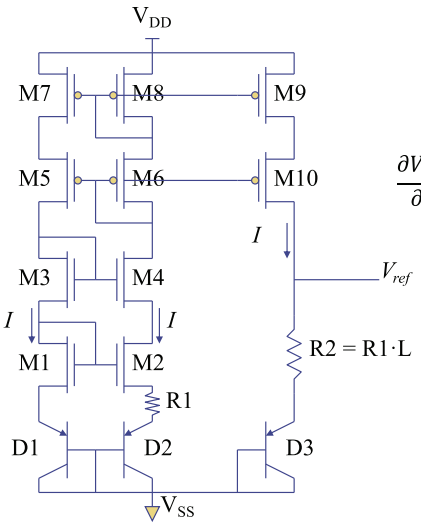


Figure 2. Diode-referenced self-biasing circuit.

Last, we will discuss a bandgap-referenced circuit which utilizes the fact that there is a positive temperature coefficient associated with the thermal voltage, and a negative temperature coefficient associated with the diode forward voltage. These two effects can be made to cancel each other out to

produce a circuit that has a zero-temperature coefficient, making it the most stable reference circuit. Referring to Figure 3, diode D2 is the same size as diode D3, and Resistor R2 is L times larger than R1. The temperature coefficient can be zeroed out by examining the derivative of the equation on the right in Figure 3 and solving the equation when the derivative of vref is equal to zero. The thermal coefficients of the thermal voltage, the diode voltage, and n can be determined from the IC process, and values for K and L can be set in the design/layout.



$$V_{ref} = (L \cdot n \cdot \ln K)V_T + V_{D3}$$

$$\frac{\partial V_{ref}}{\partial T} = L \cdot n \cdot \ln K \cdot \frac{\partial V_T}{\partial T} + \frac{\partial V_{D3}}{\partial T} = 0$$

Figure 3. Bandgap-referenced self-biasing circuit.

In next month's Feature Article, we will discuss amplifier circuits.

Technical Tidbit

Interconnect Scaling and Resistivity

This month's Technical Tidbit covers interconnect scaling and resistivity. Most people think about scaling in terms of the diagrams and equations we show in Figure 1 below. This type of thinking works okay for bulk metals, but this is not true in practice anymore. We need to take into account grain boundaries and scattering when evaluating interconnect behavior at the nanoscale.

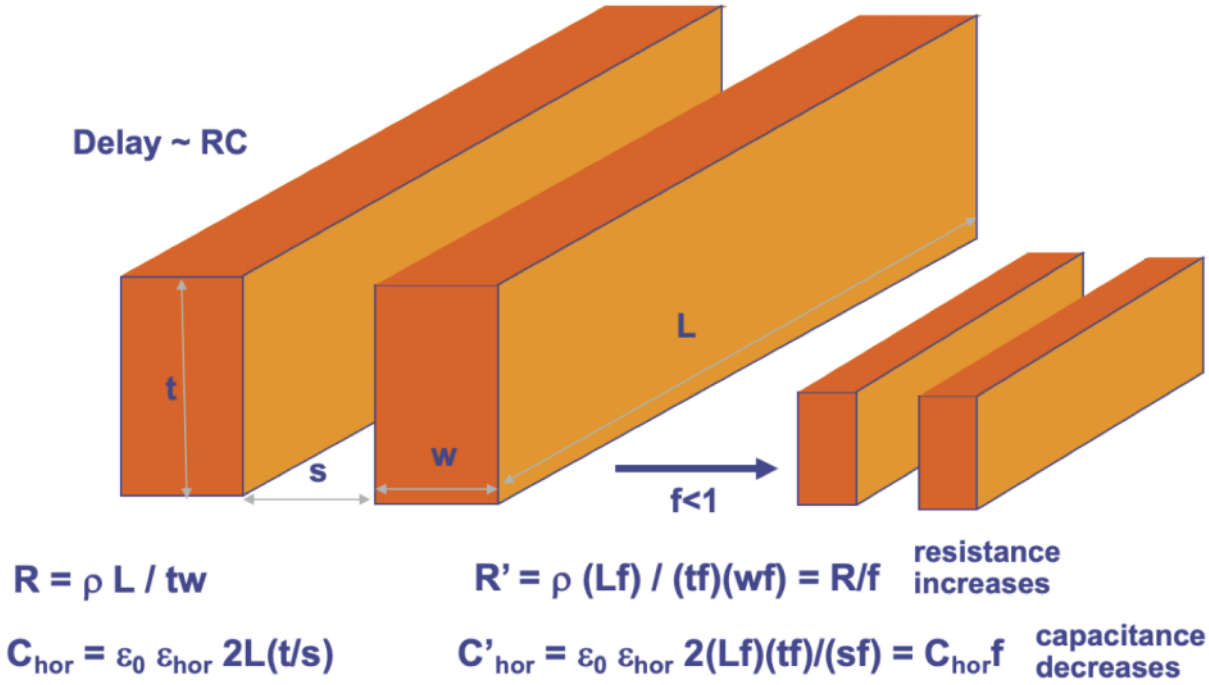


Figure 1. Diagrams and equations that represent the effects of scaling, assuming bulk metal resistivity properties.

Electron scattering at the grain boundaries is becoming a bigger component of the overall resistance in metal interconnect. Also, the cross-sectional area of the Tantalum/Tantalum Nitride liner is becoming a bigger component of the overall cross-sectional area of the metal interconnect, which affects the

resistance. The graph in Figure 2 shows the measured and simulated values for aluminum and copper. Notice that as the linewidths go down, the actual measured values begin to diverge away from the simulation, increasing even faster. This increased resistivity in narrow lines is due to grain boundary scattering, surface scattering, and increased resistance in the tantalum-based barrier layer, as shown on the right in Figure 2.

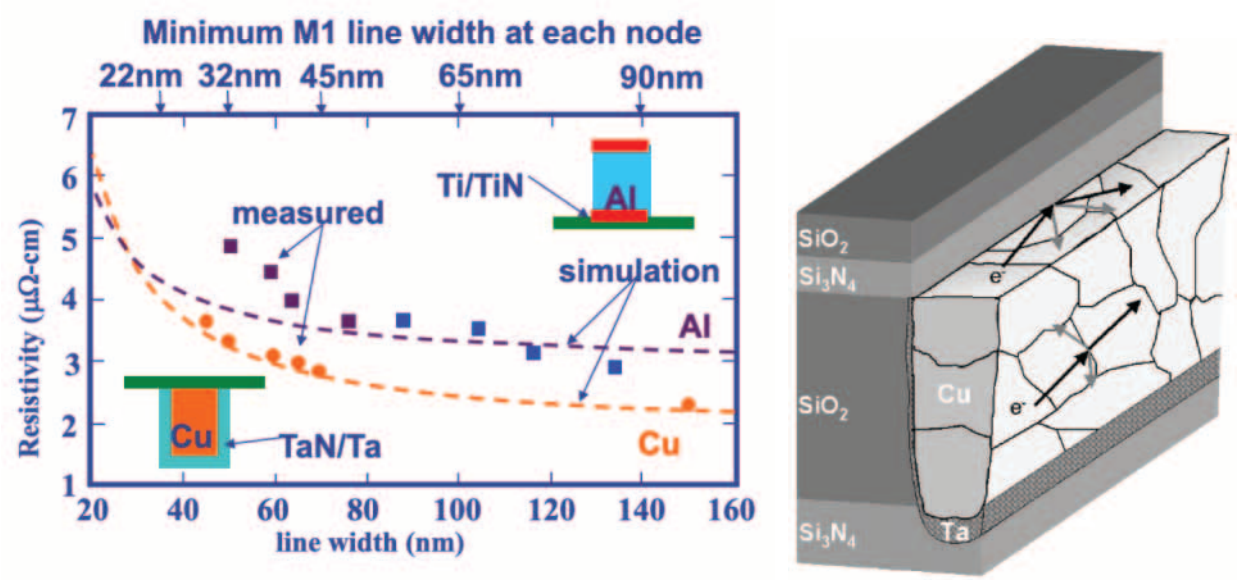


Figure 2. Graph depicting resistivity as a function of line width (left), and diagram illustrating grain structure and electron scattering in metal interconnect (right).

Ask the Experts

Q: I have a quick question. When semiconductor manufacturers use Eutectic solder attach for the bond wires - what are they talking about?

A: I think you might be mixing two things together. Eutectic solder attach is typically used as a die attach material and is placed on the leadframe, or in the well of a ceramic package as a preform, and then melted using an oven to create a bond between the bottom of the die and the leadframe or package well to provide an electrical connection to ground and a heat dissipation path. Bond wires are typically connected between the bond pads on the top of the die and leadframe using a thermosonic process (heat, compression and ultrasonic energy) to provide a path for electrical signals to the circuitry in the system outside of the IC package. Hopefully that helps to clear up some of the confusion.

Spotlight: Semiconductor Reliability and Product Qualification

OVERVIEW

Package reliability and product qualification continues to evolve with the electronics industry. New electronics applications require new approaches to reliability and qualification. In the past, reliability meant discovering, characterizing and modeling failure mechanisms and determining their impact on the reliability of the circuit. Today, reliability can involve tradeoffs between performance and reliability, assessing the impact of new materials, dealing with limited margins, etc. in particular, the proliferation of new package types. This requires information on subjects like: statistics, testing, technology, processing, materials science, chemistry, and customer expectations. While customers expect high reliability levels, incorrect testing, calculations, and qualification procedures can severely impact reliability. Your company needs competent engineers and scientists to help solve these problems. ***Semiconductor Reliability and Qualification*** is a four-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor reliability and qualification. This course is designed for every manager, engineer, and technician concerned with reliability in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

What Will I Learn By Taking This Class?

Participants learn to develop the skills to determine what failure mechanisms might occur, and how to test for them, develop models for them, and eliminate them from the product.

1. **Overview of Reliability and Statistics.** Participants learn the fundamentals of statistics, sample sizes, distributions and their parameters.
2. **Failure Mechanisms.** Participants learn the nature and manifestation of a variety of failure mechanisms that can occur both at the die and at the package level. These include: time-dependent dielectric breakdown, hot carrier degradation, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, etc.
3. **Qualification Principles.** Participants learn how test structures can be designed to help test for a particular failure mechanism.
4. **Test Strategies.** Participants learn about the JEDEC test standards, how to design screening tests, and how to perform burn-in testing effectively.

COURSE OBJECTIVES

1. The seminar will provide participants with an in-depth understanding of the failure mechanisms, test structures, equipment, and testing methods used to achieve today's high reliability components.
2. Participants will be able to gather data, determine how best to plot the data and make inferences from that data.
3. The seminar will identify the major failure mechanisms, explain how they are observed, how they are modeled, and how they are eliminated.
4. The seminar offers a variety of video demonstrations of analysis techniques, so the participants can get an understanding of the types of results they might expect to see with their equipment.
5. Participants will be able to identify the steps and create a basic qualification process for semiconductor devices.

6. Participants will be able to knowledgeably implement screens that are appropriate to assure the reliability of a component.
7. Participants will be able to identify appropriate tools to purchase when starting or expanding a laboratory.

COURSE OUTLINE

Day 1 (Lecture Time 8 Hours)

1. Introduction to Reliability
    1. Basic Concepts
    2. Definitions
    3. Historical Information
2. Statistics and Distributions
    1. Basic Statistics
    2. Distributions (Normal, Lognormal, Exponent, Weibull)
    3. Which Distribution Should I Use?
    4. Acceleration
    5. Number of Failures

Day 2 (Lecture Time 8 Hours)

1. Overview of Die-Level Failure Mechanisms
    1. Time Dependent Dielectric Breakdown
    2. Hot Carrier Damage
    3. Negative Bias Temperature Instability
    4. Electromigration
    5. Stress Induced Voiding
2. Package Level Mechanisms
    1. Ionic Contamination
    2. Moisture/Corrosion
        1. Failure Mechanisms
        2. Models for Humidity
        3. Tja Considerations
        4. Static and Periodic stresses
        5. Exercises
    3. Thermo-Mechanical Stress
        1. Models
        2. Failure Mechanisms
    4. Interfacial Fatigue
        1. Low-K fracture
    5. Thermal Degradation/Oxidation

Day 3 (Lecture Time 8 Hours)

1. Package Attach (Solder) Reliability
    1. Creep/Sheer/Strain
    2. Lead-Free Issues
    3. Electromigration/Thermomigration
    4. MSL Testing
    5. Exercises
2. TSV Reliability Overview
3. Board Level Reliability Mechanisms
    1. Interposer
    2. Substrate
4. Electrical Overstress/ESD
5. Test Structures and Test Equipment
6. Developing Screens, Stress Tests, and Life Tests
    1. Burn-In
    2. Life Testing
    3. HAST
    4. JEDEC-based Tests
    5. Exercises

Day 4 (Lecture Time 8 Hours)

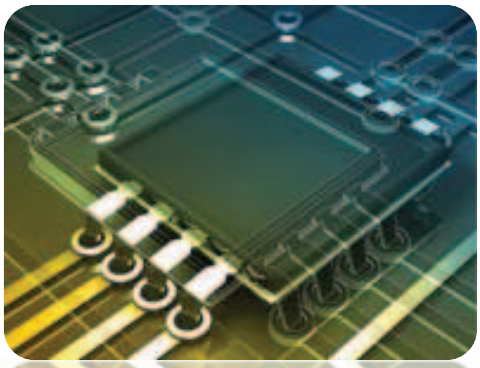
1. Calculating Chip and System Level Reliability
2. Developing a Qualification Program
    1. Process
    2. Standards-Based Qualification
    3. Knowledge-Based Qualification
    4. MIL-STD Qualification
    5. JEDEC Documents (JESD47H, JESD94, JEP148)
    6. AEC-Q100 Qualification
    7. When do I deviate? How do I handle additional requirements?
    8. Exercises and Discussion

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the failure analysis process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers hundreds of pages of additional reference material the participants can use back at their daily activities.

The Semitracks Analysis Instructional Videos™

One unique feature of this workshop is the video segments used to help train the students. Reliability Analysis is a visual discipline. The ability to identify nuances and subtleties in graphical data is critical to locating and understanding the defect. Some tools output video images that must be interpreted by engineers and scientists. No other course of this type uses this medium to help train the participants. These videos allow the analysts to directly compare material they learn in this course with real analysis work they do in their daily activities.



Upcoming Webinars

(Click on each item for details)

Design for Reliability WEBINAR

2 sessions of 4 hours each
Europe: June 13 – 14, 2022 (Mon – Tue),
1:00 P.M. – 5:00 P.M. CET

IC Packaging Technology WEBINAR

4 sessions of 4 hours each
US: June 13 – 16, 2022 (Mon – Thur)
9:00 A.M. – 1:00 P.M. PDT

Semiconductor Reliability / Product Qualification WEBINAR

4 sessions of 4 hours each
US: August 15 – 18, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

Wafer Fab Processing WEBINAR

4 sessions of 4 hours each
US: October 3 – 6, 2022 (Mon – Thur),
8:00 A.M. – 12:00 NOON PDT

Feedback

If you have a suggestion or a comment regarding our courses, online training, discussion forums, or reference materials, or if you wish to suggest a new course or location, please call us at 1-505-858-0454 or Email us (info@semitracks.com).
To submit questions to the Q&A section, inquire about an article, or suggest a topic you would like to see covered in the next newsletter, please contact Jeremy Henderson by Email (jeremy.henderson@semitracks.com).
We are always looking for ways to enhance our courses and educational materials.

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To post, read, or answer a question, visit our forums.
We look forward to hearing from you!