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InfoTracks

Semitracks Monthly Newsletter

Overview of Statistical Process Control Part 3

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In this document, we continue with our overview of statistical process control.

Unit	Bonder 1	Bonder 2	Bonder 3	Bonder 4	Bonder 5	Bonder 6	Bonder 7	Bonder 8
1	10.28	9.92	10.22	10.31	10.38	9.37	10.37	10.40
2	10.17	10.05	10.29	10.37	10.23	10.12	10.26	10.20
3	10.19	10.07	10.24	10.25	10.17	10.08	10.27	10.28
4	10.31	10.06	10.28	10.28	10.28	9.90	10.38	10.29
5	10.29	10.05	10.27	10.42	10.35	10.08	10.44	10.26
6	10.40	10.13	10.20	10.33	10.35	9.89	10.42	10.29
7	10.27	10.11	10.34	10.28	10.35	10.45	10.21	10.25
8	10.21	10.13	10.28	10.30	10.30	10.01	10.28	10.43
9	10.20	10.16	10.26	10.15	10.39	10.36	10.22	10.26
10	10.35	10.08	10.33	10.35	10.34	10.18	10.22	10.23
11	10.34	10.04	10.32	10.24	10.29	9.84	10.31	10.33
12	10.31	10.17	10.25	10.41	10.33	10.38	10.30	10.35
13	10.35	10.01	10.26	10.24	10.17	10.38	10.23	10.21
14	10.34	10.10	10.34	10.43	10.39	10.13	10.38	10.31
15	10.30	10.12	10.33	10.30	10.24	10.02	10.19	10.35
16	10.33	10.01	10.34	10.31	10.24	9.88	10.37	10.28
17	10.25	10.14	10.25	10.27	10.27	9.38	10.27	10.35
18	10.33	10.10	10.26	10.38	10.19	10.26	10.33	10.29
19	10.30	10.06	10.26	10.27	10.35	10.09	10.35	10.33
20	10.34	10.12	10.40	10.32	10.34	10.08	10.41	10.28

Figure 5. Example of a multiple tools data table.

The control chart can also be used in a situation where there is more than one tool. This data table in Figure 5 shows the bonding results from 8 different bonding tools, and the resulting pull strengths. We will use this data as an example in the following control charts.

In this Issue:

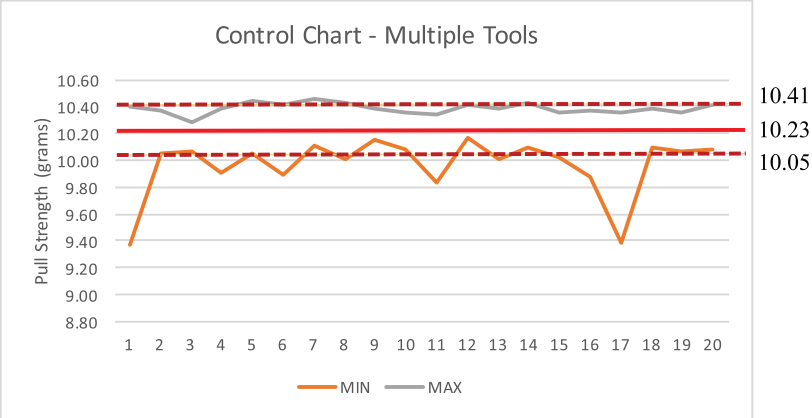


Figure 6. Example of MIN MAX chart.

First, we show the MIN MAX chart in Figure 6. We create this chart by taking the minimum of each of the bonding strengths on the unit, and the maximum of the bonding strengths on the unit. The solid line shows the average, and the dashed lines show the standard deviation in the values. When interpreting a group chart, you look for runs in the MAX and MIN positions. On this chart, the MIN plot points are predominately associated with bonders 2 and 6. This means that those bonders are consistently generating bonds with lower pull force than the other bonders. Also, the majority of the MAX moving range plot points are from bonder 6. This means that the variability from that head is consistently greater than the other heads.

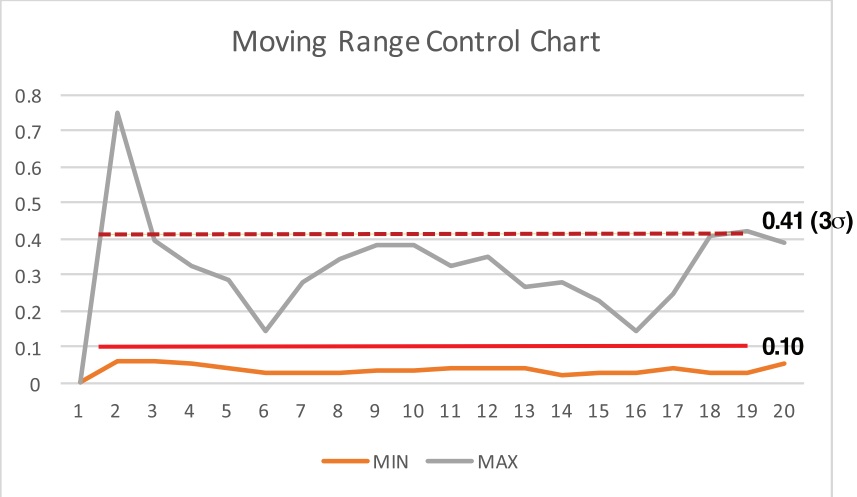


Figure 7. Example of moving range chart.

Figure 7 is an example of a moving range chart on the same data set. This looks at the difference between one bond and the next on the same tool. We show the mean as a solid color red, and the 3σ limit as a dashed red line.

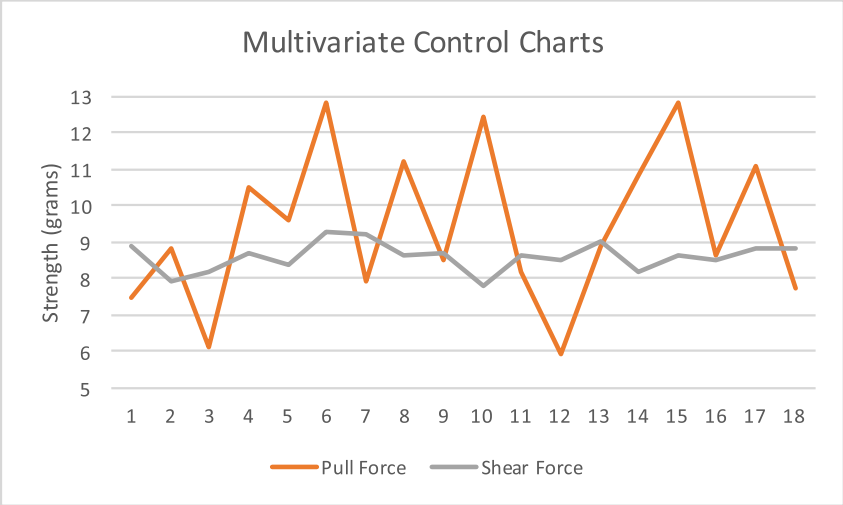


Figure 8. Example of multivariate control chart.

Another form of the control chart can be used for multivariate control, or the control of 2 or more characteristics at the same time. This chart shows both pull and shear force strength for 18 bonds.

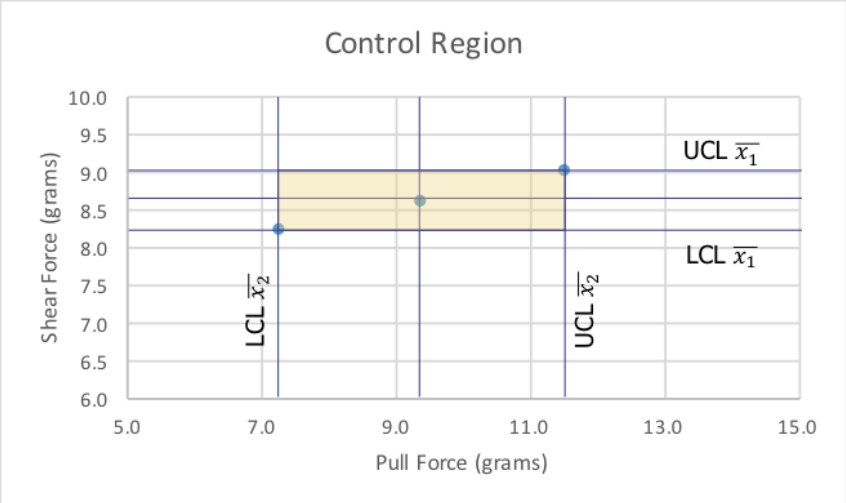


Figure 9. Control region: independent limits.

For these data points, we can define two control regions, one plotted on the x-axis, and the other plotted on the y-axis. Here, we plot pull force on the x-axis, and shear force on the y-axis. The box is bounded by the upper and lower control limits of the two characteristics, or variables.

If there are two variables then we will most likely need to control them both at the same time.

$$\chi_0^2 = \frac{n}{\sigma_1^2\sigma_2^2 - \sigma_{12}^2}\left[\sigma_2^2(\bar{x}_1 - \mu_1)^2 + \sigma_1^2(\bar{x}_2 - \mu_2)^2 - 2\sigma_{12}(\bar{x}_1 - \mu_1)(\bar{x}_2 - \mu_2)\right]$$

The chi-square statistic for this scenario is given by this equation: where μ_1 and μ_2 represent the means of x_1 and x_2; σ_1 and σ_2 represent the standard deviations; σ_{12} is the covariance of x_1 and x_2; $\bar{x_1}$ and $\bar{x_2}$ represent the sample averages. When the covariance term is zero, the ellipse is a zero degree ellipse; when it is greater than zero, the ellipse will be angled. The disadvantage of this type of analytical approach however, is that one loses time-related information, and it is difficult to plot if more than two variables are involved.

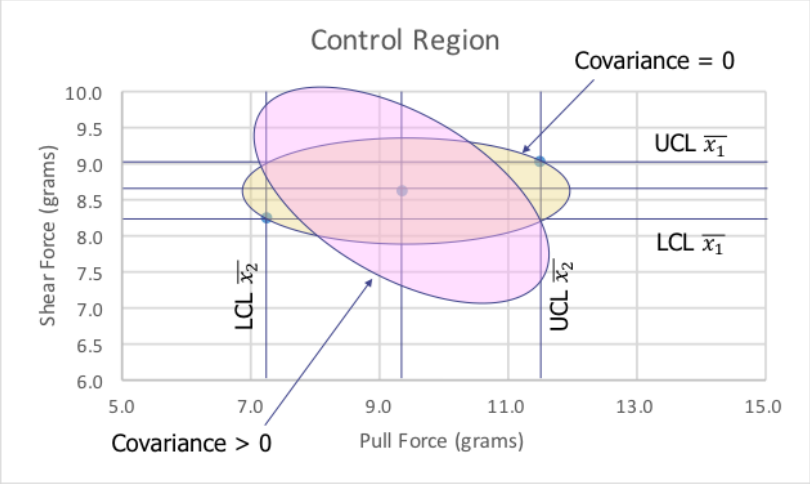


Figure 10. Control region: independent limits (cont.).

In Figure 10 we show the chi-square statistic for a situation in which the covariance is zero, and for a situation in which the covariance is greater than zero. Let's go back to the zero-covariance example for a minute. Both variables will generate normal distributions. The chance that both variables exceed the control limits at the same time is quite rare. In fact, the chance that one would exceed the control limits is most likely to happen at the center of the distribution of the other variable. This gives the chi-square statistic its elliptical shape.

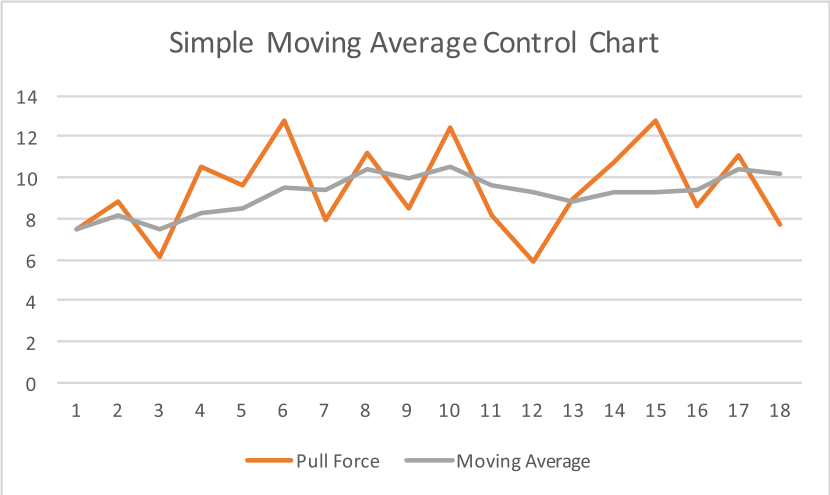


Figure 11. Basic moving average control chart.

Let's move on and briefly discuss the moving average chart (Figure 11). We can define a simple moving average by the equation shown here.

$$M_i = \frac{x_i + x_{i-1} + \ldots + x_{i-w+1}}{w}$$

Here we again show our pull force data in orange, and the simple moving average in gray. As the number of data points *i* increases, the moving average will become more constant.

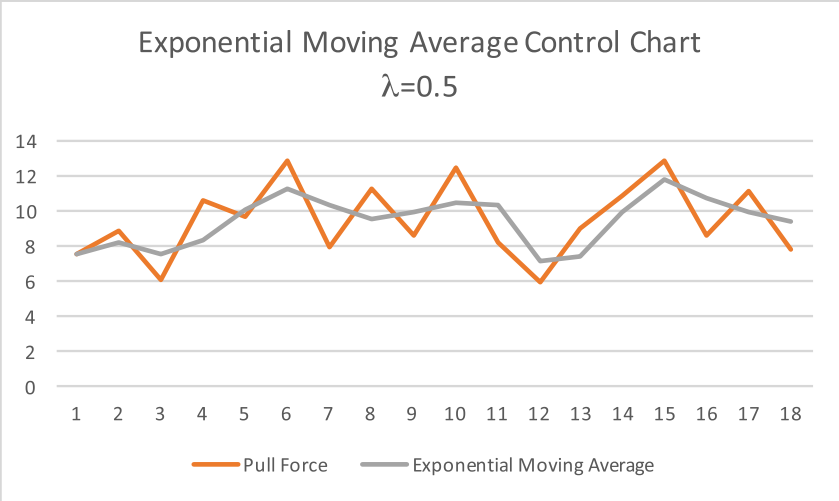


Figure 12. Exponential weighted moving average control chart.

Another form of moving average is the exponential weighted moving average (Figure 12). This type of moving average favors the more recent values compared to older values. It is also sometimes known as the geometric moving average. The equation to define each value is shown here.

$$z_i = \lambda x_i + (1 - \lambda) z_{i-1} \quad \text{where} \quad 0 < \lambda \leq 1$$

Here again is our pull force data, shown in orange, and the exponential moving average, shown in gray.

Finally, there is the Cusum chart. This type of chart can sometimes detect shifts that the Western Electric rules will miss. This chart, like the moving average charts, incorporates historical info by plotting cumulative sums of the sample deviations from a target value. We calculate the values using this equation.

$$C_i = \sum_{j=1}^{i} (\bar{x}_j - \mu_0)$$

If the process is stable around its target mean value, then the sum will be a random value with a zero mean. However, if the process drifts up, then a positive drift will develop in the Cusum chart.

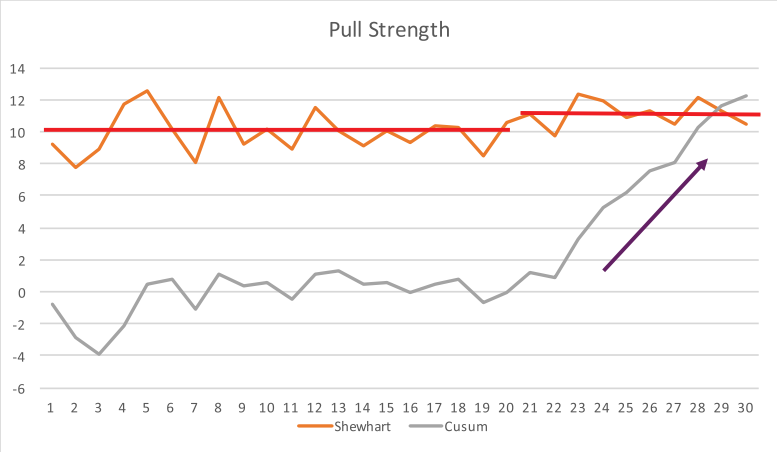


Figure 13. Example of Cusum chart.

Figure 13 is an example of a Cusum chart, again using pull strength data. We show the Cusum data points in gray. Notice that when the values increase somewhat—like we show with the two red lines—the Cusum values increase fairly dramatically, making this a great way to look for small changes.

To be continued next month…

Technical Tidbit

Process Corners

This month's technical tidbit covers the topic of process corners. Engineers use process corners to characterize a process or product to help ensure it will meet the customer's expectations over the operation conditions.

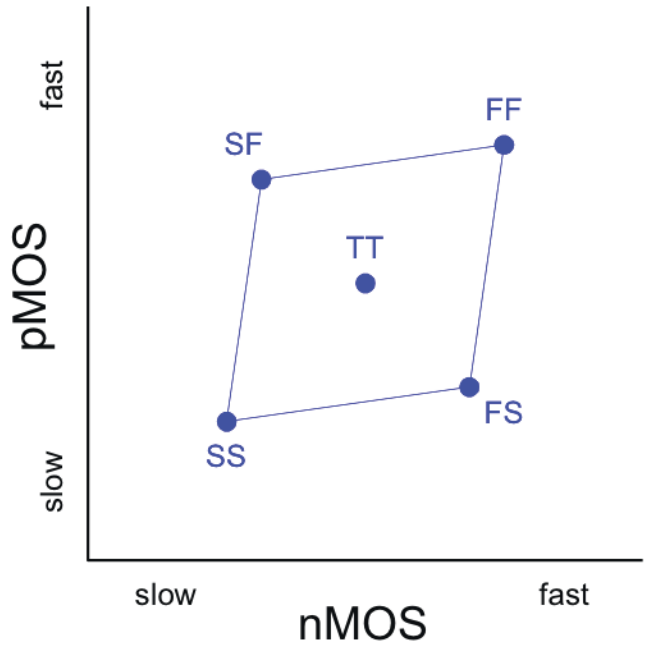


Figure 1. Diagram illustrating fast and slow process corners.

First, we need to discuss why the notion of a process corner is important. All devices have statistical variation, due to manufacturing variation that occurs naturally during processing. Quite often this type of distribution follows a normal distribution since it is caused by many small errors adding together - the principle behind the Central Limit Theorem. Because of this variation, foundries provide the range of values associated with key device parameters from four different corners, fast-fast (denoted FF), slow-slow (denoted SS), fast-slow (denoted FS), slow-fast (denoted SF) and the center, or typical-typical (denoted TT). These terms correspond to the n- and p-channel transistors, with the first letter corresponding to the n-channel transistor, and the second corresponding to the p-channel transistor. The FF corner is associated with the highest frequency and most leakage, and sets the power specification and the best performance. These transistors would have short effective channel lengths, thin gate oxides, low threshold voltages, and low contact resistances. Conversely, the SS corner is associated with the lowest frequency, and consumes the least power. These transistors would have long effective channel lengths, thick gate oxides, high threshold voltages, and high contact resistances.

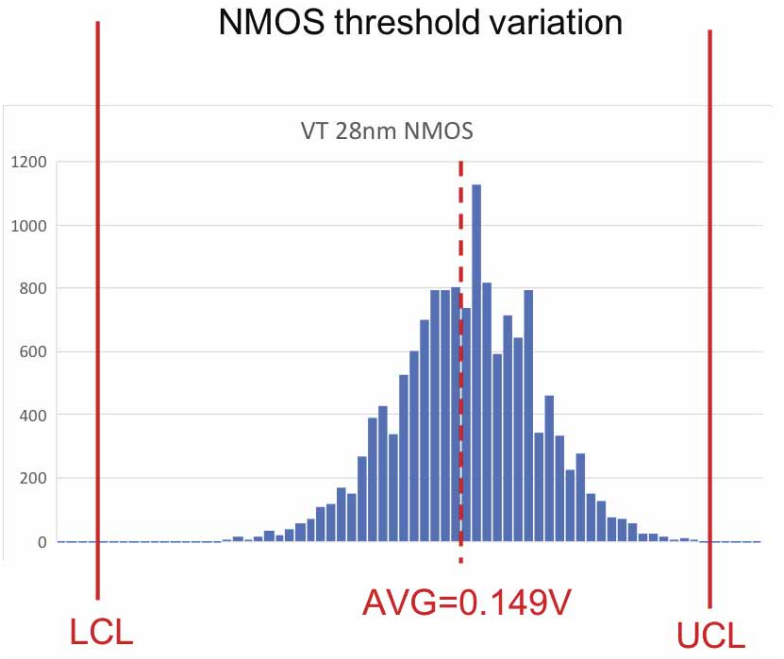


Figure 2. Distributions that can lead to corners in a process.

This parametric variation, although present in every process, can be minimized by process control during production. Engineers will typically measure values from scribeline test structures on each wafer during production, and establish pass-fail parameters. One might set up a control chart to monitor the process variation, use simplified equations for design and process tradeoffs. These values may be stored in a database for both statistical analysis and yield analysis. We show an example of such a dataset in Figure 2. LCL represents the Lower Control Limit, and UCL represents the Upper Control Limit.

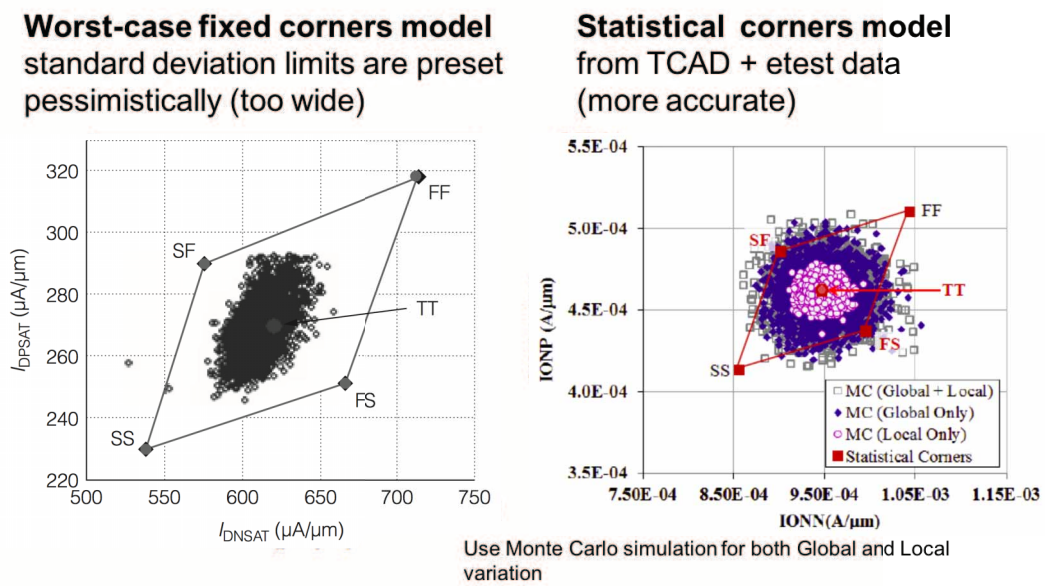


Figure 3. Examples of process corners for on-current, based on various factors, generated with Monte Carlo simulation software.

Engineers model process corners in several ways. One way is to model them as a worst-case scenario, like we show on the left in Figure 3. The bounding box represents the 4 corners of the process corner diagram. These limits are set too wide, or in other words, they are too pessimistic. Another way to model them is to use a statistical corners model that uses results from Technology Computer Aided Design, or TCAD, and scribeline test data, which tends to be more accurate. We show an example of this approach on the right in Figure 3.

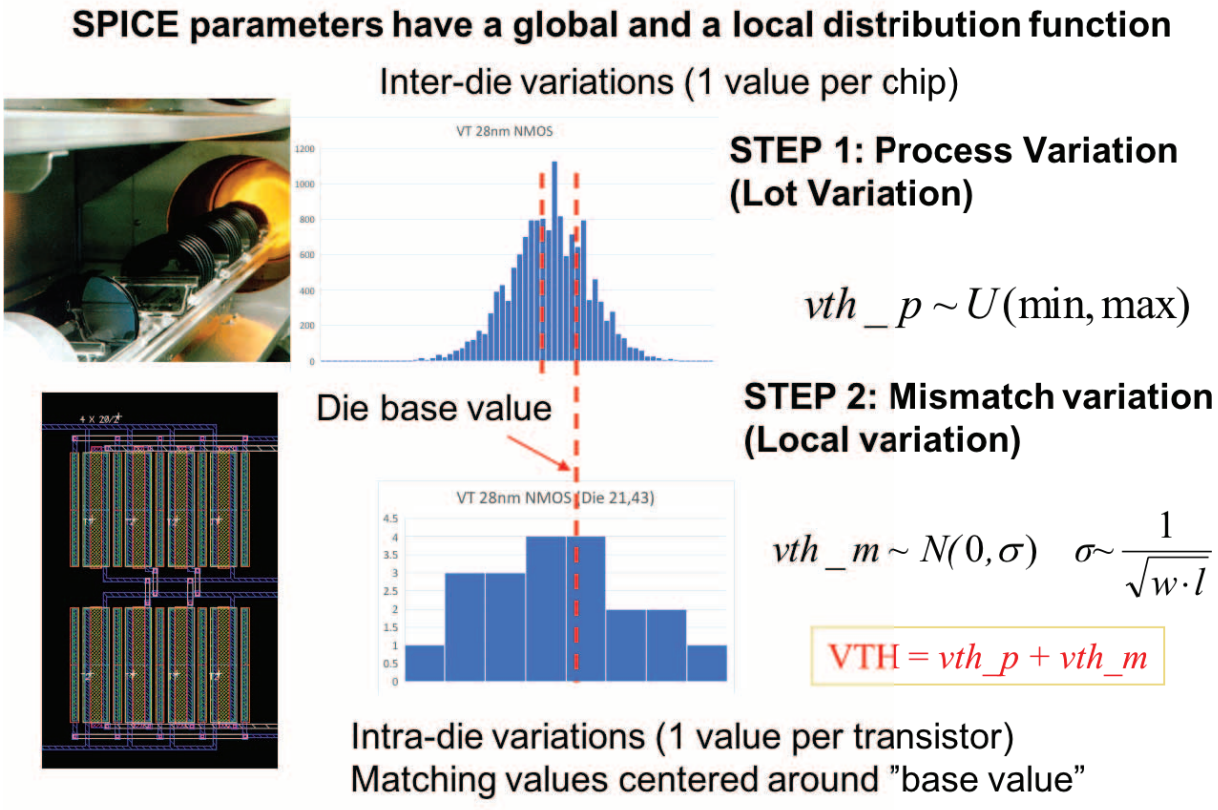


Figure 4. Illustration of intra-die versus inter-die variations.

Another approach to modeling process corners is to use Monte Carlo models. One can use SPICE parameters that have both local and global variations. This allows the engineer to examine variations across a die, and across a wafer or wafer lot. The upper set of data in Figure 4 shows an example of variations across the wafer lot, and the lower set of data shows mismatch variations across a die.

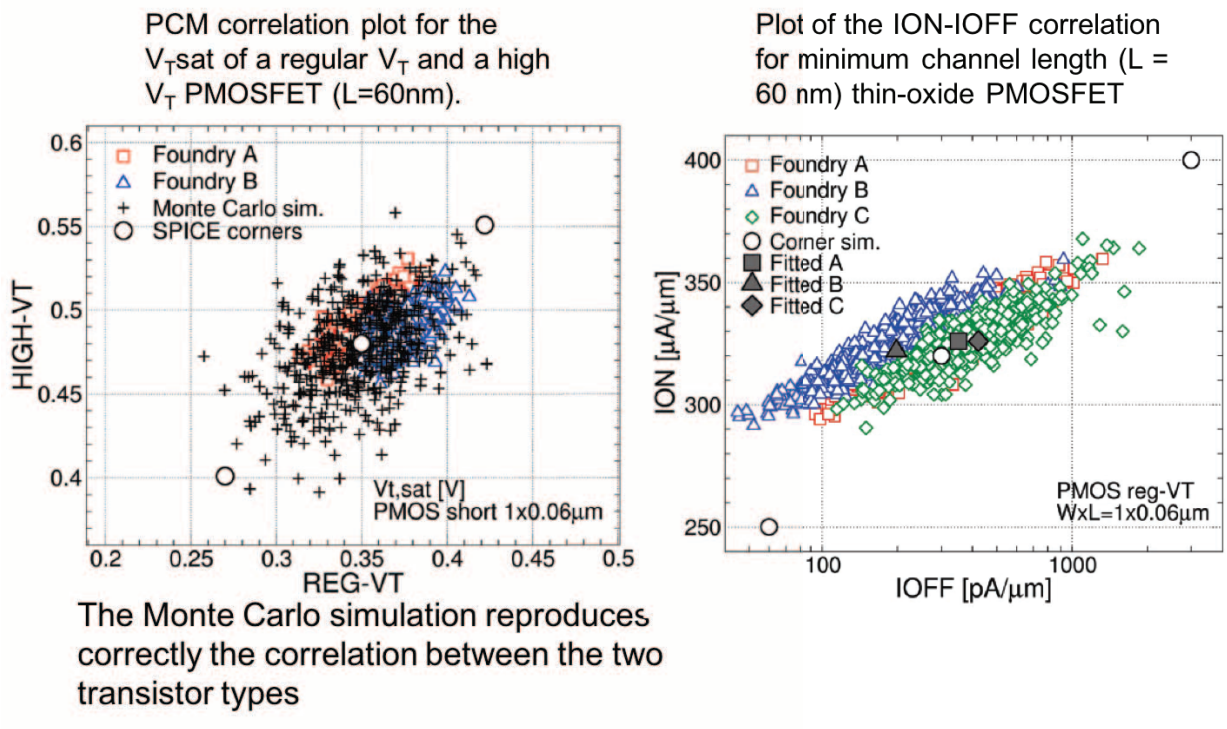


Figure 5. Examples of simulation results for threshold voltage, and on-vs-off current for different foundry processes.

Figure 5 is an example from a 65nm CMOS process. In the scatter plot on the left, we show process control monitor correlation for the saturated threshold voltage of a regular threshold voltage PMOS transistor and a high threshold voltage PMOS transistor. We show data from two foundries, Monte Carlo simulations, and SPICE corner simulations. The Monte Carlo simulations provide a reasonable correlation to the measured data. We show a similar analysis for I-ON vs. I-OFF in the right-hand plot for three foundries. Notice that the SPICE corner simulations are well outside the measured data, but the fitted data don't account for the spread within the measured data.

Ask the Experts

Q: Why do some tests use a sample size of 3?

A: 3 is sometimes considered to be sufficient to establish a value that is within a certain percentage of the mean with 90% confidence. This of course, assumes that you have a normal distribution of values.

Spotlight: IC Packaging Technology

OVERVIEW

Overview: Integrated Circuit packaging has always been integral to IC performance and functionality. An IC package serves many purposes: (1) pitch conversion between the fine features of the IC die and the system level interconnection, (2) chemical, environmental and mechanical protection, (3) heat transfer, (4) power, ground and signal distribution between the die and system, (5) handling robustness, and (6) die identification among many others. Numerous critical technologies have been developed to serve these functions, technologies that continue to advance with each new requirement for cost reduction, space savings, higher speed electrical performance, finer pitch, die surface fragility, new reliability requirements, and new applications. Packaging engineers must fully understand these technologies to design and fabricate future high-performance packages with high yields at exceptional low-costs to give their company a critical competitive advantage.

This two-day class will detail the vital technologies required to construct IC packages in a reliable, cost effective, and quick time to market fashion. When completed, the participant will understand the wide array of technologies available, how technologies interact, what choices must be made for a high-performance product vs. a consumer device, and how such choices impact the manufacturability, functionality, and reliability of the finished product. An emphasis will be given to manufacturing, processes and materials selection tailoring and development. Each fundamental package family will be discussed, including flip chip area array technologies, Wafer Level Packaging (WLP), Fan-Out Wafer Level Packaging (FO-WLP), and the latest Through Silicon Via (TSV) developments. Additionally, future directions for each package technology will be highlighted, along with challenges that must be surmounted to succeed.

WHAT WILL I LEARN BY TAKING THIS CLASS?

1. **Molded Package Technologies.** Participants learn the fundamentals of molding critical to leaded, leadless, and area array packaging, enabling them to eliminate problems such as flash, incomplete fill, and wire sweep.
2. **Flip Chip Technologies.** Participants learn the fundamentals of plating, bumping, reflow, underfill, and substrate technologies that are required for both high performance and portable products.
3. **Wafer Level Packages.** Participants learn the newest technologies that enable the increasingly popular Wafer Chip Scale Level Packages (WCSPs) and Fan-Out Wafer Level Packages (FO-WLPs).
4. **Through Silicon Via Packages and Future Directions.** Participants will know the latest advances in the recently productized TSV technology, as well as future directions that will lead to the products of tomorrow.

COURSE OBJECTIVES

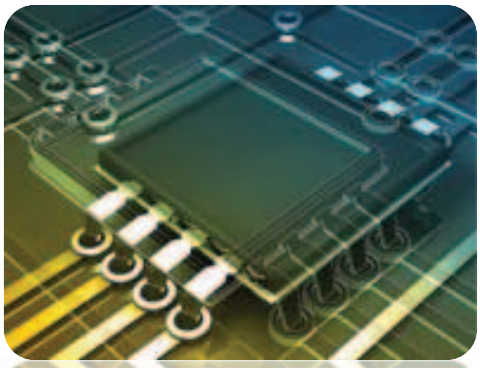
1. The course will supply participants with an in-depth understanding of package technologies current and future.
2. Potential defects associated with each package technology will be highlighted to enable the student to identify and eliminate such issues in product from both internal assembly and OSAT houses.

3. Cu and solder plating technologies will be described with special emphasis on package applications in TSVs and Cu pillars for FO-WLPs. Emphasis will be placed on eliminating issues such as reliability, non-uniformity, void free thermal aging performance, and contamination free interfaces.
4. New package processes employed in Through Silicon Via production will be described, along with current cost reduction thrusts, to enable the student to understand the advantages and limits of the technologies.
5. Temporary bonding and wafer thinning processes will be highlighted, as well as the cost reduction approaches currently being pursued to enable wider adoption of TSV packages.
6. The trade-offs between silicon, glass, and organic interposers will be highlighted, along with the processes used for each.
7. Participants will gain an understanding of the surface mount technologies that enable today's fine pitch products.
8. The class will provide detailed references for participants to study and further deepen their understanding.

COURSE OUTLINE

1. The Package Development Process as a Package Technology:
   a. Materials and Process Co-Design
2. Molded Package Technologies:
   a. Die Attach
      i. Plasma Cleans
   b. Wire Bonding
      i. Au vs. Cu vs. Ag
      ii. Die Design for Wire Bonding
   c. Lead Frames
   d. Transfer and Liquid Molding
      i. Flash
      ii. Incomplete Fill
      iii. Wire Sweep
      iv. Green Materials
   e. Pre- vs. Post-Mold Plating
   f. Trim Form
   g. Saw Singulation
   h. High Temperature and High Voltage Materials
3. Flip Chip and Ball Grid Array Technologies:
   a. Wafer Bumping Processing
      i. Cu and Solder Plating
      ii. Cu Pillar Processing
   b. Die Design for Wafer Bumping
   c. Flip Chip Joining
   d. Underfills

   e. Substrate Technologies
      i. Surface Finish Trade-Offs
      ii. Core, Build-up, and Coreless
   f. Thermal Interface Materials (TIMs) and Lids
   g. Fine Pitch Warpage Reduction
   h. Stacked Die and Stacked Packages
   i. Material Selection for Board Level Temperature Cycling and Drop Reliability
4. Wafer Chip Scale Packages:
   a. Redistribution Layer Processing
   b. Packing and Handling
   c. Underfill vs. No-Underfill
5. Fan-Out Wafer Level Packages:
   a. Chip First vs. Chip Last Technologies
   b. Redistribution Layer Processing
   c. Through Mold Vias
6. Through Silicon Via Technologies:
   a. Current Examples
   b. Fundamental TSV Process Steps
      i. TSV Etching
      ii. Cu Deep Via Plating
      iii. Temporary Carrier Attach
      iv. Wafer Thinning
   c. Die Stacking and Reflow
   d. Underfills
   e. Interposer Technologies: Silicon, Glass, Organic
7. Surface Mount Technologies:
   a. PCB Types
   b. Solder Pastes
   c. Solder Stencils
   d. Solder Reflow



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San Jose, California, USA

Advanced CMOS/FinFET Fabrication
June 5, 2019 (Wed)
San Jose, California, USA

Interconnect Process Integration
June 6, 2019 (Thur)
San Jose, California, USA

Failure and Yield Analysis
June 3 – 6, 2019 (Mon – Thur)
San Jose, California, USA

Semiconductor Reliability / Product Qualification
June 10 – 13, 2019 (Mon – Thur)
San Jose, California, USA

IC Packaging Technology
June 17 – 18, 2019 (Mon – Tue)
San Jose, California, USA

CMOS, BiCMOS and Bipolar Process Integration
June 17 – 19, 2019 (Mon – Wed)
San Jose, California, USA

Failure and Yield Analysis
July 8 – 11, 2019 (Mon – Thur)
Singapore

Semiconductor Reliability / Product Qualification
July 15 – 18, 2019 (Mon – Thur)
Singapore