Issue 107 May 2018

InfoTracks

Semitracks Monthly Newsletter

Low-K Materials Properties Part 2

By Christopher Henderson, continued from last month

In this section, we'll cover chemical stability issues with low-k materials. In particular, we'll discuss thermal stability and water diffusion problems with these materials. The properties of these materials are key to understanding the reliability in these applications. The industry is just beginning to understand these materials and how they behave in thin films and semiconductor applications.

- HSQ is less stable than MSQ or SiCOH films, due to poor thermal stability of Si-H bonds
- Si-H bonds decompose more rapidly in low concentrations of O_2 (100 ppm)

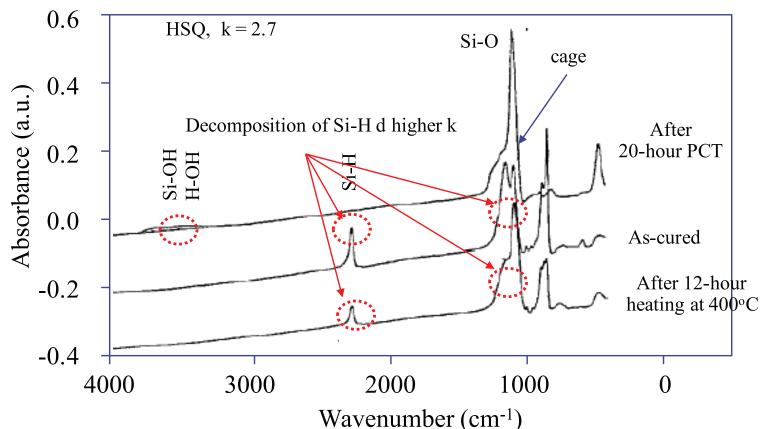

Figure 8. Effect of hi temp. N_2 and low temp. H_2O.

In this Issue:

Page 1 Low-K Materials Properties Part 2

Page 8 Technical Tidbit

Page 10 Ask the Experts

Page 11 Spotlight

Page 15 Upcoming Courses

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For a low-k dielectric to be integrated into the manufacturing process, thermal stability should not be an issue below 400°C. The backend processing steps take place at temperatures less than 400°C. It turns out that materials like hydrogen silsesquioxane, or HSQ, are not stable at these temperatures. This graph shows an FTIR spectrum of HSQ for three different conditions: after a 20-hour pressure cooker test, as cured, and after a 12-hour heating cycle at 400°C. Notice that the silicon-hydrogen bond absorbance goes down, indicating that the structure is losing hydrogen.

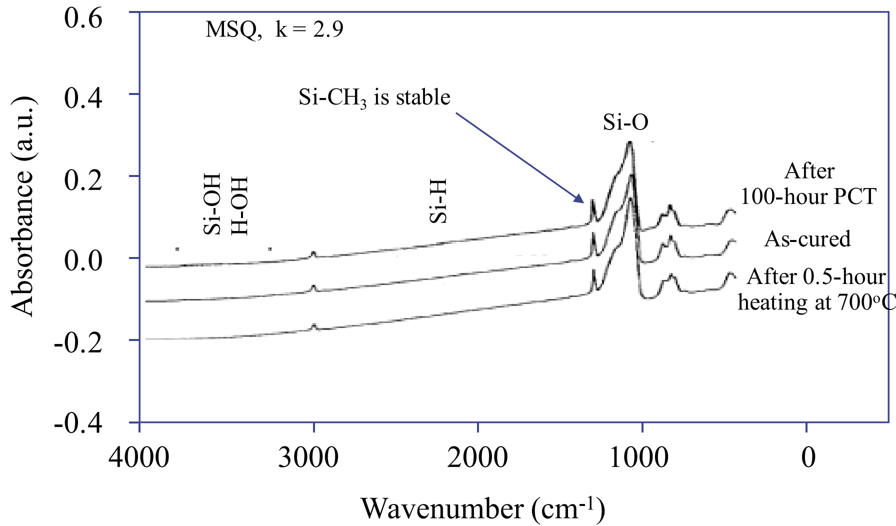

Figure 9. MSQ is more stable than MSQ films due to superior thermal stability of Si-CH3 bonds.

On the other hand, MSQ has methyl groups in the cage structure, so it is not as susceptible to degradation. The silicon-methyl bond is stable after pressure cooker testing, curing, and even after short temperature excursions as high as 700°C.

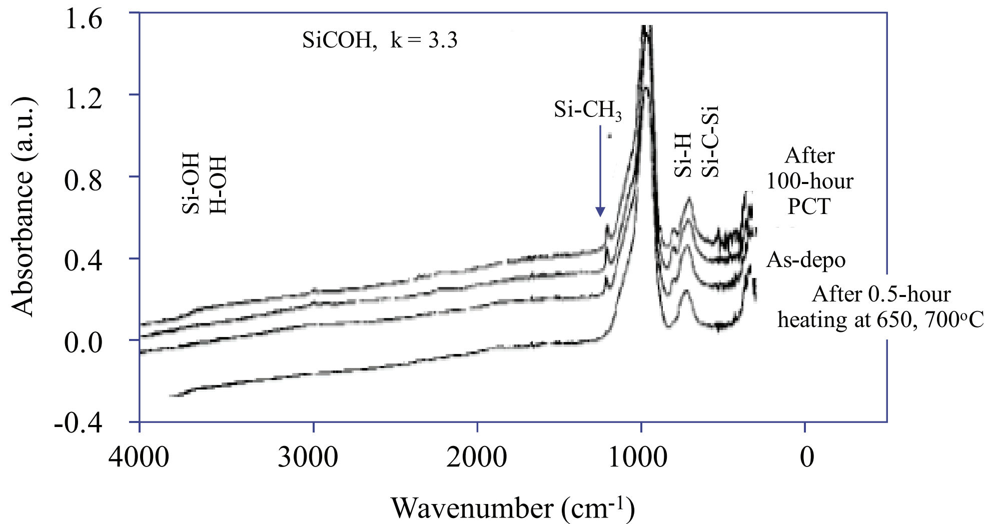

Figure 10. SiCOH is more stable than MSQ films due to superior thermal stability of Si-CH3 bonds.

The SiCOH dielectric material is also stable up to high temperatures. The silicon-methyl signal remains stable up to 700°C. So MSQ and SiCOH are thermally stable and can be used in products, whereas HSQ probably cannot.

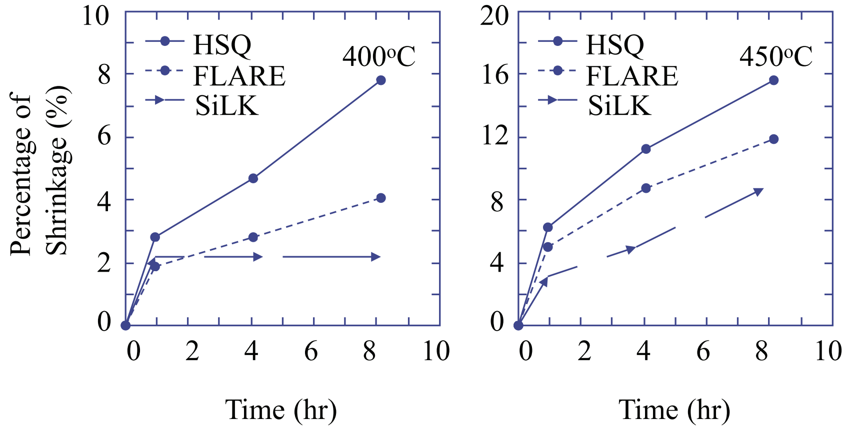

Figure 11. Thermal stability: polymers.

In addition to thermal breakdown, some of these films exhibit significant shrinkage at high cure temperatures. In the two graphs in Figure 11, notice that HSQ shrinks back by some 3 to 8 percent depending on the time at high temperature. At 450°C on the right, this increases to 6 to 16 percent. Notice that materials like Flare by Honeywell and SiLK by Dow Chemical exhibit much lower shrinkage.

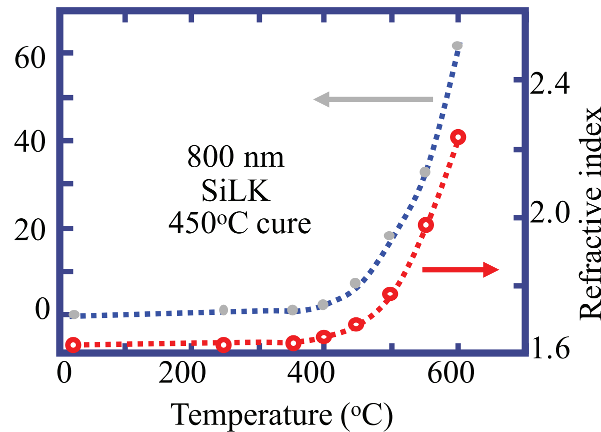

Figure 12. HSQ is less stable than SiLK or flare polymers.

Notice that as the temperature increases, even materials with less shrinkage begin to exhibit more. At temperatures of 600°C, SiLK exhibits a shrinkage of as much as 60 percent. Newer materials like HSQ are even more unstable than SiLK. Therefore, it is necessary to keep the process temperatures below 400°C.

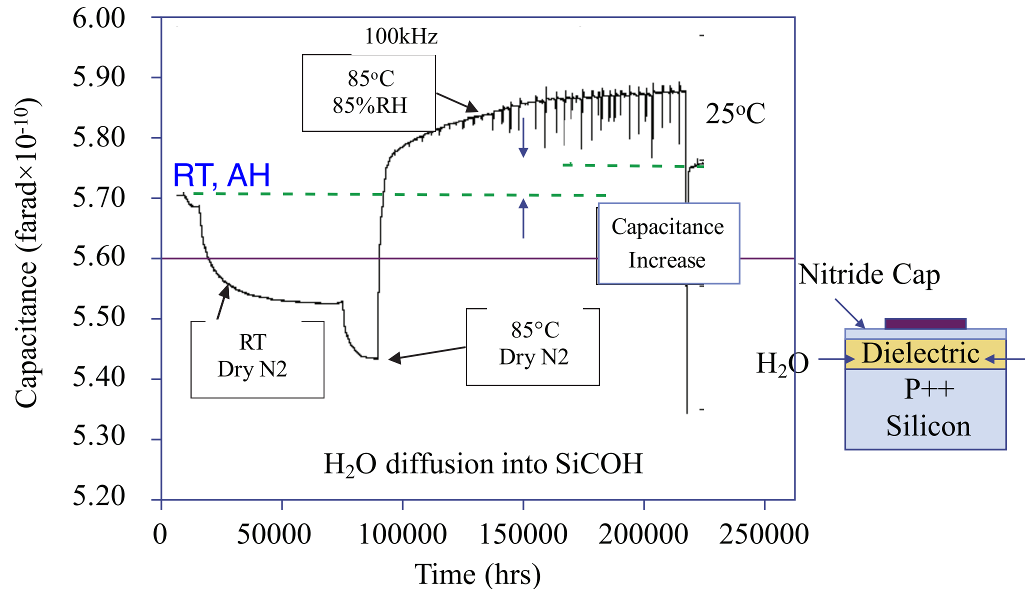

Figure 13. H_2O diffusion in low-k dielectrics.

Water diffusion into the structure of a low-k dielectric is a big problem. Most of today's packages are not hermetic. It is possible for water to diffuse into the dielectric, react with the copper interconnect, and cause a failure. For most low-k dielectrics, water diffusion is quite rapid. This requires the use of edge seals around the perimeter of the die to prevent water diffusion. In this experiment in Figure 13, the water diffusion is monitored using a capacitor. When water diffuses into the dielectric, the capacitance goes up. We start with a room temperature, ambient humidity environment. We then dry the device, causing the capacitance to go down. Water is then introduced, causing the capacitance to increase. This experiment was performed at 85°C, which could represent a realistic die temperature in a high-performance device.

The moisture diffusion into SiLK is reversible, whereas the moisture becomes trapped in SiCOH and does not significantly out-diffuse. The diffusivity is higher in SiLK and the activation energy is lower, indicating that SiLK will more readily and more quickly absorb moisture.

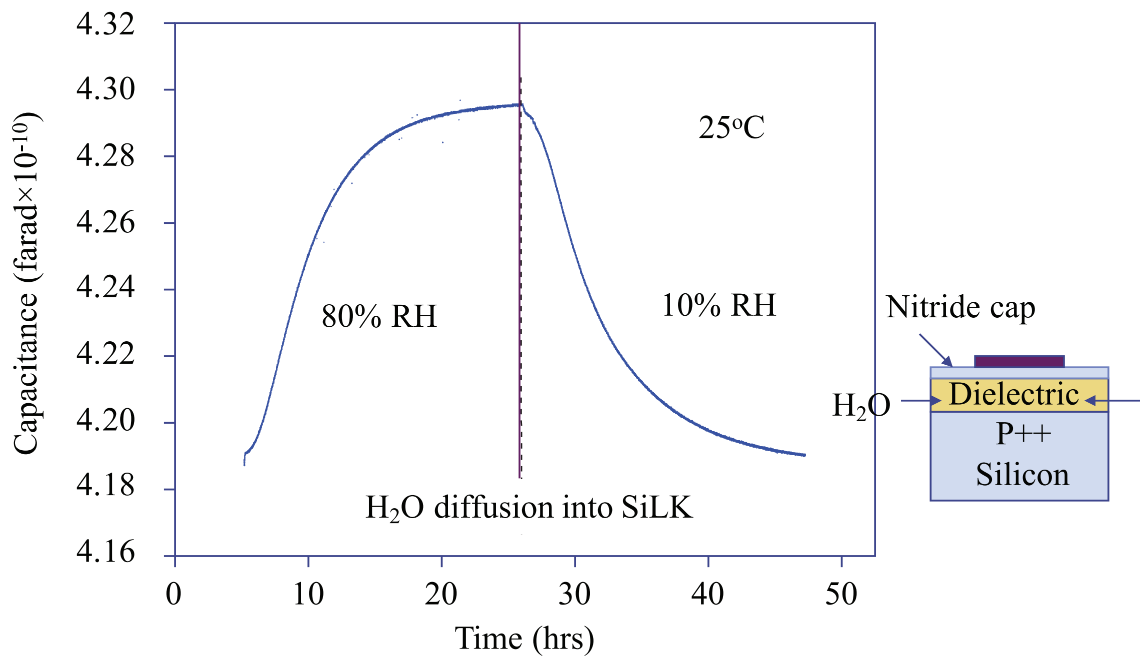

Figure 14. H2O diffusion in low-k dielectrics (cont.).

Notice that the water diffusion time constant is on the order of tens of hours, which is quite fast. Therefore, in order to use a low-k material the top dielectric must be a more impermeable dielectric, such as silicon nitride. The edge of the chip requires an edge seal, where the edge seal is a trench cut into the die and capped with silicon nitride. The other option is to use a hermetic package.

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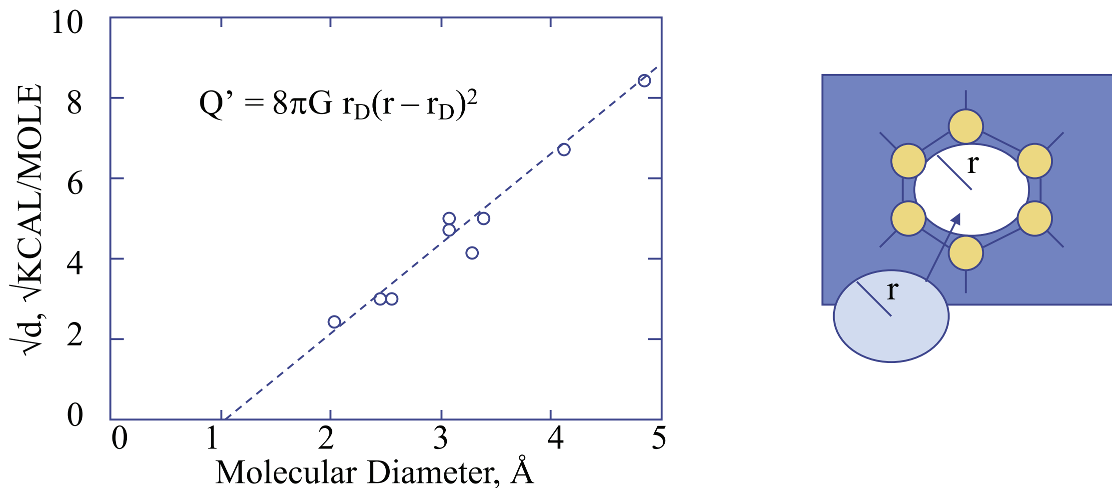

Figure 15. Molecular diffusion in glasses.

The diffusivity depends on the size of the molecule diffusing and the size of the openings in the dielectric. Therefore, water diffusivity will become worse as we move to more and more porous materials, since the openings in the dielectric will be larger.

		Diffusion coefficient (cm^2/sec)			
Molecule	**Diameter (Å)**	**25°C**	**1000°C**	**Activation energy Q' (kcal/mole)**	**Refs.**
Helium	2.0	$2.4(10)^{-8}$	$5.5(10)^{-5}$	4.8	7
Neon	2.4	$5(10)^{-12}$	$2.5(10)^{-6}$	8.8	8,10
Hydrogen	2.5	$2.2(10)^{-11}$	$7.3(10)^{-6}$	8.5	9,10
(deuterium)					
Argon	3.2		$1.4(10)^{-9}$	26.6	10
Oxygen	3.2		$6.6(10)^{-9}$	25	12
Water	3.3		$\sim 3(10)^{-9}$	17	29,30
Nitrogen	3.4			26?	1,31
Krypton	4.2			~46	10
Xenon	4.9			~72	32

Figure 16. Molecular diffusion into fused silica.

This table in Figure 16 shows some of the diffusion coefficients for elements into fused silica. Notice that small molecules or single atoms like helium, neon, and hydrogen diffuse rapidly, whereas larger atoms or molecules, such as argon oxygen and water diffuse more slowly.

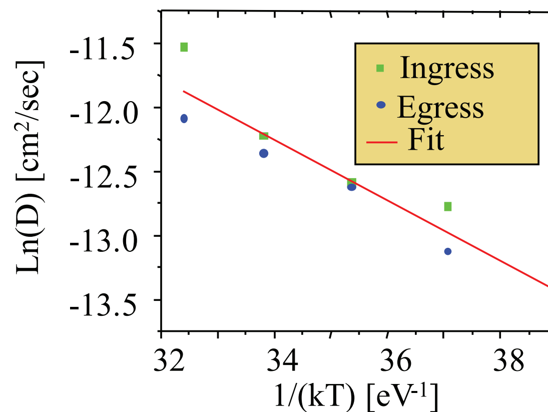

Figure 17. Water diffusion into SiLK.

This plot in Figure 17 shows water diffusion into SiLK. Notice that the diffusion rate is quite high, and the activation energy Q is quite low. The diffusion rate and activation energy are on par with a gas such as hydrogen in fused silica.

Chemical stability is another issue with low-k dielectrics. Many processing steps, especially resist strips, use oxygen plasma. Oxygen plasmas can degrade the low-k dielectrics. For example, an oxygen plasma will etch a polymer-based dielectric like SiLK. In materials such as SiCOH or methyl silsesquioxane, the oxygen plasma will convert the silicon-methyl bond to a silicon-oxygen bond. This increases the leakage and increases the dielectric constant. It also creates a hydrophilic surface, which can be problematic for some types of cleaning operations. A hydrogen plasma will remove carbon for the bulk material, while an ammonia-based plasma will remove both carbon and oxygen. Nitrogen-based plasmas will remove carbon from the surface layers. The inability to use plasmas without degradation is a serious issue for these materials.

In summary, the thermal stability is good for SiLK and the SiCOH dielectrics. It is not very good for other materials such as HSQ. For this reason, SiCOH is the preferred dielectric for the 65nm generation. Water diffusion is quite rapid in these materials. This can lead to potential reliability problems during device operation. Device manufacturers currently use edge seals to circumvent this problem. The low-k dielectrics tend to degrade in oxygen plasmas, which are used for resist strips.

In conclusion, we have discussed the materials properties of several low-k dielectrics in use as well as several potential low-k dielectrics. As the dielectric constants get lower, there is an increasing number of issues with their thermal properties, mechanical strength, and chemical stability. These materials each have strengths and weaknesses. Therefore, one may be better suited to a particular application than another. There is definitely not a “one size fits all” solution for current and future technology nodes.

Technical Tidbit

Polysilicon Resistors

In this technical tidbit, we discuss the polysilicon resistor. Engineers can form resistors in the polysilicon. These resistors can have the advantage that the drawn length and width will be the same as the electrical length and width, since we can ignore depletion effects in most cases. However, the carrier-transport is different in polysilicon than in single-crystal silicon. The polysilicon consists of grains ranging in size from 0.05 to 1.8 µm, depending on deposition and anneal conditions. Inside the grain, the atoms are arranged as in a periodic manner, as in a single-crystal, but the grains are surrounded by complex grain-boundaries. The grain boundaries consist of a few atomic layers of disordered atoms. Although we can't easily see what happens at these boundaries, scientists believe they are sites of high density of traps that can be charged and discharged. The charged traps deplete part or all the grain, creating a barrier to carrier transport. This means that although the resistance of the polysilicon resistor can be less than that of a silicon resistor; it will not be as effective as a metal film resistor in terms of low resistance, or noise, as we'll discuss shortly.

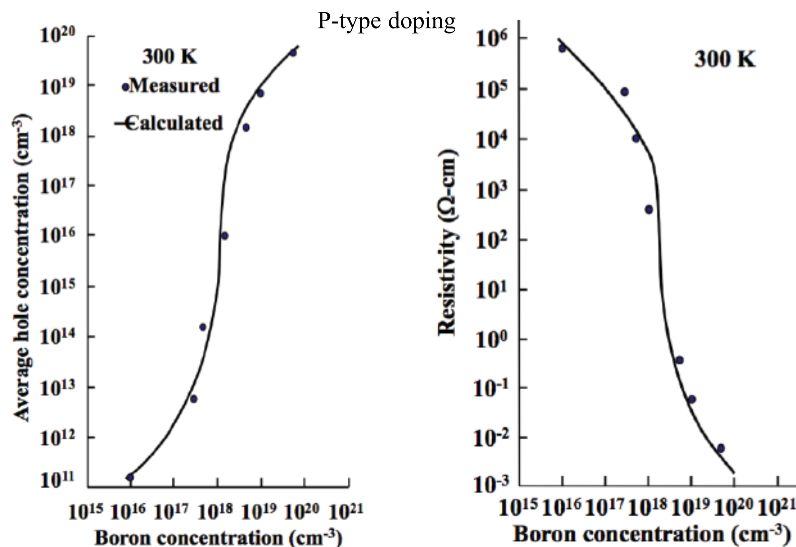

Figure 1. Carrier concentration vs. doping.

Let's look at some of the behaviors of the polysilicon resistor. The graph on the left shows hole concentration as a function of boron concentration, and the graph on the right shows resistivity as a function of boron concentration. At low boron concentrations N_A, the hole concentration p is much less than N_A. As N_A increases, p increases rapidly and approaches N_A at high boron concentrations. Notice the rapid increase in carrier concentration in the range 5×10^{17} to 5×10^{18} cm^{-3}. Within the grain, atoms are periodically arranged, and the transport of carriers is the same as it is in single-crystal silicon. However, the transport from grain to grain is more complex because of dopant segregation and barriers formed at grain boundaries. Over a doping range 5×10^{17} to 5×10^{18} the resistivity changes by 5 orders of magnitude. This is a challenge when designing high-resistivity polysilicon resistors.

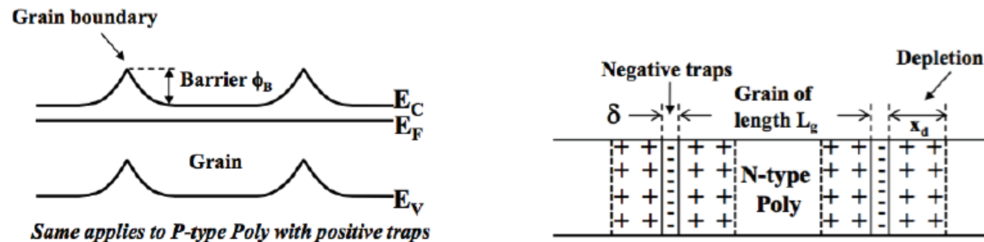

Figure 2. Carrier transport in polysilicon and TCR.

Let's delve into the carrier transport in polysilicon and the Temperature Coefficient of Resistance (TCR). The transport through the grain and across the grain boundaries is different. The transport inside the grain is the same as in single-crystal silicon. Resistance increases with increasing temperature because of increased phonon-scattering. The transport across the grain boundaries is similar to the transport across Schottky-barrier, like we show in the figure. This transport across the boundary occurs by thermionic emission. The probability for electrons to go over the barrier increases with temperature, and this tends to decrease the resistance as the temperature increases. So, the net resistance can increase, decrease, or remain almost constant with temperature. The lattice scattering within grains and thermionic emission across boundaries have opposite effects, causing the net TCR to be positive, negative or near zero. This depends on the grain size, the number of grain-boundaries along the current path, the dopant type and concentration, the segregation from boundary to grain and grain to boundary, and the annealing temperature and ambient conditions.

Ask the Experts

Q: Is a preconditioning failure considered to be a qualification failure per JEDEC JESD47?

A: I don't have a clear reason to give you, other than the wording in JESD47 says so. If you look in table 2 (section 5.6) you see the following item:

MSL Preconditioning Must be performed prior to: THB, HAST,TC, AC, & UHAST	JESD22 - A113	PC	Per appropriate MSL level per J-STD-020	Electrical Test (optional)

This statement in the table basically states that the electrical test after precon is optional, and that there are no reject criteria. You have to perform preconditioning for those tests, but the way the wording is stated, you could throw away the failures, keep the parts that pass preconditioning, submit those for the THB, HAST, TC, AC, and UHAST tests, and be within the letter of the law.

Now, you may want to go ahead and consider precon failures to be qualification failures internally, as it would be a good idea to analyze these devices to understand why they're failing, but you are not required to under JEDEC JESD47.

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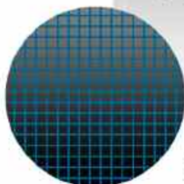

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Spotlight: Quality Basics

OVERVIEW

Quality is a fundamental aspect of the microelectronics industry. Today's ICs require ever greater levels of quality and reliability, as the electronics industry incorporates semiconductor components into more applications where the consequence of failure is high, like automotive, industrial, telecom, and medical. Engineers that work in the industry need a strong foundation to understand how to build quality into products. This requires an understanding of how quality impacts subjects like: chip technology, processing, design, testing, qualification and customer expectations. Your company needs competent engineers and scientists who understand these issues. ***Quality Basics*** is a one-day course that offers detailed instruction on a variety of subjects pertaining to semiconductor quality. This course is designed for every manager, engineer, and technician working in the semiconductor field, qualifying semiconductor components, or supplying tools to the industry.

Participants learn to develop the skills to determine the best process for qualification, how to identify issues and how to resolve them.

1. **Overview of Quality and Statistics.** Participants learn the fundamentals of quality and how the industry uses statistics, sample sizes, distributions to help quantify quality metrics.
2. **Failure Mechanisms.** Participants learn how product qualification and failure mechanisms relate to one another. We provide an overview of these mechanisms. These include: time-dependent dielectric breakdown, hot carrier degradation, bias temperature instability, electromigration, stress-induced voiding, moisture, corrosion, contamination, thermomechanical effects, interfacial fatigue, EOS, ESD, latchup, drop tests, etc.
3. **Qualification Principles.** Participants learn how the industry qualifies products for use in a customer's application.
4. **Testing for Quality.** Participants learn how the industry designs and develops test procedures for devices, how to balance quality and cost in test, and how testing relates to quality.

COURSE OBJECTIVES

1. The seminar will provide participants with a fundamental understanding of quality as it pertains to the semiconductor industry.
2. Participants will understand how we use data and statistics to quantify the level of quality in a product.
3. The seminar will identify major failure mechanisms; explain how they are observed, how they are modeled, and how they are handled during design and qualification.
4. The seminar will introduce the major qualification processes, including JEDEC JESD47, AEC Q-100, MIL-STD, and other related documents.
5. Participants will be able to identify the steps used in a return material authorization process for semiconductor devices.
6. Participants will understand how testing relates to the quality of a component.
7. Participants will be able to identify why customers require certain quality levels and how the industry works to meet those requirements.

INSTRUCTIONAL STRATEGY

By using a combination of instruction by lecture, video, problem solving and question/answer sessions, participants will learn practical approaches to the quality development process. From the very first moments of the seminar until the last sentence of the training, the driving instructional factor is **application**. We use instructors who are internationally recognized experts in their fields that have years of experience (both current and relevant) in this field. The handbook offers a number of pages of additional reference material the participants can use back at their daily activities.

COURSE OUTLINE

1. Introduction to Quality
   a. Basic Concepts
   b. Definitions
   c. Historical Information
2. Quality Statistics and Distributions
   a. Basic Statistics Concepts
   b. Distributions (Normal, Lognormal, Exponent, Weibull)
   c. Use of Statistics in Quality
   d. Exercise
3. Overview of Failure Mechanisms and Reliability
   a. Die Level Mechanisms
   b. Package Level Mechanisms
   c. Solder Joints
   d. Use Conditions
4. Designing Quality into a Product
   a. Design Rules
   b. Verification
   c. Reliability Testing
5. The Qualification Process
   a. JEDEC
   b. AEC
   c. MIL-STD
   d. Others
6. Testing for Quality
   a. Design for Test
   b. Validation
   c. Production Testing

   d. Exercise
7. Developing a Qualification Program
   a. Process
   b. Return Material Authorization
   c. Failure Analysis
   d. Corrective Action

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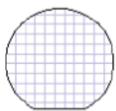
Our instructors are active in the field and they practice the disciplines daily. Please give us a call (505) 858-0454 or drop us an e-mail (info@semitracks.com).



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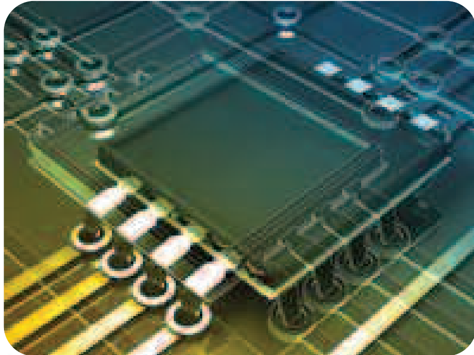
Semitracks is planning to demonstrate our Online Training Software for Failure Analysis at ISTFA. For more information, please contact us at info@semitracks.com



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(Click on each item for details)

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